SILICON GENERAL

Linear 1984-85

SILICON GENERAL
PRODUCT CATALOG

1984-85

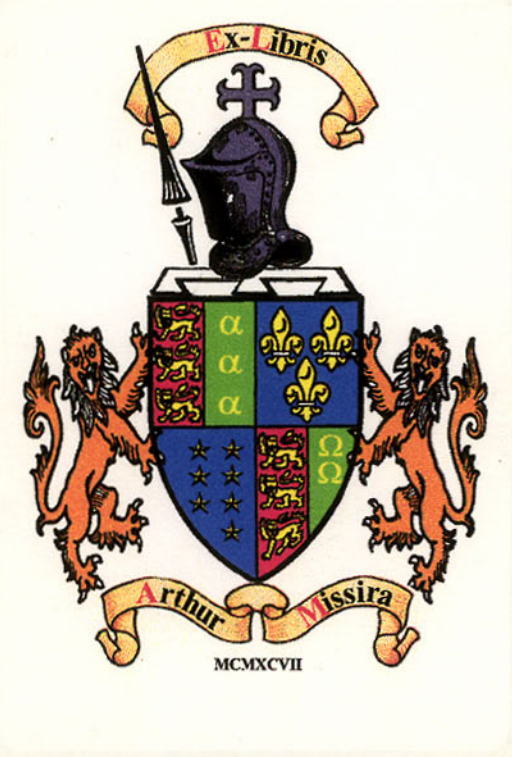
INTRODUCTION

Silicon General is committed to innovative excellence in the manufacture of integrated circuits. A unique combination of design and processing skills developed over the past ten years results in the continual generation of leadership solid state products.

All Silicon General devices are processed in the finest facilities available in strict accordance with the requirements of MIL-STD-883 level B and a complete range of screening and testing capabilities to higher levels is available.

This book describes Silicon General's complete line of products and includes information which will allow you to both specify and apply these products. Also included is a section describing our quality and reliability program.

If you need more information on these products or on other applications, please contact the nearest Silicon General representative listed in the back of this product catalog.


Ex-Libris
α
α
α
Ω
Ω
Arthur Missira
MCMXCVII

Product Selector Guide

*Consult factory for data.

Numerical Product Selector Guide

*Consult factory for data.

CROSS REFERENCE GUIDE

Silicon General	Fairchild	Motorola	National	Texas Inst.	Sprague
SG101	UA101	LM101	LM101	LM101	
*SG105	UA105		LM105		
SG107		LM107	LM107	LM107	
*SG109	UA109	LM109	LM109		
SG111	UA111	LM111	LM111	LM111	
				TL111	
SG117	UA117	LM117	LM117	TL117	
SG120-05		MC7905	LM120	UA7905	
SG120-12	UA7912	MC7912	LM120-12	UA7912	
SG120-15	UA7915	MC7915	LM120-15	UA7915	
			LM7915		
SG123	SH123	LM123	LM123		
SG124	UA124	LM124A	LM124A	LM124A	
SG133	SH133	LM133	LM133		
SG137		LM137	LM137	LM137	
SG138			LM138		
SG140-05			LM140-05		
SG140-12		LM140-12	LM140-12		
SG140-15		LM40-15	LM140-15		
SG140-18		LM140-18	LM140-18		
SG140-24		LM40-24			
SG150		LM150	LM150		
SG201	UA201	LM201	LM201	LM201	
	UA748	MC1748	LM748	UA748	
SG204		LM204	LM204		
SG205		LM205	LM205		
SG207		LM207	LM207	LM207	
*SG209	UA209	LM208	LM209		
SG211		LM211	LM211	LM211	
SG217		LM217	LM217	LM217	
SG220-05			LM220-05		
SG220-12			LM220-12		
SG220-15			LM220-15		
SG220-20					
SG223		LM223	LM223		
SG224	UA224	LM224	LM224	LM224	
SG233	SH233	LM233	LM233		
SG237		LM237	LM237	LM237	
SG238			LM238		
*SG239	UA239	LM239	LM239	LM239	
SG250		LM250	LM250		
SG301A	UA301A		LM301A	LM301A	
SG304		LM304	LM304		
SG305	UA305	LM305	LM305		
SG305A	UA305AC		LM305A		
SG307			LM307	LM307	
*SG309	UA309	LM309	LM309		
*SG310		LM310	LM310		
SG311	UA311	LM311	LM311	LM311	
SG317	UA317	LM317	LM317	LM317	
SG320-05	UA7905	MC7905	LM320-05	UA7905	
SG320-08	UA7908	MC7908		UA7908	
SG320-12	UA7912	MC7912	LM320-12	UA7912	
			LM7912		
SG320-15	UA7915	MC7915	LM320-15	UA7915	
SG320-18		MC7918		UA7918	
SG323	SH323	LM323	LM323		
SG324	UA324	LM324	LM324	LM324	
SG333	SH333	LM333	LM333		
SG337		LM337	LM337	LM337	
SG338			LM338		
SG340-05	UA7805	LM340-05	LM7805	LM340-05	
				TL780-05C	
SG340-06	UA7806	MC7806		UA7806	
		LM340-06		LM340-06	
SG340-08	UA7808	MC7808		UA7808	
		LM340-08		LM340-08	
SG340-12	UA7812	MC7812	LM7812	UA7812	
		LM340-12	LM340-12	LM340-12	
				TL780-12C	
SG340-15	UA7815	MC7815	LM7815	UA7815	
		LM340-15	LM340-15	LM340-15	
				TL780-15C	
SG340-18	UA7818	MC7818		UA7818	
		LM340-18		LM340-18	
SG340-20		MC78M20		UA78M20	
SG340-24	UA7824	MC7824		UA7824	
		LM340-24		LM340-24	
SG350		LM350	LM350		

Silicon General	Fairchild	Motorola	National	Texas Inst.	Sprague
*SG555	UA555	MC1455	LM555	NE555	
		MC1555		SE555	
*SG556	UA556	MC3456	LM556	NE556	
		MC3556		SE556	
SG723	UA723	MC1723	LM723	UA723	
*SG733	UA733	MC1733	LM733	UA733	
SG741	UA741	MC1741	LM741	UA741	
*SG741S		MC1741S			
*SG747	UA747	MC1747	LM747	UA747	
SG1436		MC1436	LM1436		
*SG1458	UA1458	MC1458	LM458		
SG1468		MC1468			
*SG1488	UA1488	MC1488	DS1488	MC1488	
				SN55188	
*SG1489	MC1489	DS1489	SN55189		
				SN75189	
SG1489A	UA1489A	MC1489A	DS1489A	SN55189A	
				SN75189A	
SG1495		MC1495			
SG1496		MC1496	LM1496		
		MC1596	LM1596		
SG1503		MC1503			
SG1524			LM1524	SG1524	
SG1525A		SG1525A			
SG1526		SG1526			UL58126
SG1527A		SG1527A			
SG1536		MC1536	LM1536		
*SG1558	UA1558	MC1588	LM1558	MC1558	
SG1568		MC1568			
SG1595		MC1595			
SG1596	UA796	MC1596	LM1596		
SG2001				ULN2001	ULN2001
					ULS2001
SG2002				ULN2002	ULN2002
					ULS2002
SG2003				ULN2003	ULN2003
					ULS2003
SG2004				ULN2004	ULN2004
					ULS2004
SG2021					ULN2021
					ULS2021
SG2022					ULN2022
					ULS2022
SG2023					ULN2023
					ULS2023
SG2024					ULN2024
					ULS2024
SG2064W				ULN2064	ULN2064
					ULS2064
SG2065W				ULN2065	ULN2065
					ULS2065
SG2066W				ULN2066	ULN2066
					ULS2066
SG2067W				ULN2067	ULN2067
					ULS2067
SG2068W				ULN2069	ULN2068
					ULS2068
SG2069W				ULN2069	ULN2069
					ULS2069
SG2070W					ULN2070
					ULS2070
SG2071W					ULN2071
					ULS2071
SG2074W		ULN2074		ULN2074	ULN2074
					ULS2074
SG2075W				ULN2075	ULN2075
					ULS2075
SG2076W				ULN2076	ULN2076
					ULS2076
SG2077W					ULN2077
					ULS2077
SG2524			LM2524	SG2524	
SG2525A		SG2525			
SG2526		SG2526			ULN8126
SG2527A		SG2527A			
*SG3059		CA3059			
*SG3079		CA3079			
*SG3146			LM3146		
SG3423		MC3423		MC3423	
SG3503		MC1503			
SG3523		MC3523		MC3523	
SG3524			LM3524	SG3524	
SG3525A		SG3525A		SG3525A	

Silicon General	Fairchild	Motorola	National	Texas Inst.	Sprague
SG3526		SG3526			ULN8126
SG3527A		SG3527A		SG3527A	
SG3821	UA3086	MC3386	LM3086		ULN2046
					ULN2086
SG3822		CA3054			ULN2054A
SG3851				SN75466	ULN2001
				ULN2001	ULS2001
SG4250			LM4250		
*SG6118					UDN6118
					ULN6118
SG7805	UA7805	MC7805	LM7805		
SG7805A	UA7805A				
SG7806	UA7806C	MC7806		UA7806	
SG7808	UA7808	MC7808		UA7808	
SG7812	UA7812	MC7812	LM7812	UA7812	
SG7815	UA7815	MC7815	LM7815	UA7815	
SG7818	UA7818	MC7818		UA7818	
SG7824	UA7824	MC7824		UA7824	
SG7905	UA7905	MC7905	LM7905	UA7905	
SG7908	UA7908	MC7908		UA7908	
SG7912	UA7912	MC7912	LM7912	UA7912	
SG7915	UA7915	MC7915	LM7915	UA7915	
			LM320-15		
SG7918		MC7918		UA7918	
SG55236				SN55236	
SG55325		MC55325	DS55325	SN55325	
SG75325		MC75325	DS75325	SN75325	
SG55326				SN55326	

Silicon General	Fairchild	Motorola	National	Texas Inst.	Sprague
SG75326				SN75326	
SG55327				SN55327	
SG75327				SN75327	
SG55450	55450			SN55450	
SG75450	75450	MC75450	DS75450	SN75450	
SG55460				SN55460	
SG75460				SN75460	
*SG55451			DS55451	SN55451	
*SG75451	7541A	MC75451	DS75451	SN75451	
*SG55461			DS55461	SN55461	
*SG75461	75461	MC75461	DS75461	SN75461	
*SG55452	55452		DS55452	SN55452	
*SG75452	75452	MC75452	DS75452	SN75452	
*SG55462			DS55462	SN55462	
*SG75462	75462	MC75462	DS75462	SN75462	
		MC75402			
*SG55453	55453		DS55453	SN55453	
*SG75453	75453		DS75453	SN75453	
*SG55463			DS55463	SN55463	
*SG75463		MC75463	DS75463	SN75463	
*SG55454			DS55454	SN55454	
*SG75454		MC75454	DS75454	SN75454	
*SG55464			DS55464	SN55464	
*SG75464			SG75464	SN75464	
*SG55470	55470	MC55470	DS55470	SN55470	
*SG75470	75470	MC75470	DS75470	SN75470	
*SG55471	55471	MC55471	DS55471	SN55471	
*SG75471	75471	MC75471	DS75471	SN75471	

*Not Recommended for New Design

Silicon General	Unitrode
SM600	PIC600
SM601	PIC600
SM602	PIC602
SM610	PIC610
SM611	PIC611
SM612	PIC612
SM625	PIC625
SM626	PIC626
SM627	PIC627
SM635	PIC635
SM636	PIC636
SM637	PIC637
SM645	PIC645
SM646	PIC646
SM647	PIC647
SM655	PIC655
SM656	PIC656
SM657	PIC657
SM600A	PIC7519
SM601A	PIC7520
SM602A	PIC7521
SM610A	PIC7522
SM611A	PIC7523
SM612A	PIC7524
SM625A	PIC7525
SM626A	PIC7526
SM627A	PIC7527

Silicon General	Unitrode
SM635A	PIC7528
SM636A	PIC7529
SM637A	PIC7530
SM645A	PIC7531
SM646A	PIC7532
SM647A	PIC7533
SM655A	PIC7534
SM656A	PIC7535
SM657A	PIC7536
SM600B	PIC7501
SM601B	PIC7502
SM602B	PIC7503
SM610B	PIC7504
SM611B	PIC7505
SM612B	PIC7506
SM625B	PIC7507
SM626B	PIC7508
SM627B	PIC7509
SM635B	PIC7510
SM636B	PIC7511
SM637B	PIC7512
SM645B	PIC7513
SM646B	PIC7514
SM647B	PIC7515
SM655B	PIC7516
SM656B	PIC7517
SM657B	PIC7518

PACKAGE SUFFIXES

	Silicon General	NSC	Signetics	Fairchild	Motorola	TI	RCA	AMD	Raytheon	Sprague
Plastic DIP 8-Lead	M	N	V A	T	P	P	E	PC	N DN DP	M
Plastic DIP 14, 16 and 18 Lead	N		B	P	P	N	E	PC	MP	A
TO 220	P	T	U	U	T	KC				T
Low Temperature Glass Hermetic Flat Pack	F	W		F	F	W		FM		J
TO-66 3 Lead 5 Lead 9 Lead	R				R				R TK	
Glass/Metal Flat Pack	F	F	Q	F	F	F S	K	F	J F Q	
TO-5, TO-39, TO-96, TO-99, TO-100 and TO-101	T	H	T K L DB	H	G	L	S* V1**	H	T H	D K
Ceramic DIP 8-Lead	Y	J	F	D	U	J			DC	R
Ceramic DIP 14, 16 and 18 Lead	J				L				DD	
TO 3 (Steel)	K	K					K		K	
(Aluminum)		KC	DA	K	K	K			LK	
SIP	S									W
Leadless Package	L			L		FC	LH	L		
Batwing	W					NE				B

Processing and Assembly Flow

The following outline describes the standard production processing procedures used exclusively at Silicon General to insure that all hermetically sealed products are manufactured in full conformance to the requirements of MIL-STD-883, Class B as a minimum.

- **BASIC RAW MATERIALS** — Silicon, Chemical, Masks, Headers, Wire, etc.
  - **QC SAMPLE INSPECTION** — Each arriving shipment is assigned a lot code identification to assure traceability and is then sample-processed through mechanical, visual, electrical, and functional lot acceptance testing prior to stocking.
- **WAFER FABRICATION**
  - **100% QC INSPECTION** — At each photomasking step, examining for:
    - Mask alignment and resolution
    - Oxide and diffusion quality
    - In-process electrical evaluation
- **100% ELECTRICAL PROBE OF COMPLETED WAFER** — Complete product performance testing on automatic test equipment to data sheet or customer specified limits.
  - **QC SAMPLE INSPECTION OF PROBING** — Performed on continuous sampling basis for evidence of adequate probe contact, correct inking, and freedom from probe point damage.
- **MANUFACTURING WAFER INVENTORY**
- **WAFER SCRIBE AND BREAK**
- **100% DIE SORT AT 100X MAGNIFICATION**
  - **QC SAMPLE INSPECTION (each lot)** — Per MIL-STD-883, Method 2010, Condition B. Minimum magnification of 100X.
- **DIE ATTACH**
  - **QC CONTINUOUS SAMPLING INSPECTION** — Per MIL-STD-883, Method 2010, Condition B minimum; including die shear strength testing per Method 2019.
- **LEAD BOND**
  - **QC CONTINUOUS SAMPLING INSPECTION** — Per MIL-STD-883, Method 2010, Condition B minimum; including bond pull testing per Method 2011, Condition D.
- **100% PRESEAL OPTICAL INSPECTION OF COMPLETED DEVICE** — Per MIL-STD-883, Method 2010, Condition B minimum.
  - **QC SAMPLE INSPECTION** — MIL-STD-883, Method 2010, Condition B minimum, magnification of 30X and 100X minimum.
- **FINAL SEAL** — Hermetically sealed in a controlled, dry environment.
  - **QC LOT INSPECTION SAMPLING AND ACCEPTANCE** — Post cap visual inspection per MIL-STD-883, Method 2010, Condition B; including Bond Pull Strength testing per Method 2011, Condition D, and Die Shear Strength testing per Method 2019.
- **MANUFACTURING POST-ASSEMBLY SCREENING** — See adjacent page.
- **100% ELECTRICAL TEST AND CLASSIFICATION** - Complete performance testing of all specified parameters to either data sheet or customer specified limits.
- **MARKING** — To customer specified or Silicon General identification plus date code traceable to seal date.
- **PRESHIP PACKING**
  - **QUALITY ASSURANCE** — Group A Preship Electrical Test and Final Visual Inspection per MIL-STD-883, Method 2009.
- **SHIP**

Post-Assembly Screening Procedures

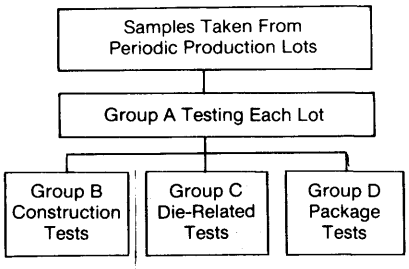
Silicon General manufactures products to the three standard levels of quality assurance processing outlined below. In addition, the company's unique flexibility allows ready accommodations to special customer requirements. The following screening procedures are in full compliance to MIL-M-38510 and all methods are as detailed in MIL-STD-883, Methods 5004 and 5005.

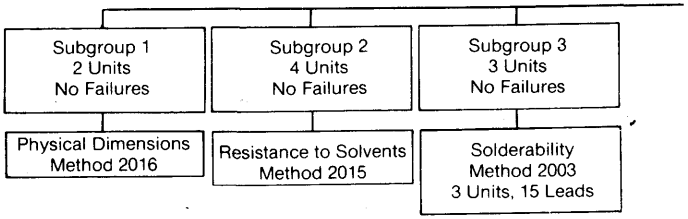
	MIL-STD-883, CLASS S		MIL-STD-883, CLASS B		STANDARD PRODUCT	
SCREEN	**METHOD**	**REQM'T**	**METHOD**	**REQM'T**	**METHOD**	**REQM'T**
Wafer Lot Acceptance	5007	Sample				
Non-Destructive Bond Pull	2023	100%				
Internal Visual Pre-Cap	2010, Condition A	100%	2010, Condition B	100%	2010, Condition B	100%
High Temperature Storage	1008, Condition C 24 Hours @ 150°C	100%	1008, Condition C 24 Hours @ 150°C	100%	1008, Condition C 24 Hours @ 150°C	100%
Temperature Cycling	1010, Condition C 10 Cycles, −65°C to +150°C	100%	1010, Condition C 10 Cycles, −65°C to +150°C	100%	1010, Condition C 10 Cycles, −65°C to + 150°C	100%
Constant Acceleration	2001, Condition E 30,000 g, Y_1 orientation	100%	2001, Condition E 30,000 g, Y_1 orientation	100%	2001, Condition E 30,000 g, Y1 orientation	100%
Particle Impact Noise Detection (PIND)	2020 Test Condition A					
Hermeticity a) Fine Leak b) Gross Leak	1014, Condition B 5 x 10^{-8} atm-cc/sec 1014, Condition C2	100% 100%	1014, Condition B 5 x 10^{-8} atm-cc/sec 1014, Condition C2	100% 100%	1014, Condition B 5 x 10^{-7} atm-cc/sec 1014, Condition C2	Sample Sample
Pre-Burn-in Electrical Test	Per Applicable Procurement Document Unit Serialization as required	100%	Per Applicable Procurement Document	100%		
Burn-in Test	1015, Dynamic 240 Hours @ 125°C (Note: An additional 72 Hours HTRB burn-in and interim electrical test as required)	100%	1015, Static or Dynamic 168 Hours @ 125°C	100%		
Final Electrical Test	Per Applicable Procurement Document		Per Applicable Procurement Document		Per Applicable Procurement Document	
a) DC @ 25°C		100%		100%		100%
b) DC @ Max and Min Rated Temperature		100%		100%		
c) Dynamic @ 25°C		100%		100%		
d) Functional @ 25°C		100%		100%		100%
Hermeticity a) Fine Leak b) Gross Leak	1014, Condition B 5 x 10^{-8}, atm-cc/sec 1014, Condition C2	100% 100%				
Radiographic	Method 2012	100%				
External Visual	Method 2009	100%	Method 2009	100%	Method 2009	100%
Quality Conformance Testing	5005		5005			
Group A	DC, AC Parameters	+25°C +125°C −55°C	DC, AC Parameters	+25°C +125°C −55°C	DC Parameters	+25°C
Groups B, C*, D	5005 Paragraph	3.5	5005 Paragraph	3.5		

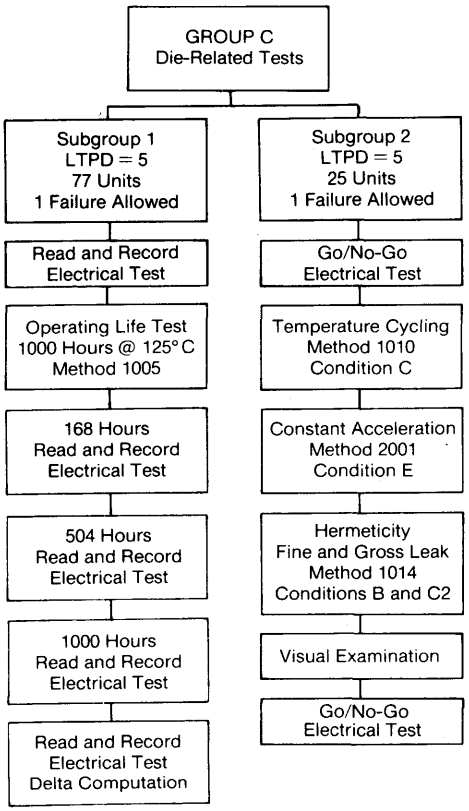
*Class B only.

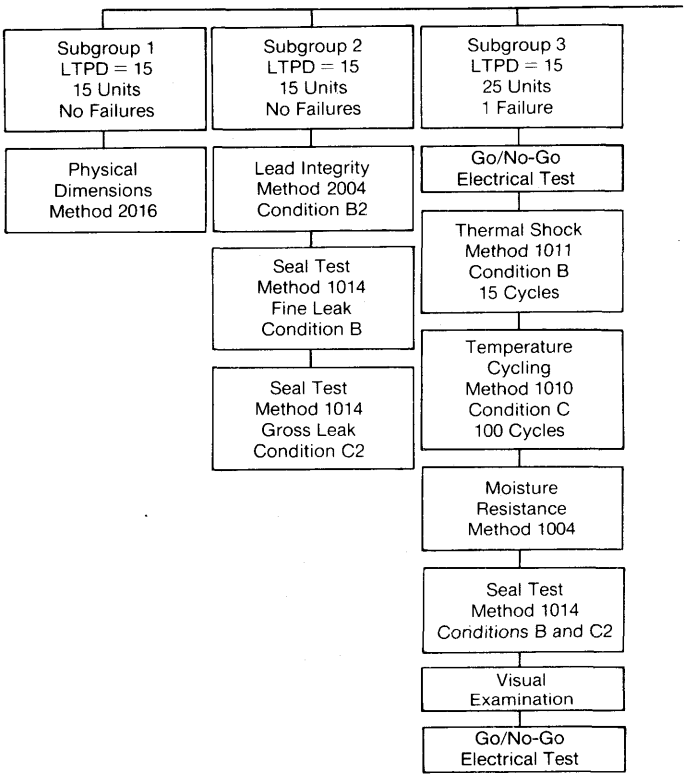
MIL-M-38510 Qualification and

The following Group B, C and D tests are performed on a periodic basis or when specified by the customer. This testing is in full compliance to MIL-M-38510 as detailed in MIL-STD-883, Method 5005, and although Class B quality level is shown below, other Class levels are also available.

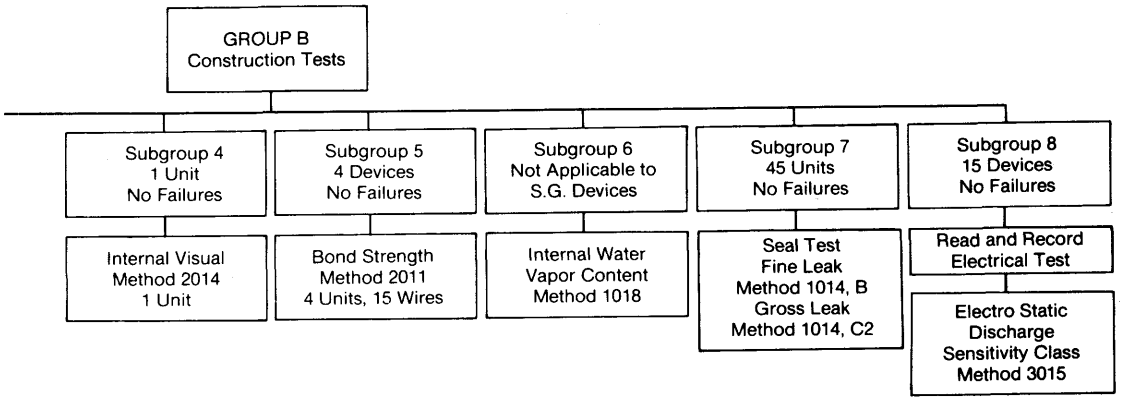


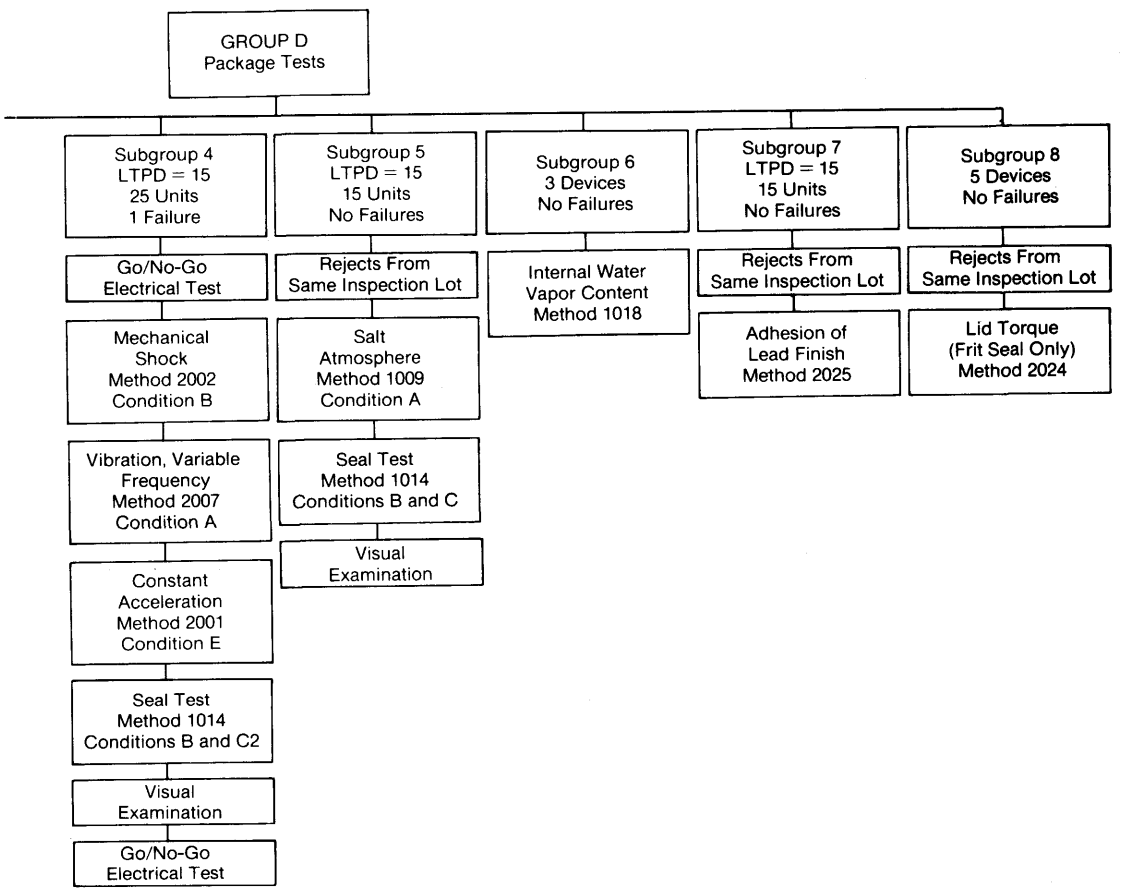






Quality Conformance Inspection





★★★★★ FIVE-STAR PROGRAM

FOR PLASTIC INTEGRATED CIRCUITS

The increased reliability of a 5 Star device will help you eliminate the high cost of circuit failure — an expense which can include the price of assembly rework, system downtime, service calls and customer goodwill. Costs that can range from $35 to $350 are not uncommon.

Silicon General's 5 Star Program removes marginal devices before shipment at a relatively low cost to you. This extra screening is done during the last stage of production and results in the highest levels of performance reliability, insuring customer satisfaction.

QUALITY IS...
a product's degree of conformance to its specified parameters. It pertains to the probability of defective units exisiting in a given lot when received by the user. Although zero percent defective is a goal, there will usually be some percentage of defective units in any lot of mass produced items. The number of defective units received by the user is a functiuon of the outgoing inspection criteria used by the supplier.

RELIABILITY IS...
a measurement of how well an initially good device will perform over time to its specified characteristics. Semiconductor failures primarily occur duing the early life phase of operation. After this phase, a low failure rate can be expected until the wear-out phase is eventually reached. Overall system reliability is improved if these early life failures are removed prior to system use.

TEST PROCEDURES ★★★★★

1. STABILIZATION BAKE. This is a process designed to stabilize electrical drift and accelerate chemical degradation such as surface contamination. It is a four hour bake at +175°C without electrical stress applied (similar to MIL-STD-883, Method 1008).

2. TEMPERATURE CYCLE. This is a screening process designed to mechanically stress the integrated circuit by alternately heating and cooling it. Potential failures are: bond failure, cracked packages or chips, etc. This process consists of ten cycles with ten minutes of dwell at −65C and at +150°C (air/air), with a maximum transfer time of five minutes (MIL-STD-883, Method 1010, condition C).

3. BURN-IN. The burn-in is performed specifically to screen out marginal devices, those with inherent defects, or defects resulting from manufacturing deviations which can cause time or stress-dependent failures. Without this conditioning, marginal circuits which initially meet all specifications could result in early lifetime failures under normal operating conditions. The test is conducted 100% under electrical stress conditions (similar to MIL-STD-883, method 1015) such as:

Type of Device	Electrical Stress
Bipolar Interface	Steady State Reverse Bias
Linear Devices	Steady State Forward Bias

4. QUALITY CONTROL AUDIT. A product's outgoing quality level from the manufacturer determines the probability of a user receiving defective units. Sampling procedures for 5 Star Integraded Circuits assures a tighter-than-normal outgoing quality level.

OUTLINE OF 5 STAR PROCEDURE

Silicon General Processing Flow
Pre-Conditioned Plastic Assembly

Wafer Fabrication

Elecrical Test
Wafer Probe

Plastic Assembly & Processing

100% Dice Visual Inspection
MIL-STD-883, Method 2010

100% Premold
Visual Inspection
MIL-STD-883, Method 2010

Stabilization Bake

Temperature Cycle

MIL-STD-883, Method 1010
(10 Cycles −65 to +150°C)

Electrical Test 100%
D.C. +25°C/Temperature Extremes
Burn-in 100% at 125°C
Or Equivalent

Electrical Test 100%
D.C., 25°C/Temperature Extremes
PDA=5% Exceeds PDA=5%
Re-Burn in 100%, 125°C

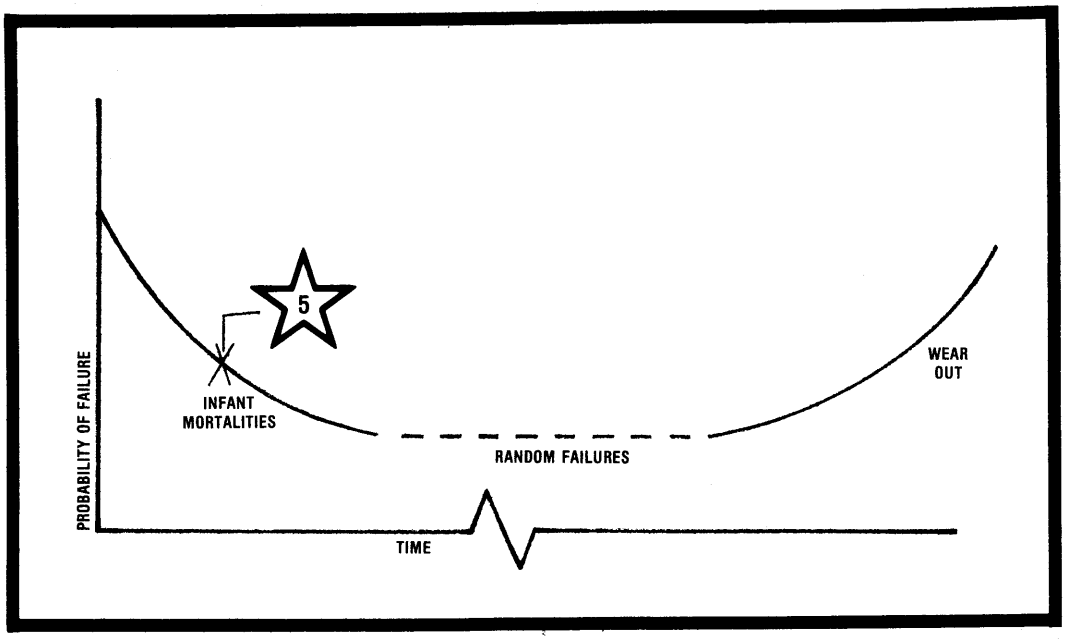
Electrical Test 100%
D.C. +25°C, PDA=2%

MEETS PDA=2%

Quality Control
Visual/Mechanical
Electrical D.C., A.C. @+25°C
LTPD=3, (SS=76, Acc=0)

SHIP

PROBABILITY OF FAILURE AS A FUNCTION OF TIME



RELATIVE FAILURE RATE vs. TIME

ORDERING INFORMATION:

All processed Silicon General Integrated Circuits are branded with the Silicon General 5-Star Trademark. The 5-Star identifies parts subject to the screening program for extra reliability. Devices processed in the 5-Star Burn-in Program are specified by adding the suffix ''5 S'' to the end of the part number. For example, to order SG3524 with this processing, specify SG3524N5S.

NOTE: The 5-Star Program is available on selected products. Please contact Silicon General or its local representatives to discuss your specific product interests.

VOLTAGE REGULATORS

SG LINEAR VOLTAGE REGULATORS

AMPS	TYPE	P/N	PACKAGE	VOLTAGE
5.0	POS. ADJ.	SG138	TO-3 (K)	+1.2 to +32
3.0	POS. FIXED	SG123	TO-3(K)	+5
	POS. FIXED	SG153		+5, 12, 15
	POS. ADJ.	SG150		+1.2 to +33
1.5	POS. FIXED	SG109	TO-3 (K) TO-66 (R) TO-220 (P)	+5
		SG140		+5, 6, 8, 12, 15,
		SG7800		18, 20, 24
	POS. ADJ.	SG117		+1.2 to +37
		SG117HV		+1.2 to +57
	NEG. FIXED	SG120		−5, 5.2, 8, 12,
		SG7900A		15, 18, 20
	NEG. ADJ.	SG137		−1.2 to −37
		SG137HV		−1.2 to −47
0.5	POS. FIXED	SG109	TO-39 (T)	+5
		SG140		+5, 6, 8, 12, 15,
		SG7800		18, 20, 24
	POS. ADJ.	SG117		+1.2 to +37
		SG117HV		+1.2 to +57
	NEG. FIXED	SG120		−5, 5.2, 8, 12,
		SG7900		15, 18, 20
	NEG. ADJ.	SG137		−1.2 to −37
		SG137HV		−1.2 to −47
0.2	DUAL TRACK	SG1501	TO-100 (T) DIP (J,N)	±15
0.15	POS. ADJ.	SG723	TO-96 (T) DIP (J)	+2 to +37
0.1	DUAL TRACK ADJ.	SG1502	DIP (J)	+10 to ±28
	POS. ADJ.	SG1532	TO-96 (T) DIP(J)	+2 to+38
	DUAL TRACK	SG1568/ 1468	TO-100 (T) DIP (J) TO-66 (R)	±15
0.025	NEG. ADJ.	SG104	TO-100 (T)	−0.015 TO −40
0.020	POS. ADJ.	SG105	TO-99 (T) DIP (Y)	+4.5 TO +40
0.010	PRECISION REFERENCE	SG1503	TO-39 (T) DIP (Y)	+2.5V

Negative Voltage Regulators

This circuit is a negative voltage regulator designed for both linear and switching applications. It is a complement of the SG100/200/300, SG105/205/305 and SG723/723C intended for systems requiring regulated negative voltages having a common ground with the unregulated supply. With an input voltage rating of up to 50V, this device will deliver load currents to 25mA. Adding external transistors will increase the current capability to greater than 10 amps and further improve regulation.

- **Output voltage adjustable from 15mV to 40V**
- **1mV regulation no load to full load**
- **0.01%/V line regulation**
- **1% maximum temperature variation**

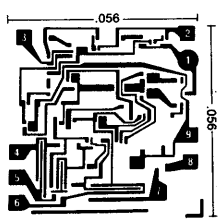
PARAMETERS*	104	204	304	UNITS
Operating Temperature Range	−55 to +125	−25 to +85	0 to +70	°C
Package Types	T			
Input Voltage Range	−50 to −8		−40 to −8	V
Output Voltage Range	−40 to −0.015		−30 to −0.035	V
Input/Output Differential I_O = 20 mA[1]	2.0 to 50		2.0 to 40	V
Load Regulation[2] $0 \leq I_O \leq 20$ mA, $R_{SC} = 15\Omega$	5mV			–
Line Regulation[3] $V_{out} \leq -5V$, $\Delta V_{in} = 0.1\ V_{in}$	0.1			%
Ripple Feed thru $C_{1G} = 10\mu f$, f = 120Hz, $-7V \leq V_{in} \leq -15V$	1.0		1.0	mV/V
Output Voltage Scale Factor $R_{23} = 2.4k\Omega$	1.8 to 2.2		1.8 to 2.2	V/kΩ
Temperature Stability $V_O \leq -1V$	1.0		1.0	%
Output Noise Voltage $C_{1G} = 0\mu F$ BW = 10Hz to 10KHz $V_O \leq -5V$	0.007 (typ)		0.007 (typ)	%
Standby Current Drain $V_O = 0$, $I_L = 5$ mA	2.5		2.5	mA
Long Term Stability $V_O \leq -1V$	1.0		1.0	%

*Parameters apply at junction temperatures equal to or less than operating temperature range unless otherwise specified. The line and load regulation specifications are for constant junction temperature. Temperature drift effects must be taken into account separately when the unit is operating under conditions of high dissipation.

[1] With I_O = 5 mA, min differential is 0.5V. With external transistors differential is increased, in the worst case, by approx. 1V.

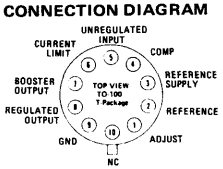
[2] Output current and load regulation can be improved with external transistors. Improvement factor will be approx. equal to the composite current gain of added transistors.

[3] With zero output, the dc line regulation is determined from the ripple rejection. Hence, with output voltages between 0 volts and −5 volts, a dc output variation, determined from the ripple rejection, must be added to find the worst-case line regulation.

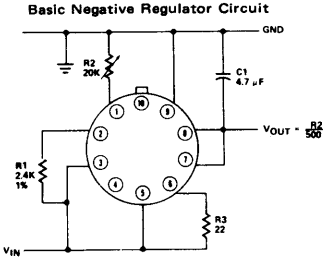


SG104/204/304 Chip (See T-package diagram for pad functions)

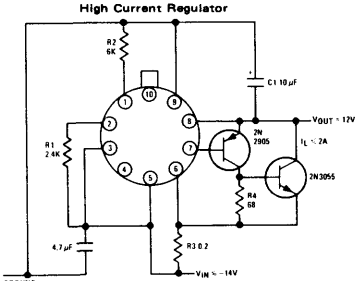
CONNECTION DIAGRAM



Basic Negative Regulator Circuit



High Current Regulator



1

Positive Voltage Regulators

This circuit is a positive voltage regulator designed for both linear and switching applications. Inherent component tracking of the monolithic integrated circuit process provides a high degree of stability and accuracy in addition to fast response to both line and load transients. With an input voltage rating of up to 50V, this device will deliver load currents of 20mA (45mA with 305A). Adding external transistors will increase the current capability to greater than 10 amps and further improve regulation.

- **Output voltage adjustable from 4.5 to 40V**
- **Load regulation better than 0.01%/mA**
- **Line regulation better than 0.06%/V**
- **Ripple rejection of 0.01%/V**
- **1.0% maximum temperature variation**

PARAMETERS*	105	205	305	305A	UNITS
Operating Temperature Range	−55 to +125	−25 to +85	0 to +70	0 to 70	°C
Package Types	T, J, Y	T, J, Y, M, N		T	–
Input Voltage Range	8.5 to 50		8.0 to 40	8.5 to 50	V
Output Voltage Range	4.5 to 40		4.5 to 30	4.5 to 40	V
Input/Output Differential	3.0 to 30		3.0 to 30	3.0 to 30	V
Load Regulation	0.1 [2,3]		0.1 [2,3]	2.0 [2,3]	%
Line Regulation $V_{in} - V_{out} \leq 5V$	0.06				%/V
Line Regulation $V_{in} - V_{out} > 5V$	0.03				%/V
Ripple Feed thru Cref = 10μf, f = 120Hz	0.01		0.01	0.003 (typ)	%/V
Temperature Stability	1.0		1.0	1.0	%
Output Noise Voltage (10 Hz ≤ f ≤ 10 KHz, C_{ref} = 0)	0.005 (typ)		0.005 (typ)	0.005 (typ)	%
Feedback Sense Voltage	1.7 (typ)		1.7 (typ)	1.55 to 1.85	V
Standby Current Drain	2.0		2.0	2.0	mA
Minimum Load Current	0		0	0	mA
Long Term Stability	1.0		1.0	1.0	%

*Parameters apply at junction temperatures equal to or less than operating temperature range, and for a divider impedance seen by the feedback terminal of 2VΩ, unless otherwise specified.

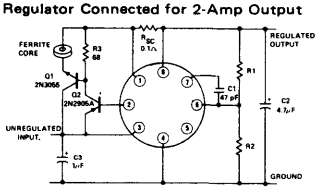
[1] I_L < 12mA, Rsc = 0Ω. Output current and load regulation can be improved with external transistors. Improvement factors will be approx. equal to the composite current gain of added transistors.

[2] Applies for constant junction temperature. Temperature drift effects must be taken into account separately when the unit is operating under conditions of high dissipation.

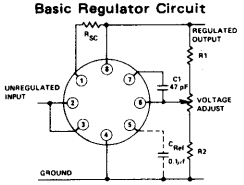
[3] Same as Note 1, except Rsc = 10Ω.

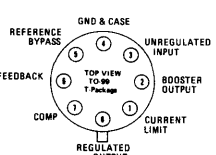
CONNECTION DIAGRAMS

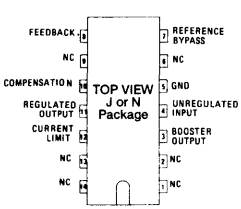
Regulator Connected for 2-Amp Output

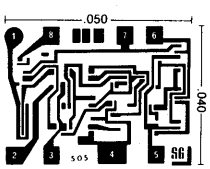


Basic Regulator Circuit









SG105/205/305 Chip (See T-Package diagram for pad functions).

5 Volt Fixed Voltage Regulators

The SG109 series is a completely self-contained 5V regulator. Designed to provide local regulation at currents up to 1 amp for digital logic cards, this device is available in two commonly used transistor packages – the solid header TO–5 and the TO–3 power package.

A major feature of the SG109's design is its built-in protective features which make it essentially blowout proof. These consist of both current limiting to control the peak currents and thermal shutdown to protect against excessive power dissipation. With the only added component being the possible need for an input bypass capacitor, this regulator becomes extremely easy to apply.

- **Fully compatible with TTL and DTL**
- **Output current in excess of 1 amp**
- **Internal thermal overload protection**
- **No additional external components**

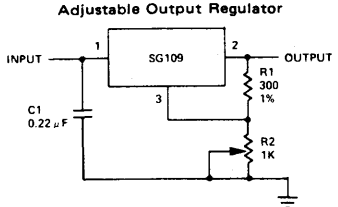
PARAMETERS[1]	109	209	309	UNITS
Operating Temperature Range	–55 to +150	–25 to +150	0 to +125	°C
Package Types	T, K		T, K	–
Output Voltage	4.9 to 5.1		4.8 to 5.2	V
Line Regulation 7V ≤ V_{in} ≤ 25V	50			mV
Load Regulation 5mA ≤ I_{out} ≤ 0.5A (1.5A for TO-3)	TO-5: 50; TO-3: 100			mV
Total Output Voltage Tolerance[2]	4.75 to 5.25			V
Quiescent Current V_{in} ≤ 25V	10			mA
Ripple Rejection 10 Hz ≤ f ≤ 10kHz	75 (typ)			dB
Output Noise Voltage 10Hz ≤ f ≤ 100kHz	40 (typ)			μVrms
Output Impedance 10Hz ≤ f ≤ 10kHz	0.1 (typ)			Ω
Long Term Stability	10			mV

[1] Unless otherwise specified, T_j = 25°C, V_{in} = 10 Volts, and I_{out} = 0.1A.

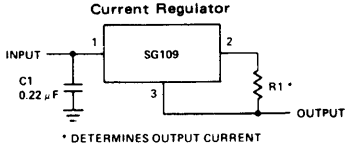
[2] 7V ≤ V_{in} ≤ 25V, 5mA ≤ I_{out} ≤ 1.0A (0.2A for TO-5), P ≤ 20W (2W for TO-5), ΔT_j max.

$T_j$max = –55°C to +150°C for the SG109
= –25°C to +150°C for the SG209
= 0°C to +125°C for the SG309

Adjustable Output Regulator

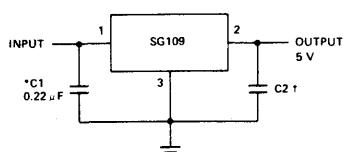


Current Regulator



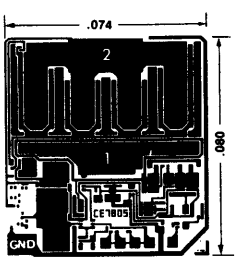
* DETERMINES OUTPUT CURRENT

Fixed 5V Regulator



* REQUIRED IF REGULATOR IS AN APPRECIABLE DISTANCE FROM POWER SUPPLY FILTER.

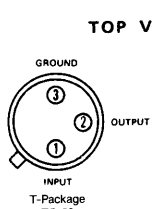
† ALTHOUGH NO OUTPUT CAPACITOR IS NEEDED FOR STABILITY IT DOES IMPROVE TRANSIENT RESPONSE.



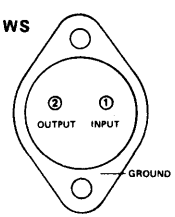
SG109/209/309 Chip

CONNECTION DIAGRAMS

TOP VIEWS

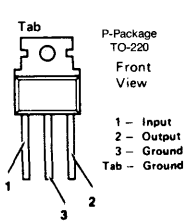


T-Package
TO-39



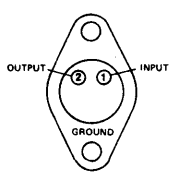
K-Package
TO-3

(CASE IS INTERNALLY CONNECTED TO GROUND)



P-Package
TO-220
Front
View

1 – Input
2 – Output
3 – Ground
Tab – Ground



R-Package
TO-66

1

1.5 - AMP Three Terminal Adjustable Voltage Regulator

DESCRIPTION

The SG117A Series are 3-terminal positive adjustable voltage regulators which offer improved performance over earlier devices. A major feature of the SG117A is the output voltage tolerance is guaranteed at a maximum of ± 1%, allowing an overall power supply tolerance to be better than 3% using inexpensive 1% resistors. Line and load regulation performance has been improved as well. Additionally, the SG117A reference voltage is guaranteed not to exceed 2% when operating over the full load, line and power dissipation conditions. The SG117A adjustable regulators offer an improved solution for all positive voltage regulator requirements with load currents up to 1.5 amps.

FEATURES

- **1% Output Voltage Tolerance**
- **0.01%/V Line Regulation**
- **0.3% Load Regulation**
- **Min. 1.5 Output Current**

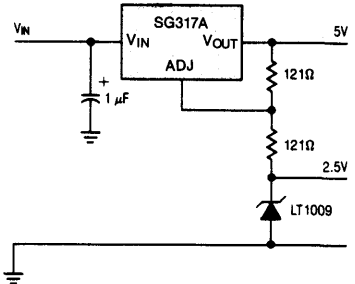
APPLICATIONS

Wide Range Power Supplies

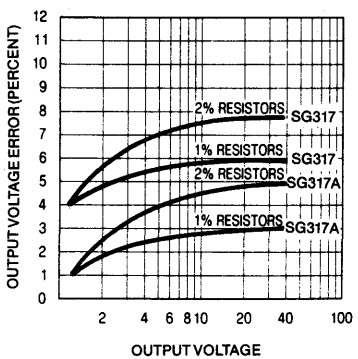
Constant Current Supplies

Voltage Programmable Supplies

Regulator with Reference



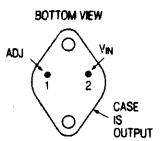
Output Voltage Error



ABSOLUTE MAXIMUM RATINGS

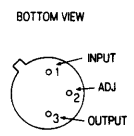
Power Dissipation ..... Internally Limited
Input to Output Voltage Differential 40V
Operating Junction Temperature Range
SG117A/117 ..... −55 °C to 150 °C
SG217A/SG217 ..... −25 °C to 150 °C
SG317A/SG317 ..... 0 °C to 150 °C
Storage Temperature Range
SG117A/117 ..... −65 °C to 150 °C
SG217A/SG217 ..... −65 °C to 150 °C
SG317A/SG317 ..... 0 °C to 150 °C
Lead Temperature (Soldering, 10 sec.) .. 300 °C

PACKAGE ORDER INFORMATION



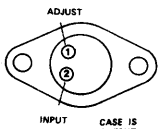
K PACKAGE
TO-3 METAL CAN
(STEEL)

ORDER PART NO.
SG117AK
SG217AK
SG317AK
SG117K
SG217K
SG317K



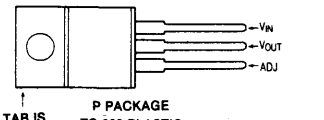
T PACKAGE
TO-39 METAL CAN

ORDER PART NO.
SG117AT
SG217AT
SG317AT
SG117T
SG217T
SG317T



R-Package
TO-66
METAL CAN

ORDER PART NO.
SG117AR
SG217AR
SG117R
SG217R



P PACKAGE
TO-220 PLASTIC

ORDER PART NO.
SG317AP
SG317P

ELECTRICAL CHARACTERISTICS (See Note 1)

SYMBOL	PARAMETER	CONDITIONS		SG117A/SG217A MIN	SG117A/SG217A TYP	SG117A/SG217A MAX	SG117/SG217 MIN	SG117/SG217 TYP	SG117/SG217 MAX	UNITS
V_{REF}	Reference Voltage	I_{OUT} = 10mA T_J = 25°		1.238	1.250	1.262				V
		3V ≤ (V_{IN} − V_{OUT}) ≤ 40V 10mA ≤ I_{OUT} ≤ I_{max}, ≤ P_{max}	•	1.225	1.250	1.270	1.20	1.25	1.30	V
$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	Line Regulation	3V ≤ (V_{IN} − V_{OUT}) ≤ 40V, (See Note 2)			0.005	0.01		0.01	0.02	%/V
			•		0.01	0.02		0.02	0.05	%/V
$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	Load Regulation	10mA ≤ I_{OUT} ≤ I_{max} (See Note 2) V_O ≤ 5V			5	15		5	15	mV
		V_O ≥ 5V			0.1	0.3		0.1	0.3	%
		V_O ≤ 5V	•		20	50		20	50	mV
		V_O ≥ 5V	•		0.3	1		0.3	1	%
	Thermal Regulation	T_A = 25°C, 20msec Pulse			0.002	0.02		0.03	0.07	%/W
	Ripple Rejection	V_O = 10V, f = 120Hz C_{ADJ} = 0			65			65		dB
		C_{ADJ} = 1μF	•	66	80		66	80		dB
I_{ADJ}	Adjust Pin Current				50	100		50	100	μA
ΔI_{ADJ}	Adjust Pin Current Change	10mA ≤ I_{OUT} ≤ I_{max} 2.5V ≤ (V_{IN} − V_{OUT}) ≤ 40V	•		0.2	5		0.2	5	μA
I_{min}	Minimum Load Current	(V_{IN} − V_{OUT}) = 40V	•		3.5	5		3.5	5	mA
	Current Limit	(V_{IN} − V_{OUT}) ≤ 15V K Package	•	1.5	2.2		1.5	2.2		A
		T Package	•	0.5	0.8		0.5	0.8		A
		(V_{IN} − V_{OUT}) = 40V, T_J = 25°C K Package	•	0.3	0.4		0.3	0.4		A
		T Package	•	0.15	0.2		0.15	0.2		A
$\frac{\Delta V_{OUT}}{\Delta Temp}$	Temperature Stability	0°C ≤ T_J ≤ 125°C			1	2		1		%
$\frac{\Delta V_{OUT}}{\Delta Time}$	Long Term Stability	T_A = 125°C			0.3	1		0.3	1	%
e_n	RMS Output Noise (% of V_{OUT})	T_A = 25°C, 10Hz ≤ f ≤ 10kHz			0.001			0.001		%
θ_{jc}	Thermal Resistance Junction to Case	T Package			12	15		12	15	C/W
		K Package			2.3	3		2.3	3	C/W

SYMBOL	PARAMETER	CONDITIONS		SG317A MIN	SG317A TYP	SG317A MAX	SG317 MIN	SG317 TYP	SG317 MAX	UNITS
V_{REF}	Reference Voltage	I_{OUT} = 10mA T_J = 25°		1.238	1.250	1.262				V
		3V ≤ (V_{IN} − V_{OUT}) ≤ 40V 10mA ≤ I_{OUT} ≤ I_{max}, P ≤ P_{max}	•	1.225	1.250	1.270	1.20	1.25	1.30	V
$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	Line Regulation	3V ≤ (V_{IN} − V_{OUT}) ≤ 40V, (See Note 2)			0.005	0.01		0.01	0.04	%/V
			•		0.01	0.02		0.02	0.07	%/V
$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	Load Regulation	10ma ≤ I_{OUT} ≤ I_{max} (See Note 2) V_O ≤ 5V			5	25		5	25	mV
		V_O ≥ 5V			0.1	0.5		0.1	0.5	%
		V_O ≤ 5V	•		20	50		20	70	mV
		V_O ≥ 5V	•		0.3	1		0.3	1.5	%
	Thermal Regulation	T_A = 25°C, 20msec Pulse			0.002	0.02		0.03	0.07	%/W
	Ripple Rejection	V_O = 10V, f = 120Hz C_{ADJ} = 0			65			65		dB
		C_{ADJ} = 1μF		66	80		66	80		dB
I_{ADJ}	Adjust Pin Current				50	100		50	100	μA
ΔI_{ADJ}	Adjust Pin Current Change	10mA ≤ I_{OUT} ≤ I_{max} 2.5V ≤ (V_{IN} − V_{OUT}) ≤ 40V	•		0.2	5		0.2	5	μA
I_{min}	Minimum Load Current	(V_{IN} − V_{OUT}) = 40V	•		3.5	10		3.5	10	mA
	Current Limit	(V_{IN} − V_{OUT}) ≤ 15V K, R, & P Package	•	1.5	2.2		1.5	2.2		A
		T Package	•	0.5	0.8		0.5	0.8		A
		(V_{IN} − V_{OUT}) ≤ 40V = 25°C K, R, & P Package	•	0.15	0.4		0.15	0.4		A
		T Package	•	.075	0.2		.075	0.2		A
$\frac{\Delta V_{OUT}}{\Delta Temp}$	Temperature Stability	0°C ≤ T_J ≤ 125°C			1	2		1		%
$\frac{\Delta V_{OUT}}{\Delta Time}$	Long Term Stability	T_A = 125°C			0.3	1		0.3	1	%
e_n	RMS Output Noise (% of V_{OUT})	T_A = 25°C, 10Hz ≤ f ≤ 10kHz			0.001			0.001		%
θ_{jc}	Thermal Resistance Junction to Case	T Package			12	15		12	15	C/W
		K Package			2.3	3		2.3	3	C/W
		P Package			4	5		4	5	C/W

The • denotes the specifications which apply over the full operating temperature range.

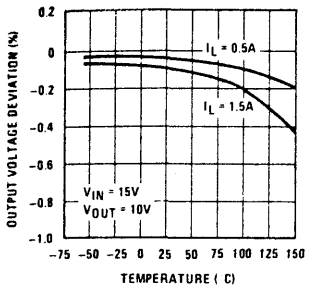
Note 1: Unless otherwise specified, these specifications apply for V_{IN} − V_{OUT}; and I_{OUT} = 0.1A for the TO-39 and I_{OUT} = 0.5A for the TO-3 and TO-220 packages. Although power dissipation is internally limited, these specifications are applicable for power dissipations of 2W for the TO-39, and 20W for the TO-3 and TO-220. I_{MAX} is 1.5A for the TO-3 and TO-220 packages and 0.5A for the TO-39.

Note 2: Regulation is measured at constant junction temperature, using pulse testing with a low duty cycle. Changes in output voltage due to heating effects are covered under the specification for thermal regulation.

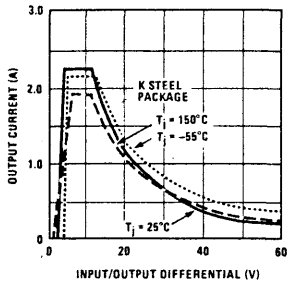
1

Typical Performance Characteristics (K and T Packages)

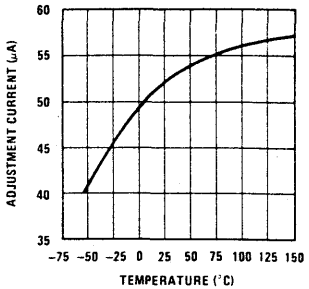
Load Regulation



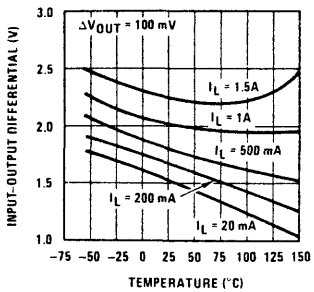
Current Limit



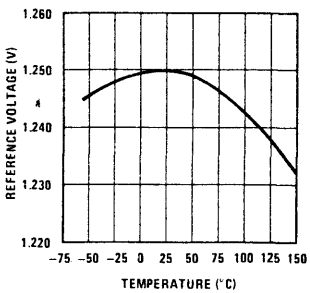
Adjustment Current



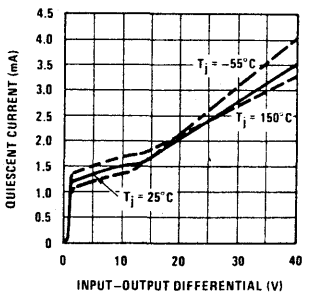
Dropout Voltage



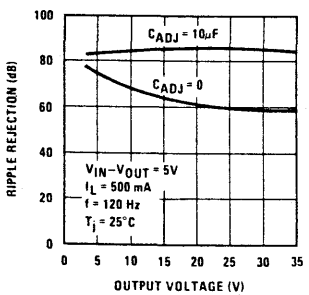
Temperature Stability



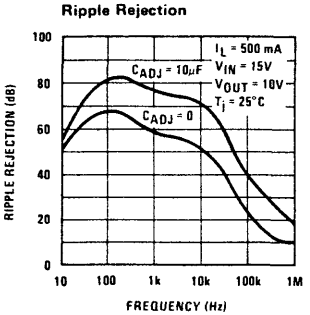
Minimum Operating Current



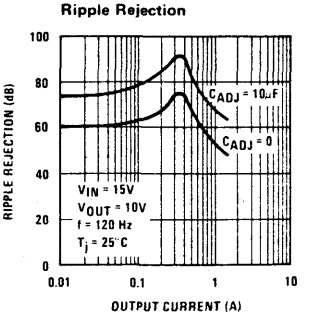
Ripple Rejection



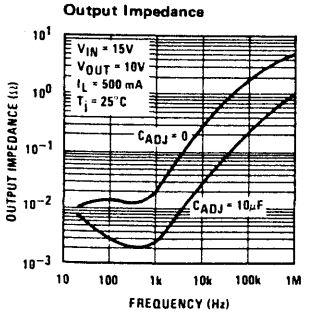
Ripple Rejection



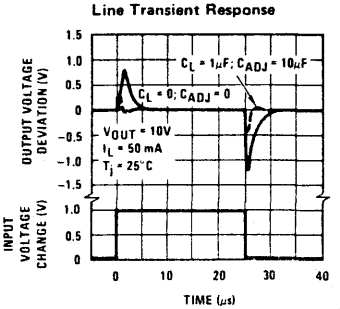
Ripple Rejection



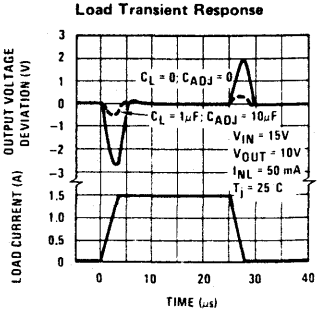
Output Impedance

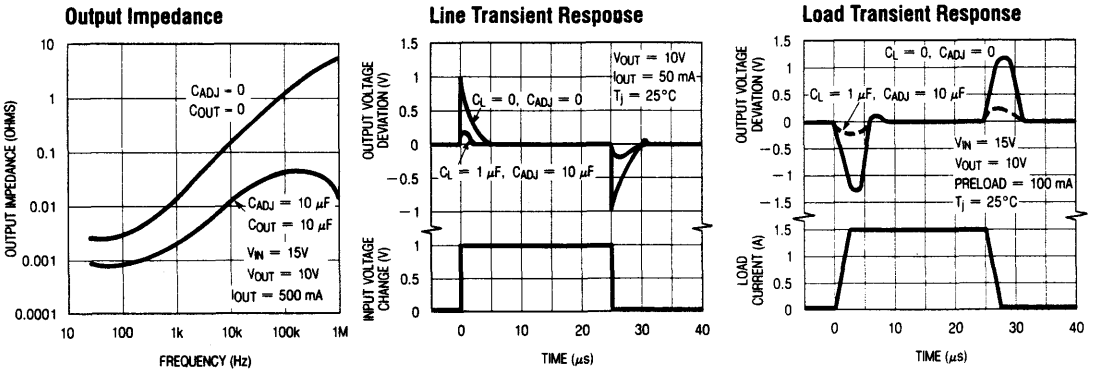


Line Transient Response



Load Transient Response





APPLICATION INFORMATION

GENERAL

The SG117A develops a 1.25V reference voltage between the output and the adjustable terminal (see Figure 1). By placing a resistor, R_1, between these two terminals, a constant current is caused to flow through R_1 and down through R_2 to set the overall output voltage. Normally this current is the specified minimum load current of 5mA or 10mA.

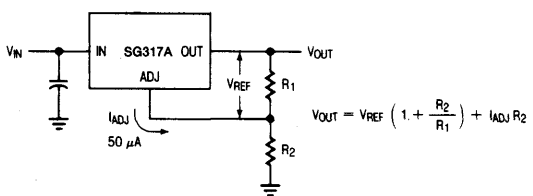


Figure 1

Because I_{ADJ} is very small and constant when compared with the current through R_1, It represents a small error and can usually be ignored.

It is easily seen from the above equation, that even if the resistors were of exact value, the accuracy of the output is limited by the accuracy of V_{REF}. Earlier adjustable regulators had a reference tolerance of ±4%. This tolerance is dangerously close to the ±5% supply tolerance required in many logic and analog systems. Further, many 1% resistors can drift 0.01%/°C adding another 1% to the output voltage tolerance.

For example, using 2% resistors and ±4% tolerance for V_{REF}, calculations will show that the expected range of a 5V regulator design would be $4.66V \leq V_{OUT} \leq 5.36V$ or approximately ±7%. If the same example were used for a 15V regulator, the expected tolerance would be ±8%. With these results most applications require some method of trimming, usually a trim pot. This solution is both expensive and not conducive to volume production.

One of the enhancements of Silicon General's adjustable regulators over existing devices is tightened initial tolerance. This allows relatively inexpensive 1% or 2% film resistors to be used for R_1 and R_2 while setting output voltage within an accepatble tolerance range.

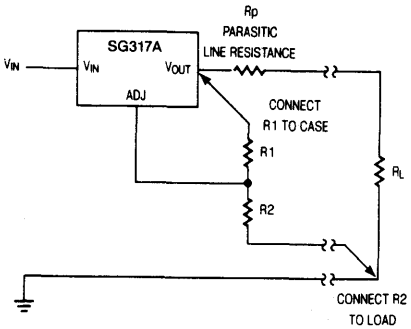
With a guaranteed 1% reference, a 5V power supply design, using ±2% resistors, would have a worse case manufacturing tolerance of ±4%. If 1% resistors were used, the tolerance would drop to ±2.5%. A plot of the worst case output voltage tolerance as a function of resistor tolerance is shown on the front page.

For convenience, a table of standard 1% resistor values is shown below.

Table of ½% and 1% Standard Resistance Values

1.00	1.47	2.15	3.16	4.64	6.81
1.02	1.50	2.21	3.24	4.75	6.98
1.05	1.54	2.26	3.32	4.87	7.15
1.07	1.58	2.32	3.40	4.99	7.32
1.10	1.62	2.37	3.48	5.11	7.50
1.13	1.65	2.43	3.57	5.23	7.68
1.15	1.69	2.49	3.65	5.36	7.87
1.18	1.74	2.55	3.74	5.49	8.06
1.21	1.78	2.61	3.83	5.62	8.25
1.24	1.82	2.67	3.92	5.76	8.45
1.27	1.87	2.74	4.02	5.90	8.66
1.30	1.91	2.80	4.12	6.04	8.87
1.33	1.96	2.87	4.22	6.19	9.09
1.37	2.00	2.94	4.32	6.34	9.31
1.40	2.05	3.01	4.42	6.49	9.53
1.43	2.10	3.09	4.53	6.65	9.76

Standard Resistance Values are obtained from the Decade Table by multiplying by multiples of 10. As an example, 1.21 can represent 1.21Ω, 12.1Ω, 1.21KΩ, etc.

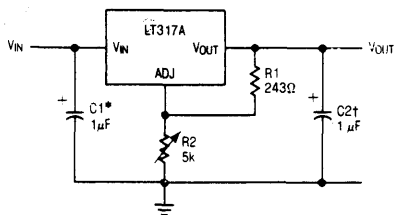


Connections for Best Load Regulation
Figure 2

TYPICAL APPLICATIONS

SG317A

1.2V-25V Adjustable Regulator



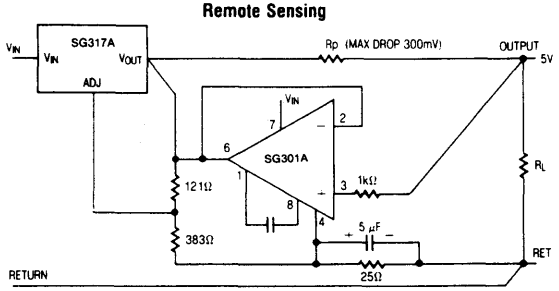
† Optional — improves transient response

* Needed if device is far from filter capacitors

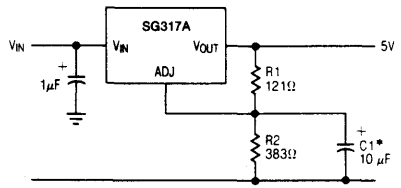
$$V_{OUT} = 1.25V \left(1 + \frac{R2}{R1}\right)$$

Bypass Capacitors: Input bypassing using a 1μF tantalum or 25μF electrolytic is recommended when the input filter capacitors are more than 5 inches from the device. Improved ripple rejection (80 dB) can be accomplished by adding a 10μF capacitor from the adjust pin to ground. For improved AC transient response and to prevent the possibility of oscillation due to unknown reactive load, a 1μF capacitor is also recommended at the output. Because of their low impedance at high frequencies, the best type of capacitor to use is solid tantalum.

Remote Sensing



Improving Ripple Rejection



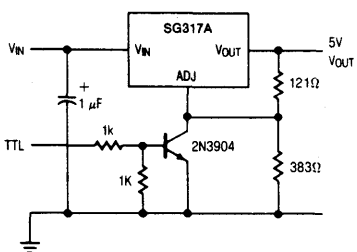
*C1 Improves Ripple Rejection. X_C should be small compared to R2.

Load Regulation: Because the SG117A is a three-terminal device, it is not possible to provide true remote load sensing. Load regulation will be limited by the resistance of the wire connecting the regulator to the load. For the data sheet specification, regulation is measured at the bottom of the package. Negative side sensing is a true Kelvin connection, with the bottom of the output divider returned to the negative side of the load. Although it may not be immediately obvious, best load regulation is obtained when the top of the divider is connected directly to the case, not to the load. This is illustrated in Figure 2. If R_1 were connected to the load, the effective resistance between the regulator and the load would be

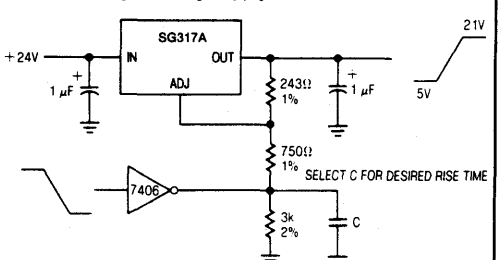
$$R_P \times \left(\frac{R2 + R1}{R1}\right) \quad R_P = \text{Parasitic Line Resistance.}$$

Connected as shown, R_p is not multiplied by the divider ratio. R_p is about 0.004Ω per foot using 16 gauge wire. This translates to 4mV/ft. at 1A load current, so it is important to keep the positive lead between regulator and load as short as possible.

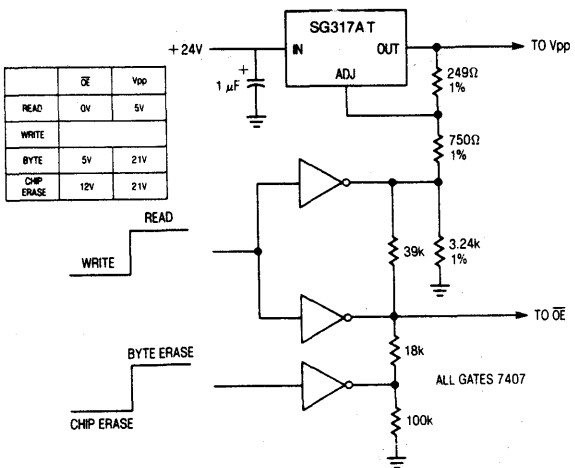
5V Regulator with Shut Down



21V Programming Supply for UV PROM/EEROM

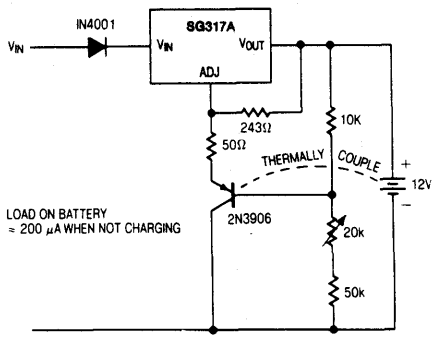


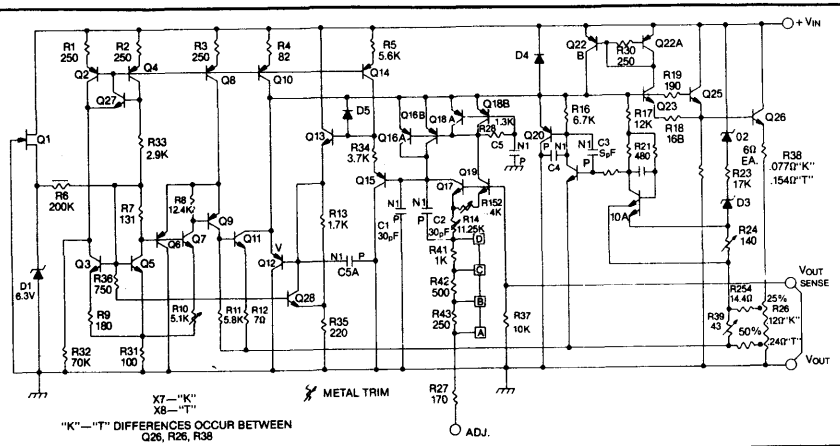
2816 EEPROM Supply Programmer for Read/Write Control



	OE	Vpp
READ	0V	5V
WRITE		
BYTE	5V	21V
CHIP ERASE	12V	21V

Temperature Compensated Lead Acid Battery Charger

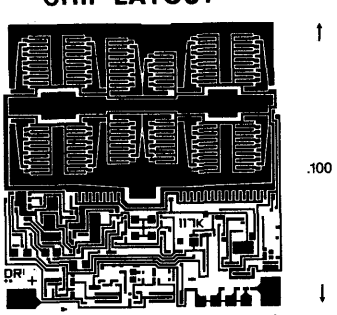




PACKAGE DESCRIPTION

DEVICE	PACKAGE	RATED POWER DISSIPATION	DESIGN LOAD CURRENT
SG117 SG217 SG317	TO-3	20W	1.5A
	TO-39	2W	0.5A
SG317TP	TO-220	15W	1.5A

CHIP LAYOUT



Silicon General
LINEAR INTEGRATED CIRCUITS

SG117HV / SG217HV / SG317HV

1.5-Amp Positive Adjustable Voltage Regulator

DESCRIPTION

The SG117HV / SG217HV / SG317HV positive adjustable regulators will deliver up to 1.5 Amps output current over an output voltage range of 1.2V to 57V. Silicon General has made significant improvements in these regulators compared to previous devices, such as better line and load regulation, and a maximum output voltage error of 1%.

Every effort has been made to make these devices easy to use and difficult to damage. Internal current and power limiting coupled with true thermal limiting prevents device damage due to overloads or shorts, even if the regulator is not fastened to a heat sink.

The SG117HV family of products are ideal complements to the SG137HV adjustable positive regulators.

FEATURES

- **Output Adjustable from 1.2V to 57V**
- **0.01%/V Line Regulation**
- **0.1% Load Regulation**
- **Min. 1.5 Output Current**

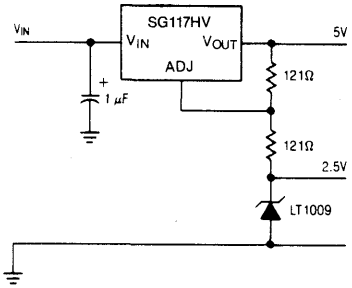
APPLICATIONS

Wide Range Power Supplies

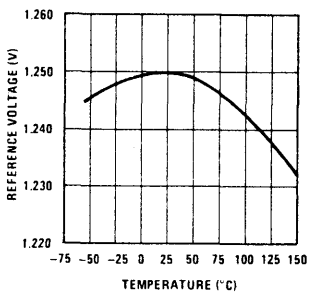
Constant Current Supplies

Voltage Programmable Supplies

Regulator with Reference



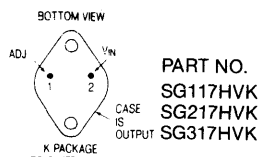
Temperature Stability Curve



ABSOLUTE MAXIMUM RATINGS

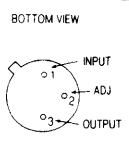
Power Dissipation ..... Internally Limited
Input to Output Voltage Differential 60V
Operating Junction Temperature Range
SG117HV ..... −55°C to 150°C
SG217HV ..... −25°C to 150°C
SG317HV ..... 0°C to 125°C
Storage Temperature Range . −65°C to 150°C
Lead Temperature (Soldering, 10 sec.) .. 300°C

PACKAGE/ORDER INFORMATION



K PACKAGE
TO-3 METAL CAN
(STEEL)

PART NO.
SG117HVK
SG217HVK
SG317HVK



T PACKAGE
TO-39 METAL CAN

PART NO.
SG117HVT
SG217HVT
SG317HVT

ELECTRICAL CHARACTERISTICS (See Note 1)

SYMBOL	PARAMETER	CONDITIONS		SG117HV/SG217HV MIN	SG117HV/SG217HV TYP	SG117HV/SG217HV MAX	SG317HV MIN	SG317HV TYP	SG317HV MAX	UNITS
V_{REF}	Reference Voltage	$3V \le (V_{IN} - V_{OUT}) \le 60V$ $10mA \le I_{OUT} \le I_{MAX}, \le P_{MAX}$	•	1.20	1.25	1.30	1.20	1.25	1.30	V
$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	Line Regulation	$3V \le (V_{IN} - V_{OUT}) \le 60V$			0.01	0.02		0.01	0.04	%/V
		$T_A = 25°C$. (See Note 2)	•		0.02	0.05		0.02	0.07	%/V
$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	Load Regulation	$10mA \le I_{OUT} \le I_{MAX}$ (See Note 2) $V_O \le 5V$			5	15		5	25	mV
		$V_O \ge 5V$			0.1	0.3		0.1	0.5	%
		$V_O \le 5V$	•		20	50		20	70	mV
		$V_O \ge 5V$	•		0.3	1		0.3	1.5	%
	Thermal Regulation	$T_A = 25°C$, 20msec Pulse			0.03	0.07		0.04	0.07	%/W
	Ripple Rejection	$V_O = 10V$, f = 120Hz $C_{ADJ} = 0$	•		65			65		dB
		$C_{ADJ} = 1\mu F$	•	66	80		66	80		dB
I_{ADJ}	Adjust Pin Current		•		50	100		50	100	μA
ΔI_{ADJ}	Adjust Pin Current Change	$10mA \le I_{OUT} \le I_{MAX}$ $2.5V \le (V_{IN} - V_{OUT}) \le 60V$	•		0.2	5		0.2	5	μA
I_{MIN}	Minimum Load Current	$(V_{IN} - V_{OUT}) = 60V$	•		3.5	7		3.5	12	mA
	Current Limit	$(V_{IN} - V_{OUT}) \le 15V$ K Package	•	1.5	2.2		1.5	2.2		A
		T Package	•	0.5	0.8		0.5	0.8		A
		$(V_{IN} - V_{OUT}) = 60V$ K Package	•		0.1			0.1		A
		T Package	•		0.03			0.03		A
$\frac{\Delta V_{OUT}}{\Delta Temp}$	Temperature Stability	$0°C \le T_J \le 125°C$			1			1		%
$\frac{\Delta V_{OUT}}{\Delta Time}$	Long Term Stability	$T_A = 125°C$			0.3	1		0.3	1	%
e_n	RMS Output Noise (% of V_{OUT})	$TA = 25°C$, $10Hz \le f \le 10kHz$			0.003			0.003		%
Θ_{jc}	Thermal Resistance Junction to Case	T Package			12	15		12	15	C/W
		K Package			2.3	3		2.3	3	C/W

The • denotes the specifications which apply over the full operating temperature range.

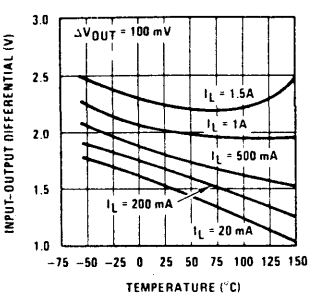
Note 1: Unless otherwise specified, these specifications apply for $V_{IN} - V_{OUT}$, and $I_{OUT} = 0.1A$ for the TO-39 and $I_{OUT} = 0.5A$ for the TO-3 package. Although power dissipation is internally limited, these specifications are applicable for power dissipations of 2W for the TO-39, and 20W for the TO-3. I_{MAX} is 1.5A for the TO-3 package and 0.5A for the TO-39.

Note 2: Regulation is measured at constant junction temperature, using pulse testing with a low duty cycle. Changes in output voltage due to heating effects are covered under the specification for thermal regulation.

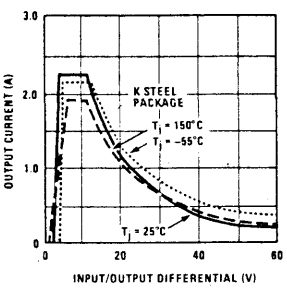
Note 3: Selected devices with tightened reference voltages are available.

TYPICAL PERFORMANCE CHARACTERISTICS

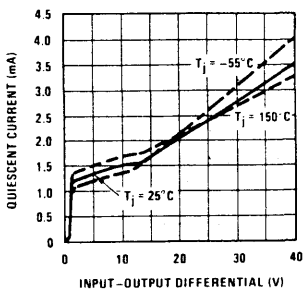
Dropout Voltage



Current Limit



Minimum Operating Current



5 VOLT—3-AMP POSITIVE REGULATOR

DESCRIPTION

The SG123A family is an improved version of the popular LM123 5 Volt, 3 Amp Regulator line. These new devices offer maximum initial output voltage tolerance of 1% and maintain a maximum tolerance of 3% over worst case operating conditions. Line and load regulation are also improved by a factor of 2. These tightened specifications ease design and application problems since safety margins are improved. Also, error budgets in other parts of the system can be expanded, and output voltages at the end of long supply runs can be more accurately calculated.

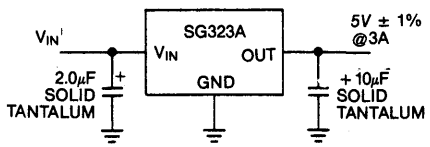
FEATURES

- 1% Initial Tolerance of Output Voltage
- 3 Amp Output Current
- 30 Watt
- Full Internal Overload Protection

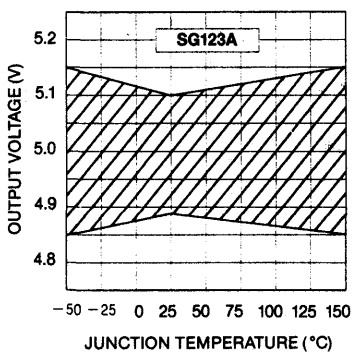
APPLICATIONS

- Local 5V Regulators
- On Card Regulation
- Lab Supplies
- Instrumentation Supplies

Precision 5 Volt Regulator



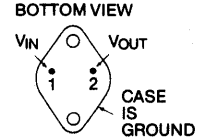
Worst Case Output Voltage



ABSOLUTE MAXIMUM RATINGS

Input Voltage ..... 20 Volts
Power Dissipation ..... Internally Limited
Operating Junction Temperature Range
SG123A / SG123 ..... −55 °C to 150 °C
SG223A / SG223 ..... −25 °C to 150 °C
SG323A / SG323 ..... 0 °C to 125 °C
Storage Temperature Range
SG123A / SG123 ..... −65 °C to 150 °C
SG223A / SG223 ..... −65 °C to 150 °C
SG323A / SG323 ..... −65 °C to 150 °C
Lead Temperature (Soldering, 10 sec.) .. 300 °C

PACKAGE / ORDER INFORMATION



K PACKAGE
TO-3 METAL CAN
(STEEL)

ORDER PART NO.
SG123AK
SG223AK
SG323AK
SG123K
SG223K
SG323K

ELECTRICAL CHARACTERISTICS (See Note 1)

SYMBOL	PARAMETER	CONDITIONS		SG123A/SG223A MIN	SG123A/SG223A TYP	SG123A/SG223A MAX	SG123/SG223 MIN	SG123/SG223 TYP	SG123/SG223 MAX	UNITS
V_{OUT}	Output Voltage	T_J = 25°C, V_{IN} = 7.5V, I_{OUT} = 0		4.95	5.0	5.05	4.7	5.0	5.3	V
		7.5V ≤ V_{IN} ≤ 15V, T_{MIN} ≤ T_J ≤ T_{MAX} 0 ≤ I_{OUT} ≤ 3A, P ≤ 30W	•	4.85	5.0	5.15	4.6		5.4	V
$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	Line Regulation	T_j = 25°C, 7.5V ≤ V_{IN} ≤ 15V (See Note 1)			5	10		5	25	mV
$\frac{\Delta V_{OUT}}{\Delta I_{OUT}}$	Load Regulation	T_J = 25°C, V_{IN} = 7.5V 0 ≤ I_{OUT} ≤ 3A (See Note 1)			25	50		25	100	mV
I_Q	Quiescent Current	7.5V ≤ V_{IN} ≤ 15V, 0 ≤ I_{OUT} ≤ 3A	•		12	20		12	20	mA
e_n	Output Noise Voltage	T_J = 25°C, 10Hz ≤ f ≤ 100kHz			40			40		μV_{rms}
I_{SC}	Short Circuit Current Limit	T_J = 25°C, V_{IN} = 15V V_{IN} = 7.5V			3 4	4.5 6		3 4	4.5 5	A A
	Long Term Stability of Output Voltage					35			35	mV
Θ_{JC}	Thermal Resistance Junction to Case	K Package			1.8	2.5		1.8		°C/W

SYMBOL	PARAMETER	CONDITIONS		SG323A MIN	SG323A TYP	SG323A MAX	SG323 MIN	SG323 TYP	SG323 MAX	UNITS
V_{OUT}	Output Voltage	T_J = 25°C, V_{IN} = 7.5V, I_{OUT} = 0		4.95	5.0	5.05	4.8	5.0	5.2	V
		7.5V ≤ V_{IN} ≤ 15V, T_{MIN} ≤ T_J ≤ T_{MAX} 0 ≤ I_{OUT} ≤ 3A, P ≤ 30W (Note 2)	•	4.85	5.0	5.15	4.75	5.0	5.25	V
$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	Line Regulation	T_j = 25°C, 7.5V ≤ V_{IN} ≤ 15V (See Note 1)			5	10		5	25	mV
$\frac{\Delta V_{OUT}}{\Delta I_{OUT}}$	Load Regulation	T_J = 25°C, V_{IN} = 7.5V 0 ≤ I_{OUT} ≤ 3A (See Note1)			25	50		25	100	mV
I_Q	Quiescent Current	7.5V ≤ V_{IN} ≤ 15V, 0 ≤ I_{OUT} ≤ 3A	•		12	20		12	20	mA
e_n	Output Noise Voltage	T_J = 25°C, 10Hz ≤ f ≤ 100kHz			40			40		μV_{rms}
I_{SC}	Short Circuit Current Limit	T_J = 25°C, V_{IN} = 15V V_{IN} = 7.5V			3 4	4.5 6		3 4	4.5 5	A A
	Long Term Stability of Output Voltage					35			35	mV
Θ_{JC}	Thermal Resistance Junction to Case	K Package			1.8	2.5		1.8		°C/W

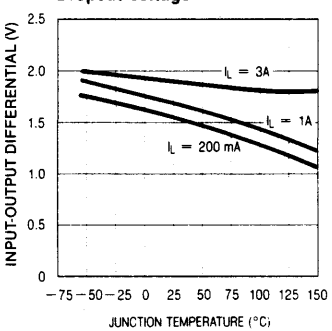
The • denotes the specifications which apply over the full operating temperature range.

Note 1: Load and line regulation are tested with pulsed low duty cycle techniques where pulse width ≤ 1msec and duty cycle ≤ 5%.

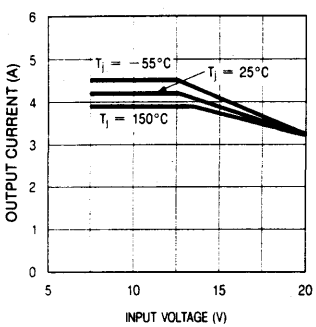
Note 2: T_{min} = −55°C for the SG123A / SG123, −25°C for SG223A / SG223 and 0°C for SG323A / SG323. T_{max} = 150°C for the SG123A / SG123, for SG223A / SG223 and 125°C for SG323A / SG323.

TYPICAL PERFORMANCE CHARACTERISTICS

Dropout Voltage



Peak Available Output Current



1

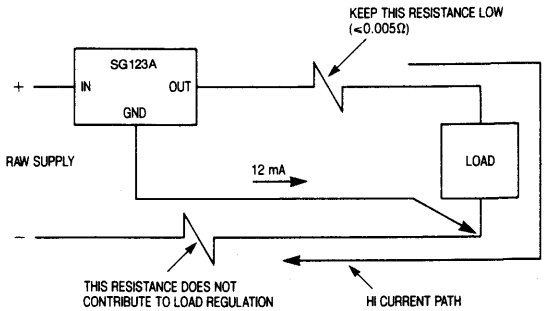
APPLICATIONS INFORMATION

Bypass Capacitors: The SG123A does not require an output capacitor for resistive loads. For almost all applications, however, a 1μF or larger solid tantalum capacitor should be used at the output within 2″ of the regulator to improve the output impedance at high frequencies. For applications where very low high frequency impedance is required, a 10μF solid tantalum output capacitor is recommended. Total output capacitance either local or distributed may be increased without limit.

A 2μF or larger solid tantalum capacitor or a 25μF aluminum capacitor, must be used at the input if the regulator is more than 4″ away from the large rectifier capacitor.

Avoiding Ground Loops: For best regulation, the ground pin of the SG123A should be tied directly to the load point as shown. This prevents excess drop in load voltage caused by load current flowing through the ground return lead. This is essentially a Kelvin connection for the low side of the regulator. A Kelvin connection cannot be made for the high output of regulator because only three pins are available on the package. Therefore, every attempt should be made to minimize the resistance between the output pin of the regulator and the load. #18 gauge hookup wire has a resistance of 0.006 ohms per foot. This translates to 0.36% change in load voltage at full load current. The SG123A is specified at 1% maximum load regulation, so one foot of wire represents a significant loss of regulation. If connectors are used, careful consideration must be given to contact resistance, especially if the connector is subjected to nasty ambients, vibration, or multiple insertions.

Raw Supply: Transformer, diode, and capacitor selection for the raw supply to the SG123A is very important because of the conflicting requirements for reliability, efficiency, and resistance to "brown-out" conditions. High secondary voltage on the transformer will cause unnecessarily high power dissipation in the regulator. Too low a secondary voltage will cause the regulator output to drop out of regulation with only a small reduction in AC mains voltage. The following formula gives a good starting point for transformer selection. This formula assumes a center tapped transformer, using two recifier diodes.



where:

V_{OUT} = 5V

V_{DO} = Minimum input-output differential of the regulator

V_{RECT} = Rectifier forward drop at $3I_{OUT}$

V_{RIP} = ½ p-p capacitor ripple voltage

$$\approx \frac{(5.3 \times 10^{-3})(I_{OUT})}{2C}$$

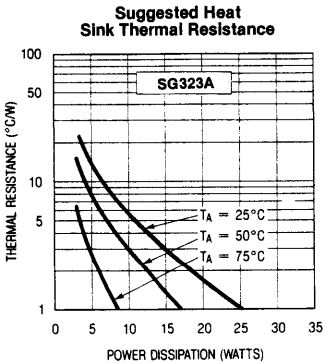
V_{NOM} = Rated line voltage for the transformer (RMS)

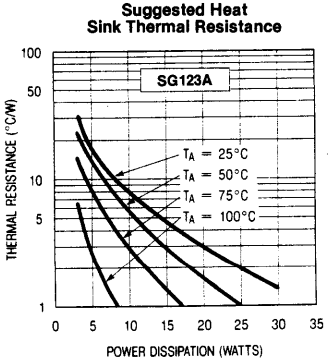
V_{LOW} = Lowest expected line voltage (RMS)

I_{OUT} = DC output current

*1.1 is a nominal load regulation factor for the transformer

TYPICAL PERFORMANCE CHARACTERISTICS





APPLICATIONS INFORMATION

Example: $I_{OUT} = 2.5A$, $V_{OUT} = 5V$
Assume: $V_{DO} = 2.5V$, $V_{RECT} = 1.1V$, $C = 8{,}000\mu F$
$V_{NOM} = 115V$, $V_{LOW} = 0.88V$

$$V_{RIP} = \frac{(5.3 \times 10^{-3})(2.5)}{2(8 \times 10^{-3})} = 0.83V$$

$$V_{RMS} = \left(\frac{5 + 2.5 + 1.1 + 0.83}{\sqrt{2}}\right)\left(\frac{115}{05}\right) \quad (1.1)$$

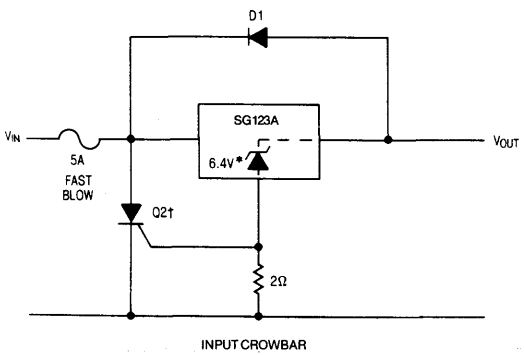
$$= 8.03\ V_{RMS}$$

$$V_{RMS} = \left(\frac{V_{OUT} + V_{DO} + V_{RECT} + V_{RIP)}}{\sqrt{2}}\right)\left(\frac{V_{NOM}}{V_{LOW}}\right) \quad (1.1^*)$$

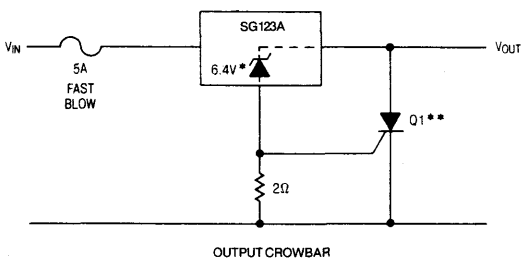
$$I_{RMS} = (I_{OUT})\ (1.2)$$

The filter capacitor should be at least 2000 μF per amp of load current to minimize capacitor heating and ripple voltage. The diodes should be rated at 5-6 amps even though their average current is only 1.5A at full rated load current. The reason for this is that although the average current is 1.5A, the RMS current is typically twice this value. In addition, the diode must withstand very high surge currents during power turn-on. This surge can be 10-20 times the DC rating of the supply, depending on capacitor size and wiring resistance and induction.

TYPICAL APPLICATIONS



INPUT CROWBAR



OUTPUT CROWBAR

† Q2 and D1 must withstand large surge currents until the 5A fuse blows. Peak surge current is limited only by the fuse, wiring, and filter cap resistance.

††Trip point is approximately 7.3V.

* The 6.4V Zener is internal to the SG123A.

**Q1 must be able to withstand continuous currents of 5A if additional system shutdown is not used.

1.5 - AMP NEGATIVE ADJUSTABLE REGULATOR

DESCRIPTION

The SG137A/SG337A negative adjustable regulators will deliver up to 1.5 Amps output current over an output voltage range of – 1.2V to – 37V. Silicon General has made significant improvements in these regulators compared to previous devices, such as better line and load regulation, and a maximum output voltage error of 1%.

Every effort has been made to make these devices easy to use and difficult to damage. Internal current and power limiting coupled with true thermal limiting prevents device damage due to overloads or shorts, even if the regulator is not fastened to a heat sink.

The SG137A family of products are ideal complements to the SG117A adjustable positive regulators.

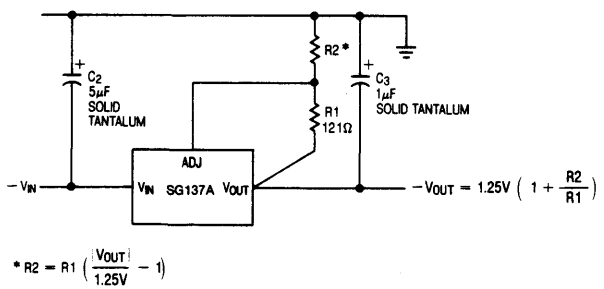
FEATURES

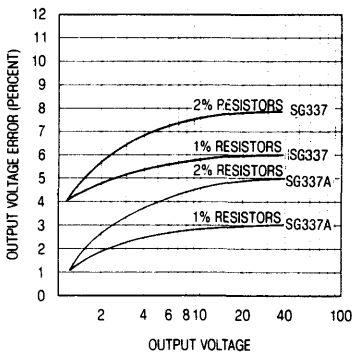
- **– 1% initial voltage tolerance**
- **– 0.01%Iv line regulation**
- **– 0.5% load regulation**
- **– 0.02% Iw thermal regulation**

APPLICATIONS

- Adjustable Power Supplies
- System Power Supplies
- Precision Voltage/Current Regulators
- On-Card Regulators

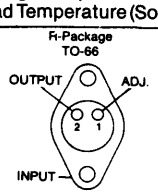
Negative Regulator



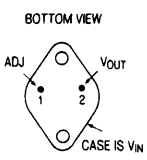


ABSOLUTE MAXIMUM RATINGS

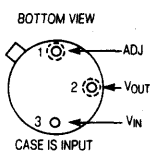
Power Dissipation ..... Internally Limited
Input to Output Voltage Differential 40V
Operating Junction Temperature Range
SG137A/SG137 ..... – 55 °C to 150 °C
SG237A/SG237 ..... – 25 °C to 150 °C
SG337A/SG337 ..... 0 °C to 125 °C
Storage Temperature Range ..... – 65 °C to 150 °C
Lead Temperature (Soldering, 10 sec.) ..... 300 °C



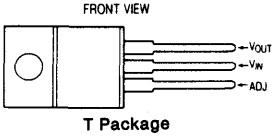
PART NO.
SG137AR
SG137R
SG237AR
SG237R
SG337AR
SG337R



PART NO.
SG137AK
SG137K
SG237AK
SG237K
SG337AK
SG337K



PART NO.
SG137AT
SG137T
SG237AT
SG237T
SG337AT
SG337T



PART NO.
SG337AP
SG337P

ELECTRICAL CHARACTERISTICS (See Note 1)

SYMBOL	PARAMETER	CONDITIONS		SG137A/SG237A MIN	SG137A/SG237A TYP	SG137A/SG237A MAX	SG137/SG237 MIN	SG137/SG237 TYP	SG137/SG237 MAX	UNITS
V_{REF}	Reference Voltage	$\lvert V_{IN} - V_{OUT} \rvert$ = 5V, I_{OUT} = 10mA, T_j = 25°C		−1.238	−1.250	−1.262	−1.225	−1.250	−1.275	V
		3V ≤ $\lvert V_{IN} - V_{OUT} \rvert$ ≤40V 10mA≤I_{OUT} ≤ I_{MAX} P ≤P_{MAX}	•	−1.220	−1.250	−1.280	−1.200	−1.250	−1.300	V
$\frac{\Delta I_{OUT}}{\Delta I_{OUT}}$	Load Regulation	10mA≤I_{OUT} ≤ I_{MAX} (See Note 2 & 3) T_j = 25°C, $\lvert V_{OUT} \rvert$ ≤ 5V T_j = 25°C, $\lvert V_{OUT} \rvert$ ≤ 5V $\lvert V_{OUT} \rvert$ ≤ 5V $\lvert V_{OUT} \rvert$ ≤ 5V			5 0.1 10 0.2	25 0.5 50 1.0		15 0.3 20 0.3	25 0.5 50 1.0	mV % mV %
$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	Line Regulation	3V ≥ $\lvert V_{IN} - V_{OUT} \rvert$ ≤ 40V, (See Note 2)-I_{OUT} ≤ I_{MAX} (See Note 2 & 3) T_j = 25°C			0.005	0.01		0.01	0.02	%/V
	Ripple Rejection	V_{OUT} = −10V, f = 120hZ C_{ADJ} = 0 C_{ADJ} = 10μF	• •	60 70	66 80		66	60 77		dB dB
	Thermal Regulation	T_j = 25°C, 10msec Pulse			0.002	0.02		0.002	0.02	%/W
I_{ADJ}	Adjust Pin Current				65	100		65	100	μA
ΔI_{ADJ}	Adjust Pin Current Change	10mA ≤ I_{OUT} ≤ I_{MAX} 3V ≤ $\lvert V_{IN} - V_{OUT} \rvert$ ≤ 40V	•		0.2 1.0	2 5		0.5 2	5 5	μA μA
	Minimum Load Current	$\lvert V_{IN} - V_{OUT} \rvert$ ≤ 40V $\lvert V_{IN} - V_{OUT} \rvert$ ≤ 10V	• •		2.5 1.2	5 3		2.5 1.2	5.0 3.0	mA mA
I_{SC}	Current Limit	$\lvert V_{IN} - V_{OUT} \rvert$ ≤ 15V, K and P Package T Package $\lvert V_{IN} - V_{OUT} \rvert$ ≤ 40V, K and P Package T_j = 25°C T Package	• •	1.5 0.5 0.24 0.15	2.2 0.8 0.4 0.25	3.2 1.5 1.0 0.5	1.5 0.5 0.24 0.15	2.2 0.8 0.4 0.25		A A A A
$\frac{\Delta V_{OUT}}{\Delta V_{Temp}}$	Temperature Stability				0.6	1.5		0.6		%
$\frac{\Delta V_{OUT}}{\Delta V_{Time}}$	Long Term Stability	T_A = 125°C, 1000 Hours			0.3	1.0		0.3	1.0	%
e_n	RMS Output Noise (% of V_{OUT})	T_A = 25°C, 10 Hz ≤ f ≤ 10kHz			0.003			0.003		%
θ_{JC}	Thermal Resistance Junction to Case	T Package K Package			12 2.3	15 3.0		12 2.3	15 3.0	°C/W °C/W

SYMBOL	PARAMETER	CONDITIONS		SG337A MIN	SG337A TYP	SG337A MAX	SG337 MIN	SG337 TYP	SG337 MAX	UNITS
V_{REF}	Reference Voltage	$\lvert V_{IN} - V_{OUT} \rvert$ = 5V, I_{OUT} = 10mA, T_j = 25°C		−1.238	−1.250	−1.262	−1.213	−1.250	−1.287	V
		3V ≤ $\lvert V_{IN} - V_{OUT} \rvert$ ≤40V 10mA≤I_{OUT} ≤ I_{MAX} P ≤P_{MAX}	•	−1.220	−1.250	−1.280	−1.200	−1.250	−1.300	V
$\frac{\Delta I_{OUT}}{\Delta I_{OUT}}$	Load Regulation	10mA≤I_{OUT} ≤ I_{MAX} (See Note 2 & 3) T_j = 25°C, $\lvert V_{OUT} \rvert$ ≤ 5V T_j = 25°C, $\lvert V_{OUT} \rvert$ ≤ 5V $\lvert V_{OUT} \rvert$ ≤ 5V $\lvert V_{OUT} \rvert$ ≤ 5V			5 0.1 10 0.2	25 0.5 50 1.0		15 0.3 20 0.3	50 1.0 70 1.5	mV % mV %
$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	Line Regulation	3V ≥ $\lvert V_{IN} - V_{OUT} \rvert$ ≤ 40V, (See Note 2)-I_{OUT} ≤ I_{MAX} (See Note 2 & 3) T_j = 25°C			0.005	0.01		0.01	0.04	%/V
	Ripple Rejection	V_{OUT} = −10V, f = 120hZ C_{ADJ} = 0 C_{ADJ} = 10μF	• •	60 70	66 80		66	60 77		dB dB
	Thermal Regulation	T_j = 25°C, 10msec Pulse			0.002	0.02		0.003	0.04	%/W
I_{ADJ}	Adjust Pin Current				65	100		65	100	μA
ΔI_{ADJ}	Adjust Pin Current Change	10mA ≤ I_{OUT} ≤ I_{MAX} 3V ≤ $\lvert V_{IN} - V_{OUT} \rvert$ ≤ 40V	•		0.2 1.0	2 5		0.5 2	5 5	μA μA
	Minimum Load Current	$\lvert V_{IN} - V_{OUT} \rvert$ ≤ 40V $\lvert V_{IN} - V_{OUT} \rvert$ ≤ 10V	• •		2.5 1.2	5 3		2.5 1	10 6	mA mA
I_{SC}	Current Limit	$\lvert V_{IN} - V_{OUT} \rvert$ ≤ 15V, K and P Package T Package $\lvert V_{IN} - V_{OUT} \rvert$ ≤ 40V, K and P Package T_j = 25°C T Package	• •	1.5 0.5 0.24 0.15	2.2 0.8 0.5 0.25	3.5 1.5 1.0 0.5	1.5 0.5 0.15 0.10	2.2 0.8 0.4 0.17		A A A A
$\frac{\Delta V_{OUT}}{\Delta V_{Temp}}$	Temperature Stability				0.6	1.5		0.6		%
$\frac{\Delta V_{OUT}}{\Delta V_{Time}}$	Long Term Stability	T_A = 125°C, 1000 Hours			0.3	1.0		0.3	1.0	%
e_n	RMS Output Noise (% of V_{OUT})	T_A = 25°C, 10 Hz ≤ f ≤ 10kHz			0.003			0.003		%
θ_{JC}	Thermal Resistance Junction to Case	T Package K Package P Package			12 2.3 4	15 3.0 5		12 2.3 4	15 3.0	°C/W °C/W °C/W

The • denotes the specifications which apply over the full operating temperature range.

Note 1: Unless otherwise indicated, these specifications apply: $\lvert V_{IN} - V_{OUT} \rvert$ = 5V; and I_{OUT} = 0.1A for the T package, I_{OUT} = 0.5A for the K and P packages. Power dissipation up to 2W for the T package and 20W for the K and P packages. I_{MAX} = 1.5A for the K and P packages, and 0.5 for the T package.

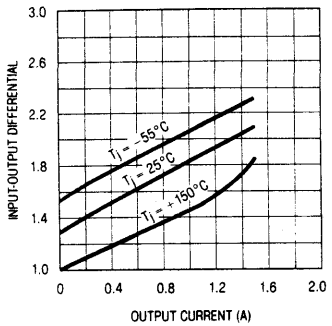
Note 2: Testing is done using a pulsed low duty cycle technique. See thermal regulation specifications for output changes due to heating effects. Load regulation is measured on the output pin at a point ⅛" below the base of the K and T package and at the junction of the wide and narrow portion of the lead on the P package.

Note 3: Load Regulation for the SG337AP is the same as for SG337P.

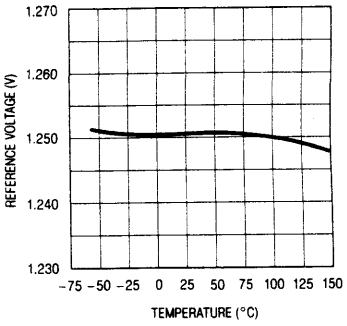
1

TYPICAL PERFORMANCE CHARACTERISTICS

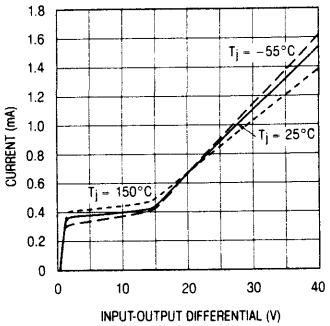
Dropout Voltage



Temperature Stability

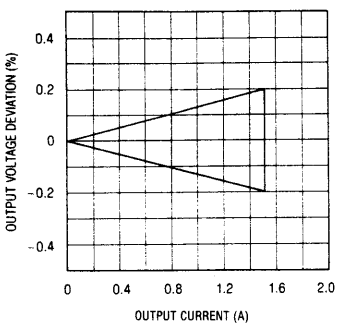


Minimum Load Current



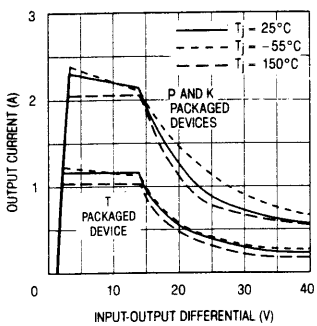
TYPICAL PERFORMANCE CHARACTERISTICS

Load Regulation*

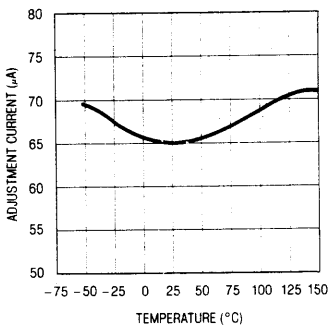


*The SG137A has load regulation compensation which makes the typical unit read close to zero. This band represents the typical production spread.

Current Limit



Adjustment Current



APPLICATION INFORMATION

Output Voltage: The output voltage is determined by two external resistors, R_1 & R_2 (see Figure 1). The exact formula for the output voltage is:

$$V_{OUT} = V_{Ref}\left(1 + \frac{R_2}{R_1}\right) + I_{ADJ}(R_2)$$

Where: V_{Ref} = Reference Voltage, I_{ADJ} = Adjustment Pin Current. In most applications, the second term is small enough to be ignored, typically about 0.5% of V_{OUT}. In more critical applications, the exact formula should be used, with I_{ADJ} equal to 65μa. Solving for R_2 yields:

$$R_2 = \frac{V_{OUT} - V_{Ref}}{\frac{V_{Ref}}{R_1} - I_{ADJ}}$$

Smaller values of R_1 and R_2 will reduce the influence of I_{ADJ} on the output voltage, but the no-load currrent drain on the regulator will be increased. Typical values for R_1 are between 100Ω and 300Ω, giving 12.5 mA and 4.2mA no-load current respectively. There is an additional consideration in selecting R_1, the minimum load current specification of the regulator.

The operating current of the SG137A flows from input to output. If this current is not absorbed by the load, the output of the regulator will rise above the regulated value. The current drawn by R_1 and R_2 is normally high enough to absorb the current, but care must be taken in no-load situations where R_1 and R_2 have high values. The maximum value for the operating current, which must be absorbed, is 5mA for the SG137A. If input-output voltage differential is less than 10V, the operating current that must be absorbed drops to 3mA.

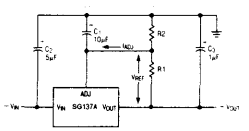


Figure 1

EXAMPLES:

1. A precision 10V regulator to supply up to 1Amp load current.
   a. Select R_1 = 100Ω to minimize effect of I_{ADJ}
   b. Calculate $R_2 = \frac{V_{OUT} - V_{Ref}}{\frac{V_{Ref}}{R_1} - I_{ADJ}} = \frac{10V - 1.25V}{\frac{1.25V}{100\Omega} - 65\mu A} = 704\Omega$
2. A 15V regulator to run off batteries and supply 50mA. V_{IN} MAX = 25V
   a. To minimize battery drain, select R_1 as high as possible

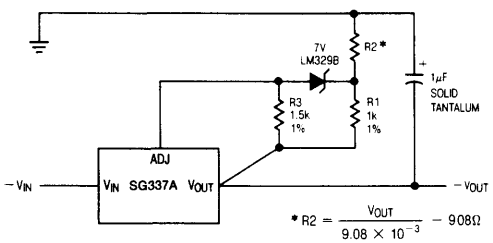
$$R_1 = \frac{1.25V}{3mA} = 417\Omega, \text{ use } 404\Omega, 1\%$$

TYPICAL APPLICATION

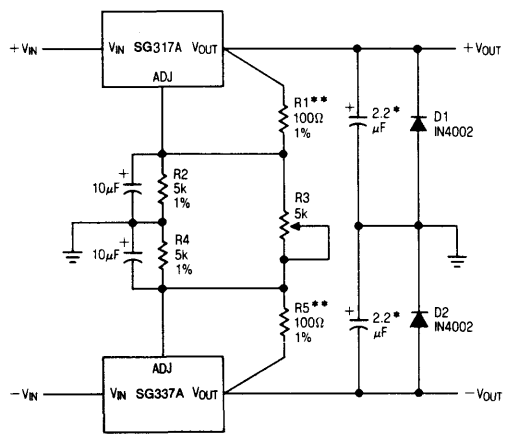
the output stability, load regulation, line regulation, thermal regulation, temperature drift, long term drift, and noise, can be improved by a factor of 6.6 over the standard regulator configuration. This assumes a zener whose drift and noise is considerably better than the regulator itself. The LM329B has 20 PPM/°C maximum drift and about 10 times lower noise than the regulator.

In the application shown below, regulators #2 to "N" will track regulator #1 to within ±24mV initially, and to ±60mV over all load, line, and temperature conditions. If any regulator output is shorted to ground, all other outputs will drop to −2V. Load regulation of regulators 2 to "N" will be improved by V_{OUT}1.5V compared to a standard regulator, so regulator #1 should be the one which has the lowest load current.

High Stability Regulator



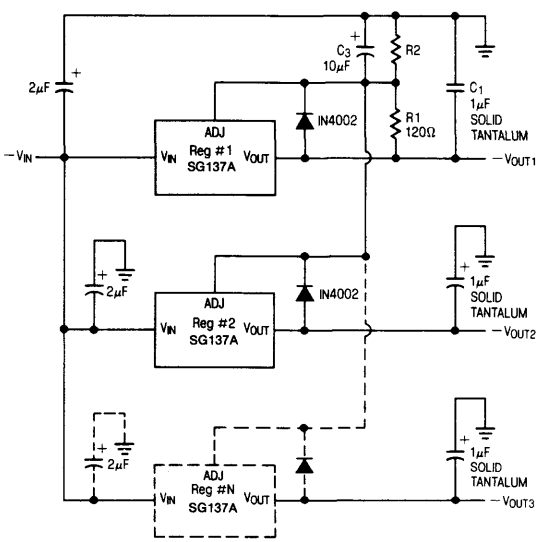
Dual Tracking Supply ±1.25V to ±20V



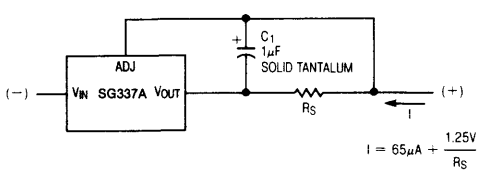
* Solid Tantalum

** R_1 or R_5 may be trimmed slightly to improve tracking

Multiple Tracking Regulators



Current Regulator



Silicon General
LINEAR INTEGRATED CIRCUITS

SG137HV/SG237HV/SG337HV

1.5 - AMP NEGATIVE ADJUSTABLE REGULATOR

DESCRIPTION

The SG137HV/SG237HV/SG337HV negative adjustable regulators will deliver up to 1.5 Amps output current over an output voltage range of −1.2V to −47V. Silicon General has made significant improvements in these regulators compared to previous devices, such as better line and load regulation, and a maximum output voltage error of 1%.

Every effort has been made to make these devices easy to use and difficult to damage. Internal current and power limiting coupled with true thermal limiting prevents device damage due to overloads or shorts, even if the regulator is not fastened to a heat sink.

The SG137HV family of products are ideal complements to the SG117HV adjustable positive regulators.

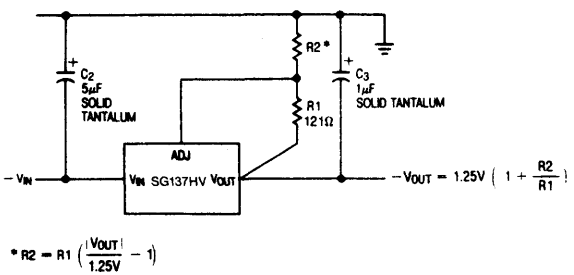
FEATURES

- **Output adjustable from −1.2V to −47V**
- **0.01%/V line regulation**
- **0.5% load regulation**
- **0.002% thermal regulation**

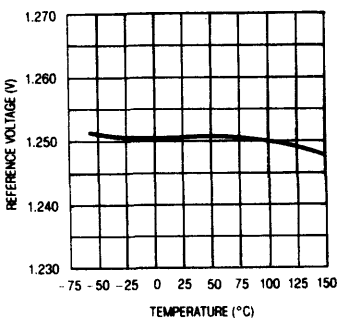
APPLICATIONS

- **Adjustable Power Supplies**
- **System Power Supplies**
- **Precision Voltage/Current Regulators**
- **On-Card Regulators**

NEGATIVE REGULATOR



TEMPERATURE STABILITY CURVE



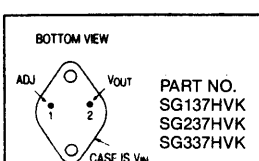
ABSOLUTE MAXIMUM RATINGS

Power Dissipation ..... Internally Limited
Input to Output Voltage Differential 50V
Operating Junction Temperature Range

SG137HV ..... −55°C to 150°C
SG237HV ..... −25°C to 150°C
SG337HV ..... 0°C to 125°C

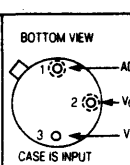
Storage Temperature Range .. −65°C to 150°C
Lead Temperature (Soldering, 10 sec.) .. 300°C

PACKAGE ORDER INFORMATION



K PACKAGE

PART NO.
SG137HVK
SG237HVK
SG337HVK



T Package

PART NO.
137HVT
237HVT
337HVT

ELECTRICAL CHARACTERISTICS (See Note 1)

SYMBOL	PARAMETER	CONDITIONS		SG137HV/SG237HV MIN	SG137HV/SG237HV TYP	SG137HV/SG237HV MAX	SG337HV MIN	SG337HV TYP	SG337HV MAX	UNITS
V_{REF}	Reference Voltage	$\lvert V_{IN} - V_{OUT}\rvert$ = 5V. I_{OUT} = 10mA, T_J = 25°C (Note 3)		−1.225	−1.250	−1.275	−1.213	−1.250	−1.287	V
		3V ≤ $\lvert V_{IN} - V_{OUT}\rvert$ ≤ 50V 10mA ≤ I_{OUT} ≤ I_{MAX} P ≤ P_{MAX}	•	−1.200	−1.250	−1.300	−1.200	−1.250	−1.300	V
$\frac{\Delta V_{OUT}}{\Delta I_{OUT}}$	Load Regulation	10mA ≤ I_{OUT} ≤ I_{MAX} (See Note 2) $\lvert V_{OUT}\rvert$ ≤ 5V $\lvert V_{OUT}\rvert$ ≥ 5V	 •		20 0.3	50 1.0		20 0.3	70 1.5	mV %
$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	Line Regulation	3V ≤ $\lvert V_{IN} - V_{OUT}\rvert$ ≤ 50V (See Note 2)	•		0.02	0.05		0.02	0.07	%/V
	Ripple Rejection	V_{OUT} = −10V, f = 120Hz C_{ADJ} = 0 C_{ADJ} = 10μF	 • •	 66	60 77		 66	60 77		 dB dB
	Thermal Regulation	T_J = 25°C, 10msec Pulse			0.002	0.02		0.003	0.04	%/W
I_{ADJ}	Adjust Pin Current		•		65	100		65	100	μA
ΔI_{ADJ}	Adjust Pin Current Change	10mA ≤ I_{OUT} ≤ I_{MAX} T_A = 25°C 2.5V ≤ $\lvert V_{IN} - V_{OUT}\rvert$ ≤ 50V			2 3	5 6		2 3	5 6	μA μA
	Minimum Load Current	$\lvert V_{IN} - V_{OUT}\rvert$ ≤ 50V $\lvert V_{IN} - V_{OUT}\rvert$ ≤ 10V	• •		2.5 1.2	5 3		2.5 1.5	10 6	mA mA
I_{SC}	Current Limit	$\lvert V_{IN} - V_{OUT}\rvert$ ≤ 13V K Package T Package $\lvert V_{IN} - V_{OUT}\rvert$ ≤ 50V K Package T Package T_J = 25°C	 • • • 	1.5 0.5 0.2 0.1	2.2 0.8 0.4 0.17	3.2 1.6 0.8 0.5	1.5 0.5 0.1 0.05	2.2 0.8 0.4 0.17	3.5 1.8 0.8 0.5	A A A A
$\frac{\Delta V_{OUT}}{\Delta V_{TEMP}}$	Temperature Stability				0.6	1.5		0.6		%
$\frac{\Delta V_{OUT}}{\Delta V_{TIME}}$	Long Term Stability	T_A = 125°C, 1000 Hours			0.3	1.0		0.3	1.0	%
e_n	RMS Output Noise (% of V_{OUT})	T_A = 25°C, 10Hz ≤ f ≥ 10kHz			0.003			0.003		%
θ_{JC}	Thermal Resistance Junction to Case	T Package K Package			12 2.3	15 3.0		12 2.3	15 3.0	°C/W °C/W

The • denotes the specifications which apply over the full operating temperature range.

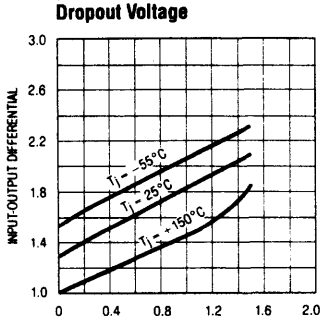
Note 1: Unless otherwise indicated, these specifications apply: $\lvert V_{IN} - V_{OUT}\rvert$ = 5V; and I_{OUT} = 0.1A for the T package, I_{OUT} = 0.5A for the K package. Power dissipation up to 2W for the T package and 20W for the K package. I_{MAX} = 1.5A for the K package and 0.5 for the T package.

Note 2: Testing is done using a pulsed low duty cycle technique. See thermal regulation specifications for output changes due to heating effects. Load regulation is measured on the output pin at a point 1/8-" below the base of the K and T package.

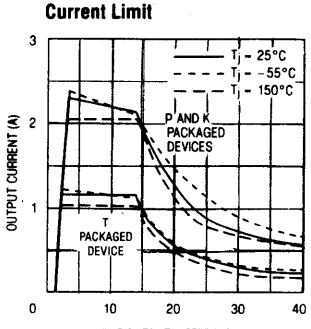
Note 3: Selected devices with tightened reference voltages available.

TYPICAL PERFORMANCE CHARACTERISTICS

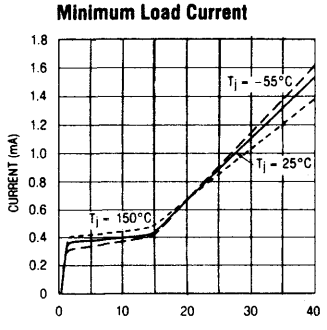
Dropout Voltage



Current Limit



Minimum Load Current



5 AMP POSITIVE ADJUSTABLE VOLTAGE REGULATOR

DESCRIPTION

The SG138A series of adjustable regulators provide 5 amps output current over an output voltage range of 1.2 volts to 32 volts. The internal voltage reference is trimmed to less than 1%, enabling a very tight output voltage. In addition to excellent line and load regulation, with full overload protection, the SG138A incorporates new current limiting circuitry allowing large transient load currents to be handled for short periods. Transient load currents of up to 12 amps can be supplied without limiting, eliminating the need for a large output capacitor.

The SG138A is an improved version of the popular LM138 with improved circuit design and advanced process techniques to provide superior performance and reliability.

The graph below shows the significant improvement in output voltage tolerance achieved by using the SG138A or SG338A.

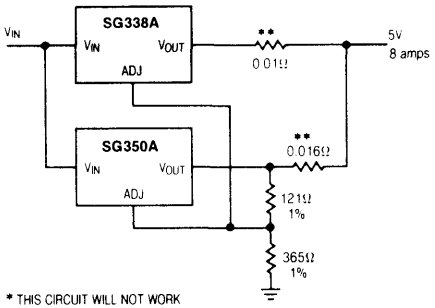
FEATURES

- 1% Initial Tolerance
- 0.3% Load Regulation
- 5 Amp output Current
- 12 Amp Transient Output Current

APPLICATIONS

- High Power Linear Regulator
- Battery Chargers
- Power Driver
- Constant Current Regulator

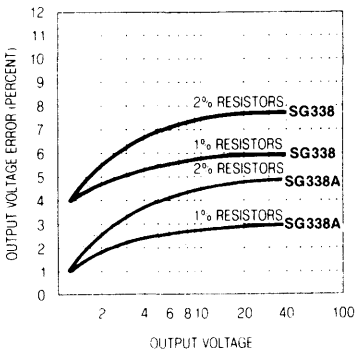
***Parallel Regulators for Higher Current**



* THIS CIRCUIT WILL NOT WORK WITH LM VERSION DEVICES

** CURRENT SHARING RESISTORS DEGRADE REGULATION TO 1%

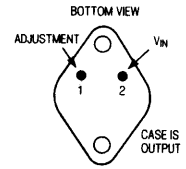
Output Voltage Error



ABSOLUTE MAXIMUM RATINGS

Power Dissipation ..... Internally Limited
Input to output Voltage Differential 35V
Operating Junction Temperature Range
SG138A/138 ..... – 55°C to 150°C
SG238A/238 ..... – 25°C to 150°C
SG338A/338 ..... 0°C to 125°C
Storage Temperature Range ..... – 65°C to 150°C
Lead Temperature (Soldering, 10 sec.) ..... 300°C

PACKAGE/ORDER INFORMATION



K PACKAGE
TO-3 METAL CAN
(STEEL)

ORDER PART NUMBER
SG138AK
SG238AK
SG338AK
SG138K
SG238K
SG338K

ELECTRICAL CHARACTERISTICS (See Note 1)

SYMBOL	PARAMETER	CONDITIONS		SG138A/SG238A MIN	SG138A/SG238A TYP	SG138A/SG238A MAX	SG138/SG238 MIN	SG138/SG238 TYP	SG138/SG238 MAX	UNITS
V_{REF}	Reference Voltage	I_{OUT} = 10mA T_A = 25°C		1.238	1.250	1.262				V
		3V ≤ (V_{IN} – V_{OUT}) ≤ 35V 10mA ≤ I_{OUT} ≤ 5A, P ≤ 50W	●	1.225	1.250	1.270	1.19	1.24	1.29	V
$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	Line Regulation	3V ≤ (V_{IN} – V_{OUT}) ≤ 35V, (See Note 2) T_A = 25°C								
					0.005	0.01		0.005	0.01	%/V
			●		0.02	0.04		0.02	0.04	%/V
$\frac{\Delta V_{OUT}}{\Delta I_{OUT}}$	Load Regulation	10mA ≤ I_{OUT} ≤ 5A, (See Note 2) T_A = 25°C								
		V_{OUT} ≤ 5V			5	15		5	15	mV
		V_{OUT} ≥ 5V			0.1	0.3		0.1	0.3	%
		V_{OUT} ≤ 5V	●		20	30		20	30	mV
		V_{OUT} ≥ 5V	●		0.3	0.6		0.3	0.6	%
	Thermal Regulation	T_A = 25°C, 20msec Pulse			0.002	.01		0.002	0.01	%/W
	Ripple Rejection	V_{OUT} = 10V, f = 120Hz C_{ADJ} = 0	●		60			60		dB
		C_{ADJ} = 10μF	●	60	75		60	75		dB
I_{ADJ}	Adjust Pin Current		●		45	100		45	100	μA
ΔI_{ADJ}	Adjust Pin Current Change	10mA ≤ I_{OUT} ≤ 5A, 3V ≤ (V_{IN} – V_{OUT}) ≤ 35V	●		0.2	5		0.2	5	μA
	Minimum Load Current	(V_{IN} – V_{OUT}) = 35V	●		3.5	5		3.5	5	mA
I_{SC}	Current Limit	(V_{IN} – V_{OUT}) ≤ 10V DC	●	5	8		5	8		A
		0.5ms peak	●	7	12		7	12		A
		(V_{IN} – V_{OUT}) = 30V, T_j = 25°C			1			1		A
$\frac{\Delta V_{OUT}}{\Delta Temp}$	Temperature Stability		●		1	2		1		%
$\frac{\Delta V_{OUT}}{\Delta Time}$	Long Term Stability	T_A = 125°C, 1000 Hours			0.3	1		0.3	1	%
e_n	RMS Output Noise (% of V_{OUT})	T_A = 25°C, 10Hz ≤ f ≤ 10kHz			0.001			0.003		%
Θ_{JC}	Thermal Resistance Junction to Case	K Package				1			1	°C/W

ELECTRICAL CHARACTERISTICS (See Note 1)

SYMBOL	PARAMETER	CONDITIONS		SG338A MIN	SG338A TYP	SG338A MAX	SG338 MIN	SG338 TYP	SG338 MAX	UNITS
V_{REF}	Reference Voltage	I_{OUT} = 10mA T_j = 25°C		1.238	1.250	1.262				V
		3V ≤ (V_{IN} − V_{OUT}) ≤ 35V 10mA ≤ I_{OUT} ≤ 5A, P ≤ 50W	●	1.225	1.250	1.270	1.19	1.24	1.29	V
$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	Line Regulation	3V ≤ (V_{IN} − V_{OUT}) ≤ 35V, (See Note 2) T_A = 25°C			0.005	0.01		0.005	0.03	%/V
			●		0.02	0.04		0.02	0.06	%/V
$\frac{\Delta V_{OUT}}{\Delta I_{OUT}}$	Load Regulation	10mA ≤ I_{OUT} ≤ 5A, (See Note 2) T_A = 25°C V_{OUT} ≤ 5V			5	15		5	25	mV
		V_{OUT} ≥ 5V			0.1	0.3		0.1	0.5	%
		V_{OUT} ≤ 5V	●		20	30		20	50	mV
		V_{OUT} ≥ 5V	●		0.3	0.6		0.3	1	%
	Thermal Regulation	T_A = 25°C, 20msec pulse			0.002	.02		0.002	0.02	%/W
	Ripple Rejection	V_{OUT} = 10V, f = 120Hz C_{ADJ} = 0	●		60			60		dB
		C_{ADJ} = 10μF	●	60	75		60	75		dB
I_{ADJ}	Adjust Pin Current		●		45	100		45	100	μA
ΔI_{ADJ}	Adjust Pin Current Change	10mA ≤ I_{OUT} ≤ 5A, 3V ≤ (V_{IN}−V_{OUT}) ≤ 35V	●		0.2	5		0.2	5	μA
	Minimum Load Current	(V_{IN} − V_{OUT}) = 35V	●		3.5	10		3.5	10	mA
I_{SC}	Current Limit	(V_{IN} − V_{OUT}) ≤ 10V DC	●	5	8		5	8		A
		0.5ms peak	●	7	12		7	12		A
		(V_{IN} − V_{OUT}) = 30V, T_j = 25°C			1	2		1		A
$\frac{\Delta V_{OUT}}{\Delta Temp}$	Temperature Stability		●		1	2		1		%
$\frac{\Delta V_{OUT}}{\Delta Time}$	Long Term Stability	T_A = 125°C, 1000 Hours			0.3	1		0.3	1	%
e_n	RMS Output Noise (% of V_{OUT})	T_A = 25°C, 10Hz ≤ f ≤ 10kHz			0.001			0.003		%
Θ_{JC}	Thermal Resistance Junction to Case	K Package				1			1	°C/W

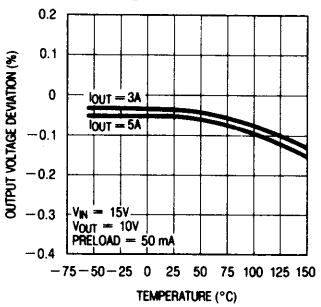
The ● denotes the specifications which apply over the full operating temperature range.

Note 1: Unless otherwise specified, these specifications apply: V_{IN} − V_{OUT} = 5V and I_{OUT} = 2.5A. These specifications are applicable for power dissipations up to 50W.

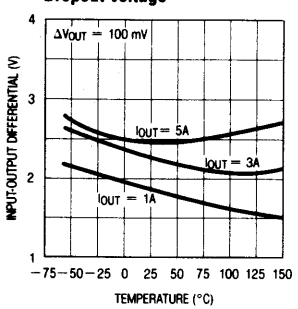
Note 2: See thermal regulation specifications for changes in output voltage due to heating effects. Load and line regulation are measured at a constant junction temperature by low duty cycle pulse testing.

TYPICAL PERFORMANCE CHARACTERISTICS

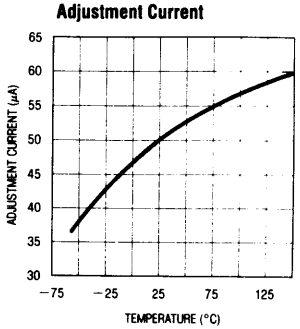
Load Regulation



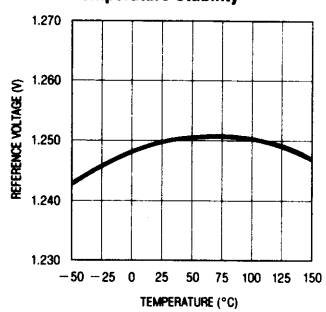
Dropout Voltage



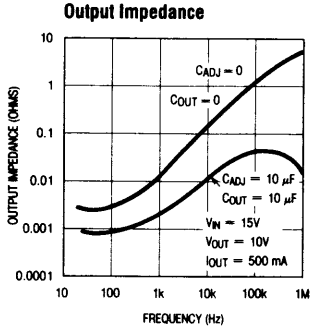
Adjustment Current



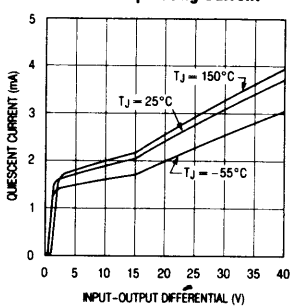
Temperature Stability



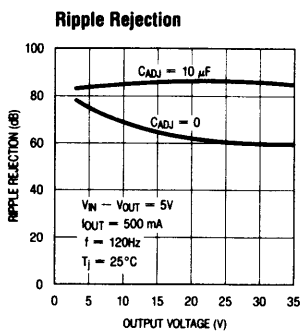
Output Impedance



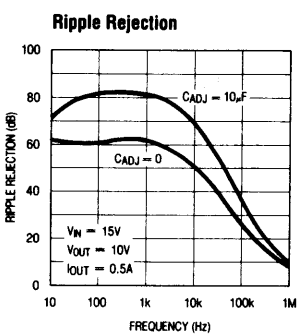
Minimum Operating Current



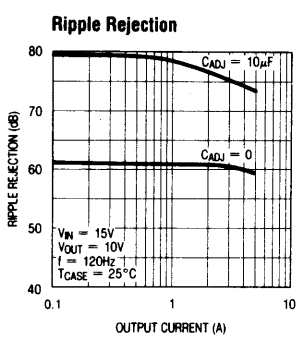
Ripple Rejection



Ripple Rejection

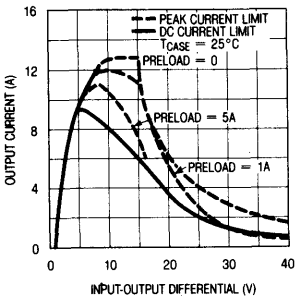


Ripple Rejection

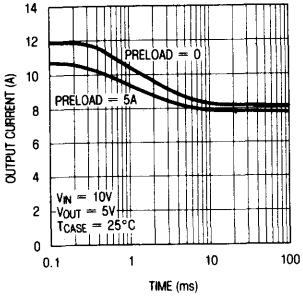


TYPICAL PERFORMANCE CHARACTERISTICS

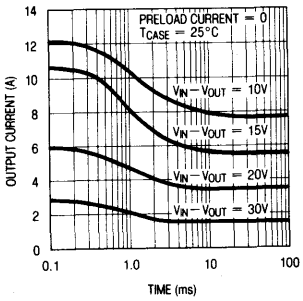
Current Limit



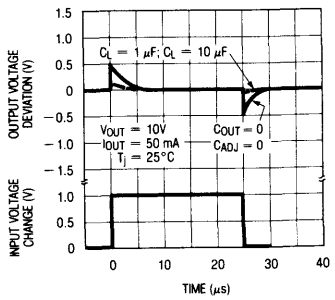
Current Limit



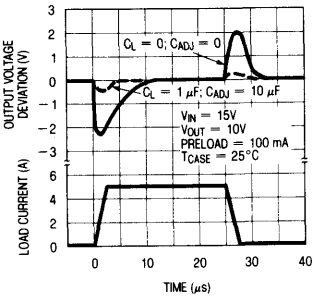
Current Limit



Line Transient Response



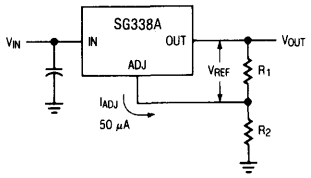
Load Transient Response



APPLICATIONS INFORMATION

General

The SG138A develops a 1.25V reference voltage between the output and the adjustable terminal (see Figure 1). By placing a resistor, R1, between these two terminals, a constant current is caused to flow through R1 and down through R2 to set the overall output voltage. Normally this current is the specified minimum load current of 5mA or 10mA. Because I_{ADJ} is very small and constant when compared with the current through R1, it represents a small error and can usually be ignored. It is easily seen from the output voltage equation, that even if the resistors were of exact value, the accuracy of the output is limited by the accuracy of V_{REF}. Earlier adjustable regulators had a reference tolerance of ±4% which is dangerously close to the ±5% supply tolerance required in many logic and analog systems. Further, even 1% resistors can drift 0.01%/°C, adding additional error to the output voltage tolerance.



$$V_{OUT} = V_{REF}\left(1 + \frac{R_2}{R_1}\right) + I_{ADJ}R_2$$

Basic Adjustable Regulator

Figure 1

For example, using 2% resistors and ±4% tolerance for V_{REF}, calculations will show that the expected range of a 5V regulator design would be $4.66V \leq V_{OUT} \leq 5.36V$ or approximately ±7%. If the same example were used for a 15V regulator, the expected tolerance would be ±8%. With these results most applications required some method of trimming, usually a trim pot. This solution is both expensive and not conducive to volume production.

One of the enhancements of Silicon General's adjustable regulators over existing devices is the tightened initial tolerance of V_{REF}. This allows relatively inexpensive 1% or 2% film resistors to be used to R1 and R2 to set the output voltage within an acceptable tolerance.

With a guaranteed 1% reference, a 5V power supply design, using ±2% resistors, would have a worst case manufacturing tolerance of ±4%. If 1% resistors are used, the tolerance will drop to ±2.5%. A plot of the worst case output voltage tolerance as a function of resistor tolerance is shown on the front page.

For convenience, a table of standard 1% resistor values is shown below.

Table of ½% and 1% Standard Resistance Values

1.00	1.47	2.15	3.16	4.64	6.81
1.02	1.50	2.21	3.24	4.75	6.98
1.05	1.54	2.26	3.32	4.87	7.15
1.07	1.58	2.32	3.40	4.99	7.32
1.10	1.62	2.37	3.48	5.11	7.50
1.13	1.65	2.43	3.57	5.23	7.68
1.15	1.69	2.49	3.65	5.36	7.87
1.18	1.74	2.55	3.74	5.49	8.06
1.21	1.78	2.61	3.83	5.62	8.25
1.24	1.82	2.67	3.92	5.76	8.45
1.27	1.87	2.74	4.02	5.90	8.66
1.30	1.91	2.80	4.12	6.04	8.87
1.33	1.96	2.87	4.22	6.19	9.09
1.37	2.00	2.94	4.32	6.34	9.31
1.40	2.05	3.01	4.42	6.49	9.53
1.43	2.10	3.09	4.53	6.65	9.76

Standard Resistance Values are obtained from the Decade Table by multiplying by multiples of 10. As an example, 1.21 can represent 1.21Ω, 12.1Ω, 121Ω, 1.21KΩ etc.

Bypass Capacitors

Input bypassing using a 1μF tantalum or 25μF electrolytic is recommended when the input filter capacitors are more than 5 inches from the device. Improved ripple rejection (80 dB) can be accomplished by adding a 10μF capacitor from the adjust pin to ground. Increasing the size of the capacitor to 20μF will help ripple rejection at low output voltage since the reactance of this capacitor should be small compared to the voltage setting resistor, R2. For improved AC transient response and to prevent the possibility of oscillation due to unknown reactive load, a 1μF capacitor is also recommended at the output. Because of their low impedance at high frequencies, the best type of capacitor to use is solid tantalum.

Protection Diodes

The SG138A/338A do not require a protection diode from the adjustment terminal to the output (see figure 2). Improved internal circuitry eliminates the need for this diode when the adjustment pin is bypassed with a capacitor to improve ripple rejection.

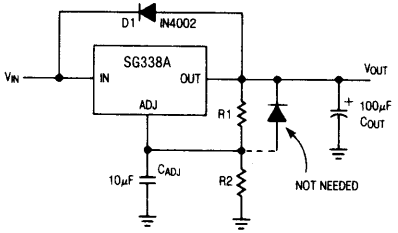


Figure 2

If a very large output capacitor is used, such as a 100μF shown in figure 2, the regulator could be damaged or destroyed if the input is accidentally shorted to ground or crowbarred, due to the output capacitor discharging into the output terminal of the regulator. To prevent this, a diode D1 as shown, is recommended to safely discharge the capacitor.

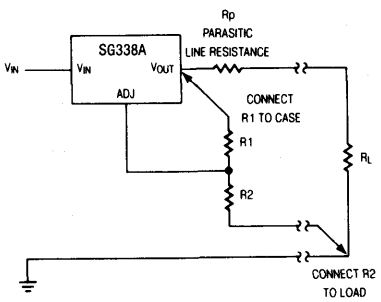
Load Regulation

Because the SG138A is a three-terminal device, it is not possible to provide true remote load sensing. Load regulation will be limited by the resistance of the wire connecting the regulator to the load. The data sheet specification for load regulation is measured at the bottom of the package. Negative side sensing is a true Kelvin connection, with the bottom of the output divider returned to the negative side of the load. Although it may not be immediately obvious, best load regulation is obtained when the top of the resistor divider, (R1), is connected *directly* to the case *not to the load.* This is illustrated in *Figure 3.* If R1 were connected to the

load, the effective resistance between the regulator and the load would be

$R_p \times \left(\frac{R2 + R1}{R1}\right)$, R_p = Parasitic Line Resistance.

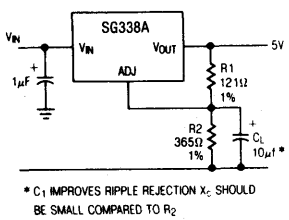
Connected as shown, R_p is not multiplied by the divider ratio. R_p is about 0.004Ω per foot using 16 gauge wire. This translates to 4mV/ft at 1A load current, so it is important to keep the positive lead between regulator and load as short as possible, and use large wire or PC board traces.



Connections For Best Load Regulation
Figure 3.

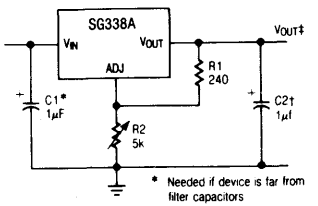
TYPICAL APPLICATIONS

Improving Ripple Rejection



* C_1 IMPROVES RIPPLE REJECTION X_C SHOULD BE SMALL COMPARED TO R_2

1.2V-25V Adjustable Regulator

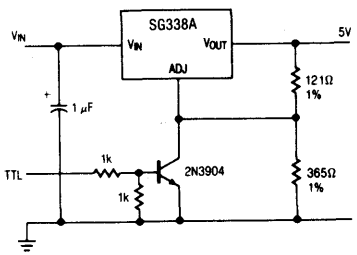


* Needed if device is far from filter capacitors

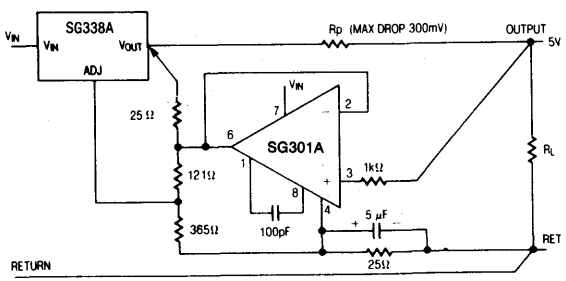
† Optional—improves transient response

‡ $V_{OUT} = 1.25V \left(1 + \frac{R2}{R1}\right)$

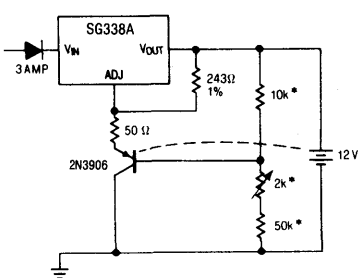
5V Regulator With Shut Down



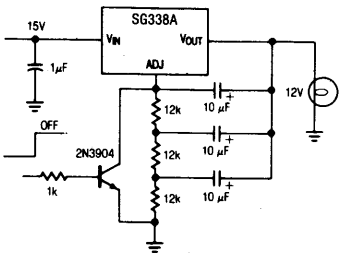
Remote Sensing



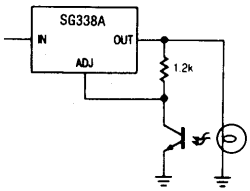
Temperature Compensated Lead Acid Battery Charger



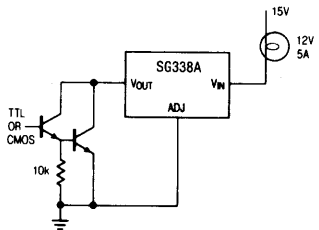
Lamp Flasher



Automatic Light Control

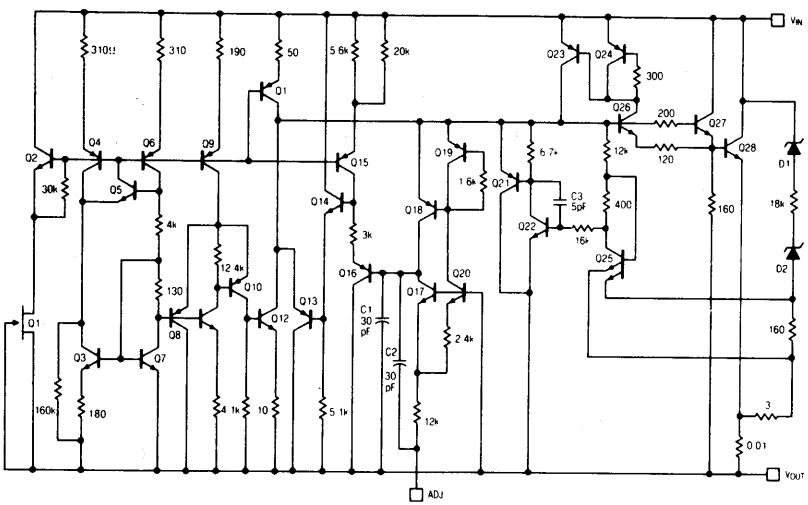


Protected High Current Lamp Driver



SCHEMATIC DIAGRAM

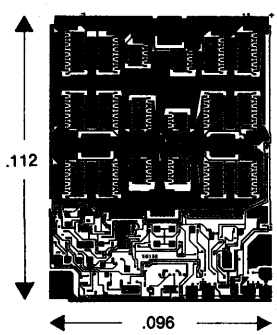
SG138A/SG338A



PACKAGE DESCRIPTION

	T_j max.	θ_{ja}	θ_{jc}
238A 238	150°C	35°C/W	1°C/W
338A 338	125°C	35°C/W	1°C/W

CHIP LAYOUT



1

3-AMP POSITIVE ADJUSTABLE REGULATOR

DESCRIPTION

The SG150/150A series are adjustable 3-terminal positive voltage regulators capable of supplying in excess of 3A over a 1.2V to 33V output range. They are exceptionally easy to use and require only 2 external resistors to set the output voltage. The SG150/150A series offers full overload protection available only in IC's. Included on the chip are current limit, thermal overload protection and safe operating area protection.

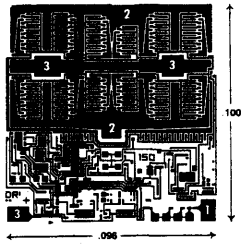
Since the regulator is "floating" and sees only the input-to-output differential voltage, supplies of several hundred volts can be regulated as long as the maximum input to output differential is not exceeded.

Supplies needing electronic shutdown can be achieved by clamping the adjustment terminal to ground, which programs the output to 1.2V where most loads draw little current. Reference voltage, which is trimmed to be within ±1% at room temperature, is guaranteed to be within ±2% over all operating conditions for the "A" version and ±4% for the standard version. They are packaged in standard steel TO-3 transistor packages.

FEATURES

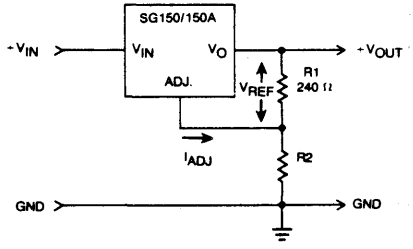
- **Trimmed ± 1% reference voltage**
- **Adjustable output down to 1.2V**
- **Guaranteed 3A output current**
- **Line Regulation typically 0.1%**
- **Guaranteed thermal regulation**
- **Current limit constant with temperature**
- **86 dB ripple rejection**
- **Standard 3-lead transistor package**

CHIP LAYOUT

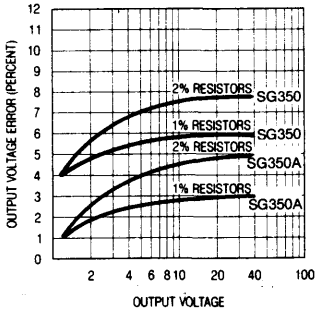


TYPICAL APPLICATIONS

BASIC REGULATOR



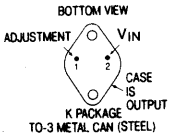
Output Voltage Error



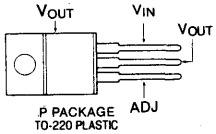
ABSOLUTE MAXIMUM RATINGS

Power Dissipation	**Internally limited**
Input-Output Voltage Differential	**35V**
Operating Junction Temperature Range	
SG150/150A	**−55°C to +150°C**
SG250/250A	**−25°C to +150°C**
SG350/350A	**0°C to +125°C**
Storage Temperature	**−65°C to +150°C**
Lead Temperature (Soldering, 10 seconds)	**300°C**

PACKAGE/ORDER INFORMATION



PART NUMBER
SG150AK
SG250AK
SG350AK
SG150K
SG250K
SG350K



PART NO.
SG350AT
SG350T

ELECTRICAL CHARACTERISTICS (See Note 1)

SYMBOL	PARAMETER	CONDITIONS		SG150A/SG250A MIN	SG150A/SG250A TYP	SG150A/SG250A MAX	SG150 MIN	SG150 TYP	SG150 MAX	UNITS
V_{REF}	Reference Voltage	I_{OUT} = 10mA, T_J = 25°C,		1.238	1.250	1.262				V
		3V ≤ (V_{IN} − V_{OUT}) ≤ 35V 10mA ≤ I_{OUT} ≤ 3A, P ≤ 30W	•	1.225	1.250	1.270	1.20	1.25	1.30	V
$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	Line Regulation	3V ≤ (V_{IN} − V_{OUT}) ≤ 35V, (See Note 2)			0.005	0.01		0.005	0.01	%/V
			•		0.02	0.05		0.02	0.05	%/V
$\frac{\Delta V_{OUT}}{\Delta I_{OUT}}$	Load Regulation	10mA ≤ I_{OUT} ≤ 3A, (See Note 2) T_A = 25°C, V_{OUT} ≤ 5V V_{OUT} ≥ 5V			5 0.1	15 0.3		5 0.1	15 0.3	mV %
		V_{OUT} ≤ 5V V_{OUT} ≥ 5V	• •		15 0.3	50 1		20 0.3	50 1	mV %
	Thermal Regulation	T_A = 25°C, 20msec Pulse			0.002	0.01		0.002	0.01	%/W
	Ripple Rejection	V_{OUT} = 10V, f = 120Hz C_{ADJ} = 0 C_{ADJ} = 10μF	• •	66	65 86		66	65 86		dB dB
I_{ADJ}	Adjust Pin Current		•		50	100		50	100	μA
ΔI_{ADJ}	Adjust Pin Current Change	10mA ≤ I_L ≤ 3A 3V ≤ (V_{IN} − V_{OUT}) ≤ 35V	•		0.2	5		0.2	5	μA
	Minimum Load Current	(V_{IN} − V_{OUT}) = 35V	•		3.5	5		3.5	5	mA
	Current Limit	(V_{IN} − V_{OUT}) ≤ 10V (V_{IN} − V_{OUT}) = 30V	• •	3 0.3	4.5 1		3 0.3	4.5 1		A A
$\frac{\Delta V_{OUT}}{\Delta TEMP}$	Temperature Stability	− 55°C ≤ T_J ≤ + 150°C	•		1	2		1		%
$\frac{\Delta V_{OUT}}{\Delta TIME}$	Long Term Stability	T_A = 125°C			0.3	1		0.3	1	%
e_n	RMS Output Noise (% of V_{OUT})	T_A = 25°C, 10Hz ≤ f ≤ 10kHz			0.001			0.001		%
Θ_{JC}	Thermal Resistance Junction to Case	K Package				1.5			1.5	°C/W

SYMBOL	PARAMETER	CONDITIONS		SG350A MIN	SG350A TYP	SG350A MAX	SG350 MIN	SG350 TYP	SG350 MAX	UNITS
V_{REF}	Reference Voltage	I_{OUT} = 10mA, T_J = 25°C,		1.238	1.250	1.262				V
		3V ≤ (V_{IN} − V_{OUT}) ≤ 35V 10mA ≤ I_{OUT} ≤ 3A, P ≤ 30W	•	1.225	1.250	1.270	1.20	1.25	1.30	V
$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	Line Regulation	3V ≤ (V_{IN} − V_{OUT}) ≤ 35V, (See Note 2) T_A = 25°C			0.005	0.01		0.005	0.03	%/V
			•		0.02	0.05		0.02	0.07	%/V
$\frac{\Delta V_{OUT}}{\Delta I_{OUT}}$	Load Regulation	10mA ≤ I_{OUT} ≤ 3A, (See Note 2) T_A = 25°C, V_{OUT} ≤ 5V V_{OUT} ≥ 5V			5 0.1	15 0.3		5 0.1	25 0.5	mV %
		V_{OUT} ≤ 5V V_{OUT} ≥ 5V	• •		15 0.3	50 1		20 0.3	70 1,5	mV %
	Thermal Regulation	T_A = 25°C, 20msec Pulse			0.002	0.01		0.002	0.03	%/W
	Ripple Rejection	V_{OUT} = 10V, f = 120Hz C_{ADJ} = 0 C_{ADJ} = 10μF	• •	66	65 86		66	65 86		dB dB
I_{ADJ}	Adjust Pin Current		•		50	100		50	100	μA
ΔI_{ADJ}	Adjust Pin Current Change	10mA ≤ I_{OUT} ≤ 3A 3V ≤ (V_{IN} − V_{OUT}) ≤ 35V	•		0.2	5		0.2	5	μA
	Minimum Load Current	(V_{IN} − V_{OUT}) ≤ 35V	•		3.5	10		3.5	10	mA
	Current Limit	(V_{IN} − V_{OUT}) ≤ 10V (V_{IN} − V_{OUT}) = 30V, T_J = 25°C	• •	3 0.25	4.5 1		3 0.25	4.5 1		A A
$\frac{\Delta V_{OUT}}{\Delta TEMP}$	Temperature Stability		•		1	2		1		%
$\frac{\Delta V_{OUT}}{\Delta TIME}$	Long Term Stability	T_A = 125°C			0.3	1		0.3	1	%
e_n	RMS Output Noise (% of V_{OUT})	T_A = 25°C, 10Hz ≤ f ≤ 10kHz			0.001			0.001		%
Θ_{JC}	Thermal Resistance Junction to Case	K Package T Package			1.2 3	1.5 4		1.2 3	1.5 4	°C/W °C/W

The • denotes the specifications which apply over the full operating temperature range.

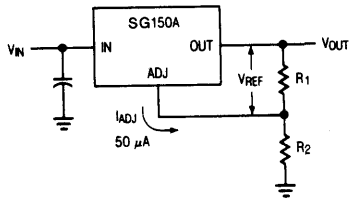
Note 1: Unless otherwise specified, these specifications apply for V_{IN} − V_{OUT} = 5V and I_{OUT} = 1.5A. These specifications are applicable for power dissipations up to 30W for the K package and up to 25W for the T package. Power dissipation is guaranteed at these values up to 15 Volts input-output differential. Above 15 Volts input-output differential power dissipation is limited by device internal protections circuitry.

Note 2: Regulation is measured at a constant T_j. Changes in output due to heating must be taken into account separately. Pulse testing with low duty cycle is used.

APPLICATIONS INFORMATION

General

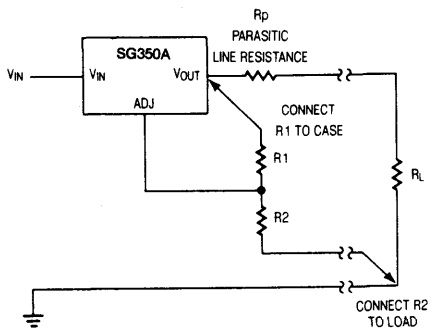
The SG150A develops a 1.25V reference voltage between the output and the adjustable terminal (see Figure 1). By placing a resistor, R1, between these two terminals, a constant current is caused to flow through R1 and down through R2 to set the overall output voltage. Normally this current is the specified minimum load current of 5mA or 10mA.



$$V_{OUT} = V_{REF}\left(1 + \frac{R_2}{R_1}\right) + I_{ADJ}R_2$$

Basic Adjustable Regulator
Figure 1

Because I_{ADJ} is a very small and constant when compared with the current through R1, it represents a small error and can usually be ignored. It is easily seen from the above equation, that even if the resistors were of exact value, the accuracy of the output is limited by the accuracy of V_{REF}. Earlier adjustable regulators had a reference tolerance of ±4% which is dangerously close to the ±5% supply tolerance required in many logic and analog systems. Further, even 1% resistors can drift 0.01%/°C, adding additional error to the output voltage tolerance.



Connections for Best Load Regulation
Figure 2

Bypass Capacitors

Input bypassing using a 1μF tantalum or 25μF electrolytic is recommended when the input filter capacitors are more than 5 inches from the device. Improved ripple rejection (80 dB) can be accomplished by adding a 10μF capacitor from the adjust pin to ground. Increasing the size of the capacitor to 20μF will help ripple rejection at low output voltage since the reactance of this capacitor should be small compared to the voltage setting resistor, R2. For improved AC transient response and to prevent the possibility of oscillation due to unknown reactive load, a 1μF capacitor is also recommended at the output. Because of their low impedance at high frequencies, the best type of capacitor to use is solid tantalum.

Load Regulation

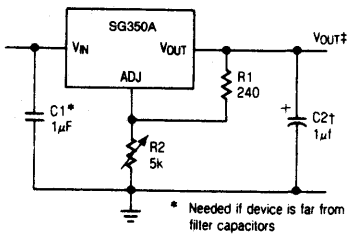
Because the SG150A is a three-terminal device, it is not possible to provide true remote load sensing. Load regulation will be limited by the resistance of the wire connecting the regulator to the load. The data sheet specification for load regulation is measured at the bottom of the package. Negative side sensing is a true Kelvin connection, with the bottom of the output divider returned to the negative side of the load. Although it may not be immediately obvious, best load regulation is obtained when the top of the resistor divider (R1) is connected directly to the case, not the load. This is illustrated in Figure 2. If R1 were connected to the load, the effective resistance between the regulator and the load would be

$$R_p \times \left(\frac{R2 + R1}{R1}\right), R_p = \text{Parasitic Line Resistance.}$$

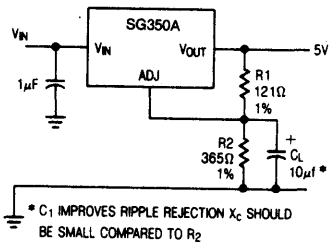
Connected as shown, R_p is not multiplied by the divider ratio. R_p is about 0.004Ω per foot using 16 gauge wire. This translates to 4mV/ft at a 1A load current, so it is important to keep the positive lead between regulator and load as short as possible, and use large wire or PC board traces.

TYPICAL APPLICATIONS

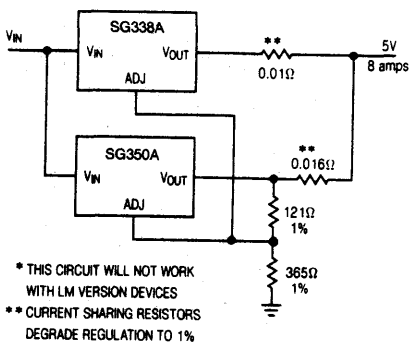
1.2V–25V Adjustable Regulator



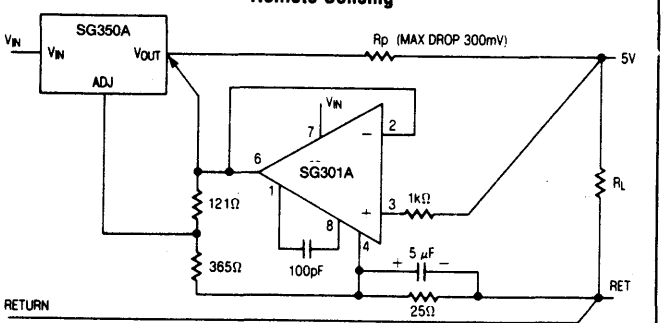
Improving Ripple Rejection



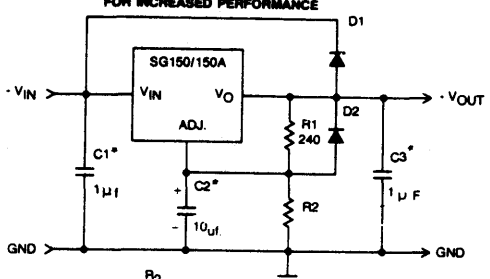
*Parallel Regulators for Higher Current



Remote Sensing



BASIC REGULATOR WITH CAPACITORS* FOR INCREASED PERFORMANCE



*No external capacitors are required with the SG150A/150 but in some applications, performance may be improved with added capacitance as follows:

C1. An input capacitor at 0.1mfd will protect against problems when high line impedance is present. The device can be more sensitive to input impedance when output or adjustment capacitors are used.

C2. Bypassing the adjustment terminal to ground with a 10 mfd capacitor will improve the ripple rejection by about 15 dB.

C3. A 1 mfd tantalum capacitor on the output will improve transient response and keep the regulator from ringing due to tight capacitive loading.

In addition to external capacitors, it is sometimes good practice to add protection diodes D1 and D2 if there is a chance that a capacitor may discharge through the regulator 1C.

Diode D1 protects against C3 with an input short.
Diode 2 protects against C2 with an output short.

SILICON GENERAL
LINEAR INTEGRATED CIRCUITS

ADVANCED DATA
SG153/SG253/SG353
Performance data described herein represent design goals.
Final design specifications are subject to change.

HIGH CURRENT FIXED VOLTAGE REGULATORS

DESCRIPTION

The SG153 family of fixed-voltage, three-terminal regulators are designed to supply load currents in excess of three amps over a wide range of operating conditions. Requiring nothing more than a small output capacitor, these regulators feature output voltages internally trimmed to greater than ±2% accuracy. In addition to excellent line regulation, a voltage-boost circuit provides positive load regulation (increasing output voltage with increasing load current) to help correct for line losses.

All protective features of thermal shutdown, current limiting, and safe-area control have been designed into these units with added reliability offered by a hard-solder eutectic die attach and an hermetically sealed TO-3 power package.

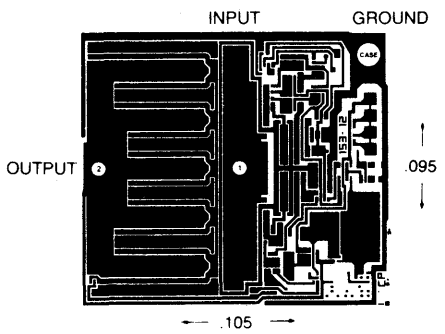
FEATURES

- **Load current in excess of 3A**
- **Output voltage trimmed to ±2%**
- **Complete self-contained protective features**
- **Correction for line resistance**
- **Eliminates external voltage setting resistors**
- **Hermetically sealed steel power package**
- **Available with 5, 12, and 15 volt outputs**

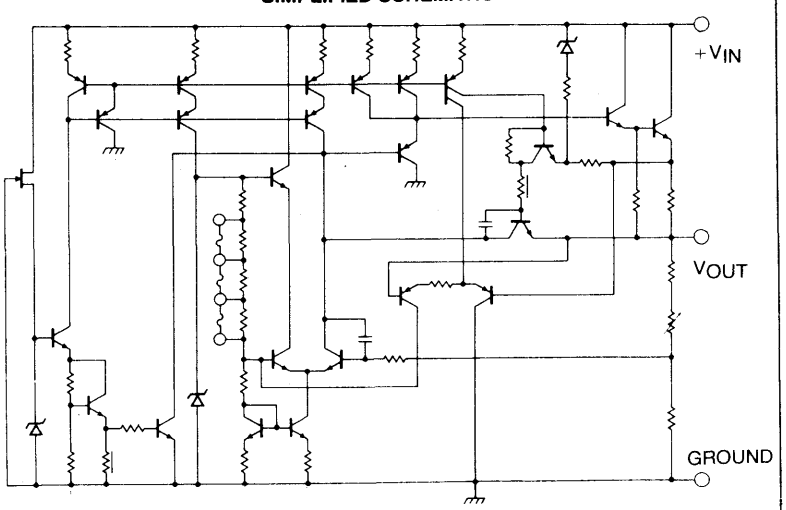
ABSOLUTE MAXIMUM RATINGS

Input Voltage	35 Volts
Power Dissipation (Internally limited)	50 Watts
Operating Temperature Range (T_J)	
SG153 Series	−55°C to +150°C
SG253 Series	−25°C to +150°C
SG353 Series	0°C to +125°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

CHIP LAYOUT

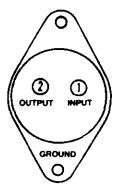


SIMPLIFIED SCHEMATIC



PACKAGE/ORDER INFORMATION

TOP VIEWS
(Case is internally connected to ground)



K-PACKAGE
TO-3

ORDER PART NO.:

SG153K-5	SG153K-12	SG153K-15
SG253K-5	SG253K-12	SG253K-15
SG353K-5	SG353K-12	SG353K-15

ELECTRICAL CHARACTERISTICS (See Note 1)

V_{in} unless otherwise specified (Note 1)

PARAMETER	TEST CONDITIONS	10V				19V				25V				UNITS
		SG153/SG253-05		SG353-05		SG153/SG253-12		SG353-12		SG153/SG253-15		SG353-15		
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
V_{OUT}	I_O = 1A, 25°C V_{IN} = (V_{OUT} + 2.5V) to 30V I_O = 5mA to 3A, P≤ 30W	4.9 4.8	5.1 5.2	4.8 4.4	5.2 5.4	11.8 11.6	12.2 12.4	11.5 11.25	12.5 12.75	14.8 14.6	15.2 15.4	14.4 14.15	15.6 15.85	V V
Load Regulation (Note 2)	5mA-1A 5mA-3A I_O, 25°C 500mA-1.5A		20 30 20		30 50 30		50 80 50		80 130 80		60 100 60		100 150 100	mV mV mV
Line Reg. Range	(Note 2)	7V ≤ V_{IN} ≤ 25V				14.5V ≤ V_{IN} ≤ 30V				17.5V ≤ V_{IN} ≤ 30V				
Line Regulation	I_O = 1A, 25°C		50		75		50		100		50		100	mV
Line Reg. Range	(Note 2)	8V ≤ V_{IN} ≤ 12V				16V ≤ V_{IN} ≤ 22V				20V ≤ V_{IN} ≤ 26V				
Line Regulation	I_O = 1A, 25°C		25		50		30		60		30		60	mV
Quiescent Current	I_O = 1A, 25°C		9		12		9		12		9		12	mA
Quiescent Current Change	With Load: I_O = 5mA-2A, 25°C With Line: V_{IN} = 8-25V, 25°C V_{IN} = 15-30V, 25°C V_{IN} = 18.5-30V, 25°C		500 1.0		500 1.5		500 1.0		500 1.5		500 1.0		 1.5	μA mA mA mA
I_O — Peak	25°C V_{IN} = 35V, 25°C	3 60	6	3 60	6	3 600	6	3 600	6	3 600	6	3 600	6	A mA
I_O, Short Circuit	V_O = V_{IN} = 35V, 25°C		100		100		100		100		100		100	mA
Ripple Rejection at I_O = 100mA	V_{IN} = 8-18V, 120Hz sine, 25°C V_{IN} = 15-25V, 120Hz sine, 25°C V_{IN} = 18-28V, 120Hz sine, 25°C	51		41		 46		 41		 46		 41		dB dB dB

Note 1: Unless otherwise specified, these specifications apply: $-55°C \leq T_J \leq +150°C$ for the SG153; $-25°C \leq T_J \leq +150°C$ for the SG253, and $0°C \leq T_J \leq +125°C$ for the SG353 and I_{OUT} = 1.0A. Although power dissipation is internally limited, these specifications are applicable for power dissipations up to 30W.

Note 2: Regulation is measured at constant junction temperature. Changes in output voltage due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

General-Purpose Positive Regulator

This regulator is designed for use with either positive or negative supplies as a series, shunt, switching, or floating regulator with currents up to 150mA. Higher current requirements may be accommodated through the use of external NPN or PNP power transistors.

- **Positive or negative supply operation**
- **0.03% line and load regulation**
- **Output adjustable from 2 to 37V**
- **Low standby current drain**
- **0.002%/°C average temperature variation**

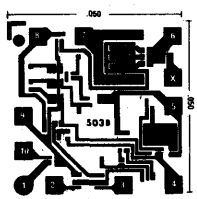
PARAMETERS	723[1]	723C[1]	UNITS
Operating Temperature Range	−55 to +125	0 to +70	°C
Package Types	T*, J	T*, J, N	—
Input Voltage Range	9.5 to 50	9.5 to 50	V
Output Voltage Range	2.0 to 37	2.0 to 37	V
Input/Output Differential	3.0 to 38	3.0 to 38	V
Load Regulation[2,3]	0.15	0.2	% V_{out}
Line Regulation V_{in} = 12 to 40V	0.2	0.5	% V_{out}
Ripple Rejection C_{ref} = 5μF; f = 50Hz to 10KHz	86 (typ)	86 (typ)	dB
Reference Voltage	6.95 – 7.35	6.80 – 7.50	V
Temperature Stability	0.015	0.015	%/°C
Output Noise Voltage C_{ref} = 0; BW = 100Hz to 10KHz	20 (typ)	20 (typ)	μV rms
Standby Current Drain	3.5	4.0	mA
Minimum Load Current	0	0	mA
Long Term Stability	0.1 (typ)	0.1 (typ)	%/khr

[1] Parameters apply at T_A = +25°C, except temperature stability is over temperature ranges.

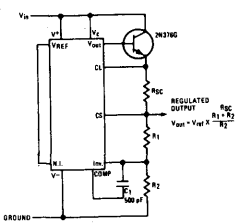
[2] Applies for constant junction temperature. Temperature drift effects must be taken into account separately when the unit is operating under conditions of high dissipation.

[3] I_L = 1 to 50 mA.

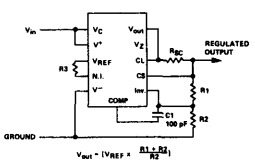
*T-package is TO-96 (can height: 240" max., 230" min.)



SG723/723C Chip
(See T-package for pad functions)
Note: V_Z (Pin X) is available only in J or N-Package

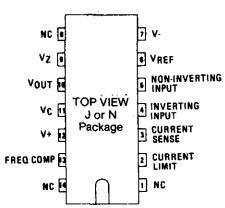


High Current Regulator
External NPN Transistor
I_L = 1A

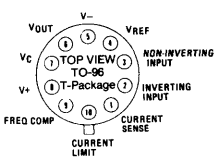


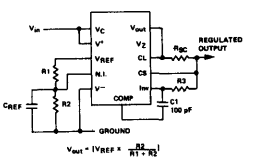
Basic High Voltage Regulator
V_{out} = 7 to 37 volts

CONNECTION DIAGRAMS



VZ available only in
J or N Package





Basic Low Voltage Regulator
V_{out} = 2 to 7 volts

SG1501A/2501A/3501A/4501

Dual-Polarity Tracking Regulators

SG1501A dual tracking regulators are factory set to provide balanced ±15V outputs, but a single external adjustment can be used to change both outputs, simultaneously. Line regulation of 20 mV and load regulation of 30 mV is guaranteed, and stability, over temperature, is 1% or less. Provision is made for adjustable current limiting and operation in excess of 2 amps is feasible with external transistors.

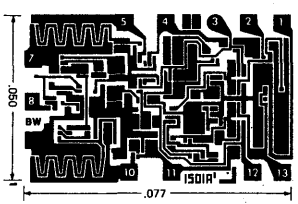
In the SG1501A, a buit-in sensing circuit monitors junction temperature and shuts down the regulator above 170°C eliminating the need for concern about power dissipation under short circuit conditions. The SG1501A series also offers superior input/output voltage range and current handling capability (refer to table of specifications.).

- **Thermal shutdown protection**
- **±35V inputs**
- **Output current to 200mA**
- **Output adjustable from ±10V to ±23V**

PARAMETERS[1]	1501A	2501A	3501A	4501	UNITS
Operating Temperature Range	−55 to +125	0 to +70	0 to +70	0 to +70	°C
Package Types	T, J		T, J, N		—
Output Voltage	±14.8/15.2		±14.5/15.5	±14.25/15.75	V
Input Voltage	±35		±30	±30	V
Input/Output Differential	2		2	2	V
Output Voltage Balance	150		300	300	mV
Line Regulation (V_{in} = 17 to V_{max})[5]	20		20	20	mV
Load Regulation (I_L = 0 to 50mA)[5]	30		30	30	mV
Output Voltage Range	10 to 23		10 to 23	10 to 23	V
Input Voltage Range (8V_{out})	10 to 35		10 to 30	12 to 30[4]	V
Ripple Rejection (f = 120Hz)	75 (typ)		75 (typ)	75 (typ)	dB
Temperature Stability	1.0		1.0	1.0	%
Short Circuit Current Limit[2]	60 (typ)		60 (typ)	60 (typ)	mA
Output Noise Voltage[3]	50 (typ)		50 (typ)	50 (typ)	μVrms
Positive Standby Current	4		4	4	mA
Negative Standby Current	5		5	5	mA
Long Term Stability	0.1 (typ)		0.1 (typ)	0.1 (typ)	%/khr
Output Current	200		200	100	mA
Thermal Shutdown Protection	yes		yes	yes	—

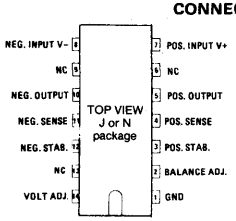
[1] All specifications apply to both positive and negative sides of the regulator, either singly or together. Unless otherwise specified T_A = +25°C, V_{in} = 20V, V_{out} = 15V, I_L = 0, Rsc = 0Ω, C1 = C2 = 0.01 mfd, C3 = C4 = 1.0 mfd, voltage adjust pin open

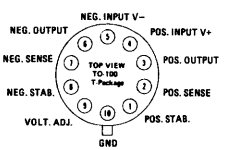
[2] Rsc = 10Ω [3] BW = 100Hz to 10kHz [4] 10V output [5] Over temperature range



SG1501A/2501A/3501A Chip (See T-package diagram for pad functions) Note: Balance Adjust (Pin X) is available only on D or N package.)

CONNECTION DIAGRAMS





See Applications Notes for additional information

Adjustable Dual-Polarity Tracking Regulators

This circuit is identical to the SG1501 series of dual polarity tracking regulators except that the internal voltage setting resistors are not included and the current limit inputs have been disconnected from the pass transistors. While this circuit does require external divider resistors, maximum versatility is offered in adjusting the output voltage levels, and additional current-limit inputs ease the application of foldback current limiting. In all other respects, this circuit performs as the SG1501.

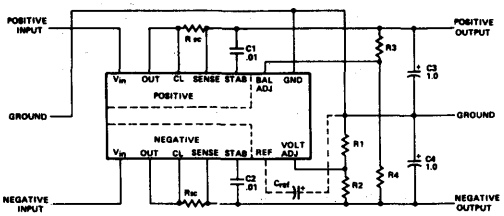
- **Positive and negative output voltages independently adjustable from 10 to 28V**
- **Output currents to 100mA**
- **Line and load regulation of 0.1%**
- **1% maximum temperature variation**
- **Standby current drain only 4mA**
- **Internal thermal shutdown protection**

PARAMETERS*	1502	2502	3502	UNITS
Operating Temperature Range	−55 to +125	0 to +70	0 to +70	°C
Package Types	J, N[4]		J, N	–
Input Voltage Range	±12/30		±12/25	V
Output Voltage Range	±10/28		±10/23	V
Input/Output Differential	2		2	V
Line Regulation (ΔV_{in} = 10V)[5]	0.2		0.2	% V_{out}
Load Regulation (I_L = 0 to 50mA)[5]	0.3		0.3	% V_{out}
Temperature Stability	1.0		1.0	% V_{out}
Current Limit Sense Voltage	0.6 (typ)		0.6 (typ)	V
Reference Voltage	6.3/6.6		6.2/6.8	V
Ripple Rejection f = 120Hz	75 (typ)		75 (typ)	dB
Output Noise Voltage[2]	50 (typ)		50	μVrms
Positive Standby Current[3]	4		4	mA
Negative Standby Current[3]	5		5	mA
Long Term Stability	0.1 (typ)		0.1 (typ)	%/khr

[1] All specifications apply to both positive and negative sides of the regulator either singly or together. Unless otherwise specified T_A = +25°C, V_{in} = +20V, V_{out} = +15V, I_L = 0, R_{SC} = 0Ω, C1 = C2 = 0.01 mfd, C3 = C4 = 1.0 mfd.

[2] BW = 100Hz to 10kHz [3] Divider 1 = 0.5mA [4] 1502 not available in plastic [5] Over temperature range

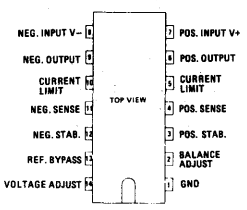
BASIC REGULATOR CIRCUIT

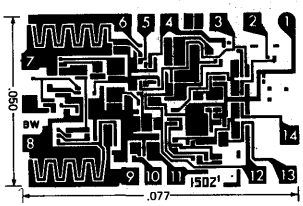


NEGATIVE $V_O = \frac{6.5 \times (R1 \times R2)}{R1}$, POSITIVE $V_O = \frac{R3}{R4}$ NEGATIVE V_O

For best temperature performance, the parallel impedance of R1 and R2 should be 6.3 K ohm while that of R3 and R4 should be 10 K. Increasing the value of C1 and C2 will reduce the frequency response while transient response may be improved by increasing C3 and C4. For very low-noise applications, a 4.7 mfd capacitor for Cref may be added. Rsc is selected such that a sense voltage of 0.6 volts (at Tj = 25°C) is developed at the maximum load current desired.

CONNECTION DIAGRAM





See Applications Notes for additional information

PRECISION GENERAL-PURPOSE REGULATOR

DESCRIPTION

This monolithic integrated circuit is a versatile, general-purpose voltage regulator designed as a substantially improved replacement for the popular SG723 device. The SG1532 series regulators retain all the versatility of the SG723 but have the added benefits of operation with input voltages as low as 4.5 volts and as high as 50 volts; a low noise, low voltage reference; temperature compensated, low threshold current limiting; and protective circuits which include thermal shutdown and independent current limiting of both the reference and output voltages. Also included is a separate remote shutdown terminal and – in the dual-in-line package – open collector outputs for low input-output differential applications.

These devices are available in both hermetic 14-pin cerdip DIL and 10-pin TO-96 packages. In the T-package, these units are interchangeable with the LAS-1000 and LAS-1100 regulators. The SG1532 is rated for operation over the temperature range of -55°C to +125°C while the SG2532 and SG3532 are intended for industrial applications of 0°C to +70°C.

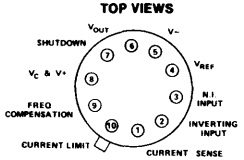
FEATURES:

- **Input voltage range of 4.5 to 50 volts**
- **2.5 volt low noise reference**
- **Independent shutdown terminal**
- **Improved line and load regulation**
- **80 mV current limit sense voltage**
- **Fully protected including thermal shutdown**
- **Useful output current to 150 mA**

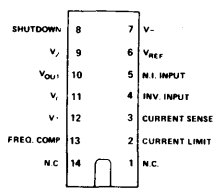
ABSOLUTE MAXIMUM RATINGS:

Input Voltage	
SG1532/2532	50 Volts
SG3532	40 Volts
Output Current	250 mA
Reference Current	25 mA
Zener current (J-package only)	100 mA
Storage Temperature Range	-65°C to +150°C
Power Dissipation	
T-Package (TO-96)	800 mW
Derate Above 25°C	6.4 mW/°C
J-Package (TO-116)	1000 mW
Derate Above 25°C	8 mW/°C
Operating Temperature Range	
SG1532	-55°C to +125°C
SG2532 and SG3532	0°C to +70°C

CONNECTION DIAGRAMS
TOP VIEWS

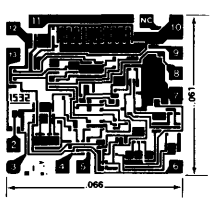


T-Package (TO-96)



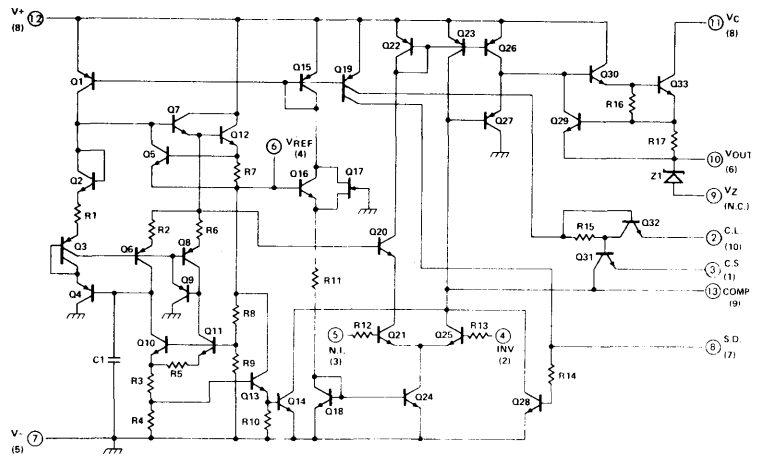
J-Package (TO-116)
"NOTE: V_z SHOULD NOT BE LEFT OPEN. IF UNUSED CONNECT TO V_{OUT}"

CHIP LAYOUT (J-pkg)



SIMPLIFIED SCHEMATIC

Pins numbered for J-Package – T-Package numbers in parenthesis



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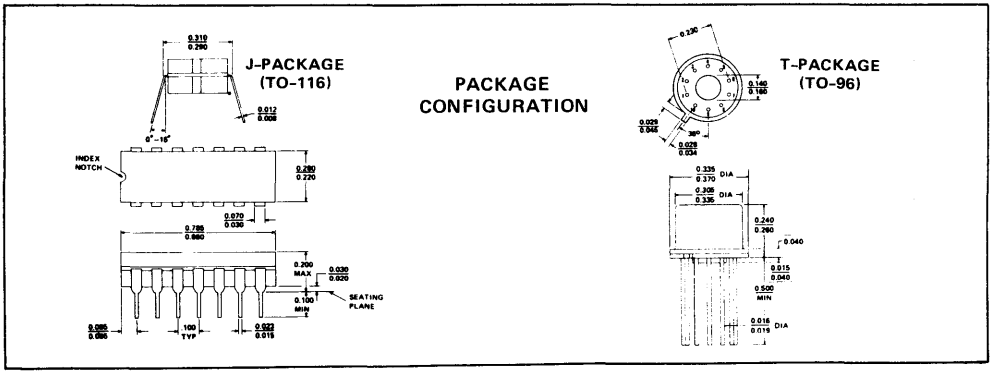
ELECTRICAL CHARACTERISTICS (See Notes 1 & 2)

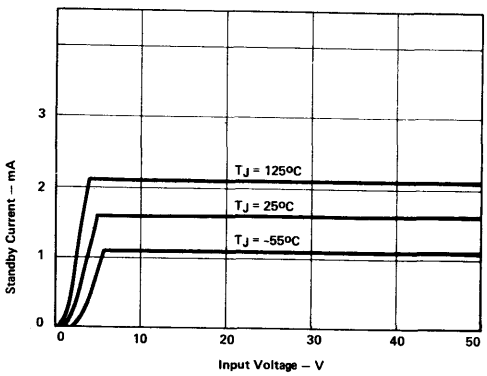
PARAMETER	CONDITIONS	SG1532/2532			SG3532			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Voltage	T_A = 25°C	4.5	–	50	4.5	–	40	Volts
Input Voltage	Over Temperature Range	4.7	–	50	4.7	–	40	Volts
Output Voltage		2.0	–	38	2.0	–	38	Volts
Max Output Current	R_{SC} = 0, V_O = 0, T_A = 25°C	–	175	250	–	175	250	mA
Min (V_{IN} - V_O)	I_O = 100 mA, T_A = 25°C	–	1.7	2.0	–	1.7	2.0	Volts
Reference Voltage	T_A = 25°C	2.40	2.50	2.60	2.40	2.50	2.60	Volts
Reference Voltage	Over Temperature Range	2.35	–	2.65	2.35	–	2.65	Volts
Temperature Stability		–	.005	.015	–	.005	.015	%/°C
Ref Short Ckt Current	V_{REF} = 0, T_A = 25°C	–	15	25	–	15	25	mA
Line Regulation	8V ≤ V_{IN} ≤ 40V	–	.005	.01	–	.005	.02	%/V
Line Regulation	8V ≤ V_{IN} ≤ 20V, I_O = 25 mA	–	.01	.02	–	.01	.03	%/V
Load Regulation	1 mA ≤ I_O ≤ 25 mA	–	.002	.004	–	.002	.004	%/mA
Load Regulation	1 mA ≤ I_O ≤ 100 mA	–	.002	.005	–	.002	.005	%/mA
Current Limit Sense Voltage	R_{SC} = 100Ω, V_O = 0	.06	.08	.10	.06	.08	.10	Volts
Shutdown Voltage Threshold		.40	.70	1.0	.40	.70	1.0	Volts
Shutdown Source Current	V_O = high	100	200	300	100	200	300	μA
Zener Voltage	J-Package only	6.0	6.4	7.0	6.0	6.4	7.0	Volts
Standby Current	V_{IN} = 40V	–	2.5	3.5	–	2.5	3.5	mA
Error Amplifier Offset Voltage		–	2.0	10	–	2.0	15	mV
Error Amplifier Input Bias Current		–	4	15	–	4	20	μA
Open Loop Gain	T_A = 25°C	66	68	72	60	68	72	dB
Ripple Rejection	f = 120Hz, T_A = 25°C	–	66	–	–	66	–	dB
Output Noise	10Hz ≤ f ≤ 100kHz, T_A = 25°C	–	50	–	–	50	–	μV_{rms}
Long Term Stability	V_{IN} = 30V, T_A = 125°C	–	0.3	1.0	–	0.3	1.0	%/kHr
Thermal Shutdown		–	175	–	–	175	–	°C

Note 1: Unless otherwise specified, V_{IN} = 10V, V_O = 5V, I_O = 1 mA, T_A = specified operating range.

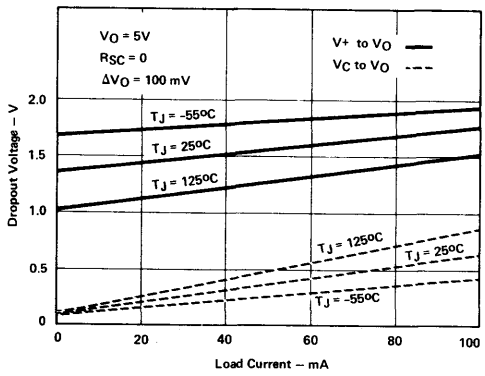
Note 2: All regulation specifications are measured at constant junction temperature using low duty-cycle pulse test.



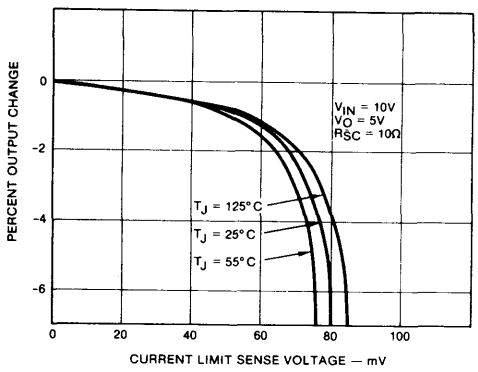
STANDBY CURRENT



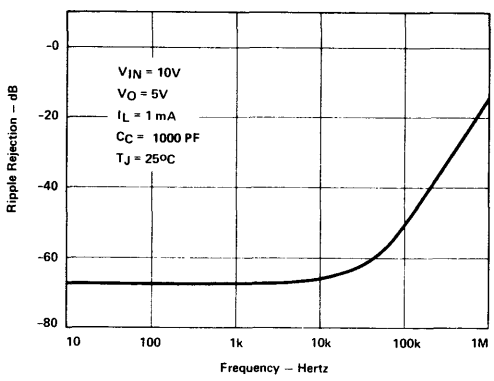
MINIMUM INPUT — OUTPUT VOLTAGE



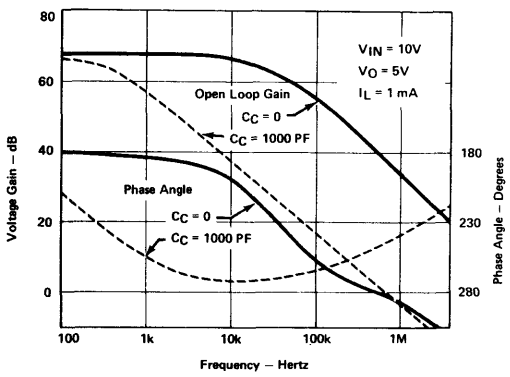
CURRENT LIMITING



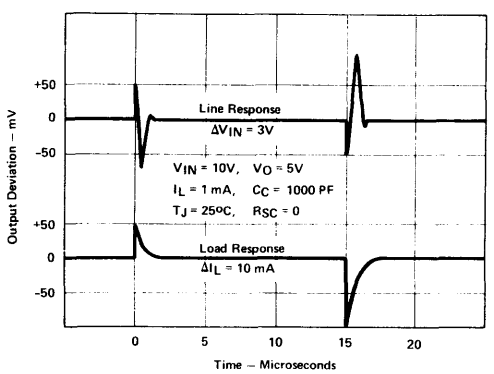
RIPPLE REJECTION



FREQUENCY RESPONSE



TRANSIENT RESPONSE



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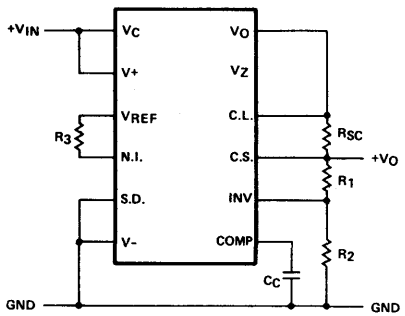
APPLICATIONS

BASIC LOW CURRENT REGULATOR



$V_O = V_{REF}\left(1 + \frac{R_1}{R_2}\right)$

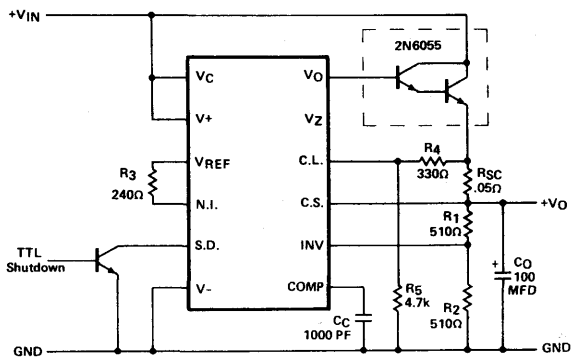
$R_3 = \frac{R_1 R_2}{R_1 + R_2}$

$I_{SC} = \frac{\text{Sense Voltage}}{R_{SC}}$

C_C = 1000 PF

I_O to 100 mA

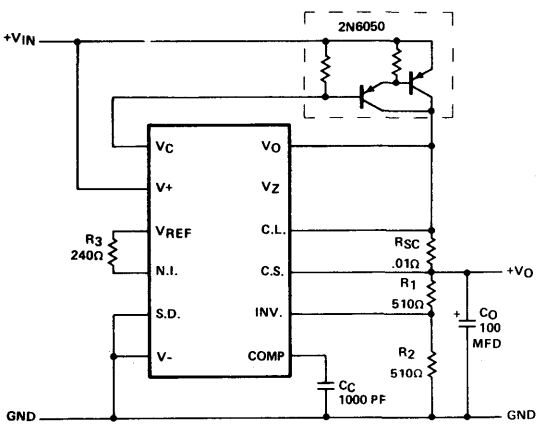
HIGH CURRENT REGULATOR WITH FOLDBACK CURRENT LIMITING AND REMOTE SHUTDOWN



Output Voltage = 5V
Max Output Current = 8A
Min V_{IN} at No Load = 6.9V
Min V_{IN} at 5A = 8.2V

Line Reg 10 - 30V = 3 mV
Load Reg 0 - 5A = 17 mV
Short Circuit Current = 1.8A

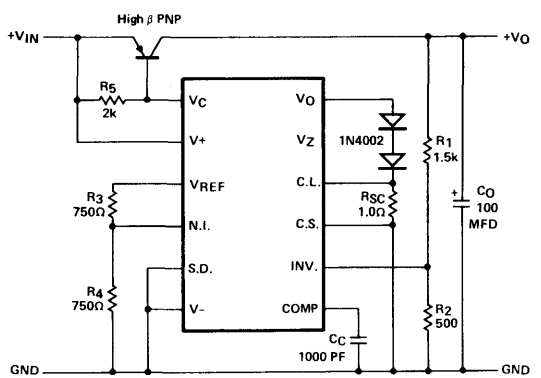
HIGH EFFICIENCY, LOW VOLTAGE REGULATOR



Output Voltage = 5V
Max Output Current = 9A
Min V_{IN} at 5A = 7.0V

Line Reg 7 - 20V = 10 mV
Load Reg 0 - 5A = 25 mV
Constant Current Limiting

90% EFFICIENT LINEAR REGULATOR



Output Voltage = 5V (Note 1)
Max Output Current = 3A (Note 2)
Min (V_{IN} - V_O) at 2A = 0.4V
Line Reg 6 - 30V = 10 mV
Load Reg 0 - 2A = 20 mV

Notes:

1. For output voltages above 8 volts and load currents which allow PNP base current to be limited to 25 mA, the internal zener may be used, eliminating the need for the two external diodes and the divider on V_{REF}.

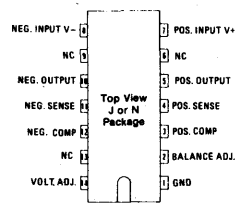
2. R_{SC} can be eliminated if the 200 mA current limit on V_O is adequate. Overall current limiting is dependent upon PNP β. For greater accuracy, load current may be sensed in the ground line.

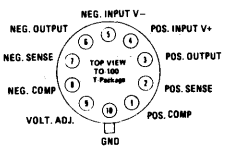
Dual-Polarity Tracking Regulators

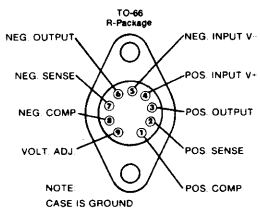
SG1568/1468 is a dual polarity tracking regulator designed to provide balanced positive and negative output voltages at currents to 100mA. The device is set internally for ±15V outputs but a single external adjustment can be used to change both outputs simultaneously from 14.5 to 20 volts. Input voltages up to ±30 volts can be used and there is provision for adjustable current limiting.

- **Outputs balanced to within 1% (SG1568)**
- **Line and load regulation of 0.06%**
- **1% maximum output variation due to temperature changes**
- **Standby current drain of 3.0mA**
- **Remote sensing provisions**

CONNECTION DIAGRAMS





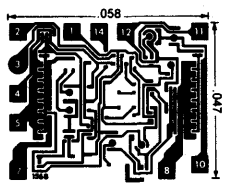


PARAMETERS*	SG1568	SG1468	UNIT
Operating Temperature Range	–55 to +125	0 to +75	°C
Package Types	T, J	T, J, N	–
Peak Load Current	100		mA
Storage Junction Temp Range	–65 to +175		°C
Output Voltage	14.8/15.2	14.5/15.5	V
Input Voltage	30	30	V
Input-Output Voltage Differential	2.0	2.0	V
Output Voltage Balance	±150	±300	mV
Line Regulation Voltage (V_{in} = 18V to 30V) (T_{low}[1] to T_{high}[2])	 10 20	 10 20	mV
Load Regulation Voltage (I_L = 0 to 50 mA, T_J = constant) (T_A = T_{low} to T_{high})	 10 30	 10 30	mV
Output Voltage Range	14.5/20	14.5/20	V
Ripple Rejection (f = 120Hz)	75 (typ)	75 (typ)	dB
Output Voltage Temperature Stability (T_{low} to T_{high})	1.0	1.0	%
Short-Circuit Current Limit (R_{SC} = 10 ohms)	60 (typ)	60 (typ)	mA
Output Noise Voltage (BW = 100Hz – 10kHz)	100 (typ)	100 (typ)	μV(rms)
Positive Standby Current (V_{in} = +30V)	4.0	4.0	mA
Negative Standby Current (V_{in} = –30V)	3.0	3.0	mA
Long-Term Stability	0.2 (typ)	0.2 (typ)	%/k Hr

(V_{CC} = +20V, V_{EE} = –20V, C1 = C2 = 1500 pF, C3 = C4 = 1.0 μF, R_{SC}^+ = R_{SC}^- = 4.0Ω, I_L^+ = I_L^- = 0, T_C = +25°C unless otherwise noted.)

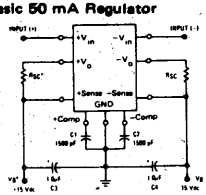
[1] T_{low} = 0°C for 1468
= –55°C for 1568

[2] T_{high} = +75°C for 1468
= +125°C for 1568



SG1568/1468 Chip (See J-Package diagram for pad functions)

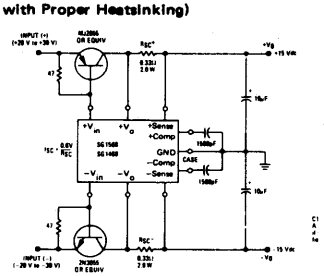
Basic 50 mA Regulator



C1 and C2 should be located as close to the device as possible. A 0.1μF ceramic capacitor may be required on the input lines if the device is located an appreciable distance from the rectifier filter capacitors.

C3 and C4 may be increased to improve load transient response and to reduce the output noise voltage. At low temperature operation it may be necessary to bypass C4 with a 0.1μF ceramic disc capacitor.

±1.5 Amp Regulator (Short Circuit Protected, with Proper Heatsinking)



See Applications Notes for additional information.

1

Three Terminal Positive Regulators

DESCRIPTION

The SG7800A/7800/140 series of positive regulators offer self contained, fixed-voltage capability with up to 1.5 amps of load current and input voltages up to 50 volts. (SG7800A series only)

These units feature a unique on-chip trimming system to set the output voltages to within ±1.5% of nominal on the SG7800A series, ±2.0% on the SG140/240 series, and ±4.0% on the SG7800/340 series. The SG7800A versions also offer much improved line and load regulation characteristics.

All protective features of thermal shutdown, current limiting, and safe-area control have been designed into these units and since these regulators require only a small output capacitor for satisfactory performance, ease of application is assured.

Although designed as fixed-voltage regulators, the output voltage can be increased through the use of a simple voltage divider. The low quiescent drain current of the device insures good regulation when this method is used.

Product is available in hermetically sealed TO-3, TO-39 and TO-66 power packages as well as the plastic TO-220 package.

FEATURES

- **Output voltage set internally to ±1.5% on SG7800A**
- **Input voltage range to 50 volts max. on SG7800A**
- **Two volt input-output differential**
- **Excellent line and load regulation**
- **Foldback current limiting**
- **Thermal overload protection**
- **Voltages available — 5V, 6V, 8V, 12V, 15V, 18V, 20V, 24V**

ABSOLUTE MAXIMUM RATINGS

Device Output Voltage	Input Voltage (operating)	7800A Series Input Voltage (transient)*	Input Voltage (Output shorted to ground)
5V	35V	50V	35V
6V	35V	50V	35V
8V	35V	50V	35V
12V	35V	50V	35V
15V	35V	50V	35V
18V	35V	50V	35V
20V	35V	50V	35V
24V	40V	50V	35V

*see note next page

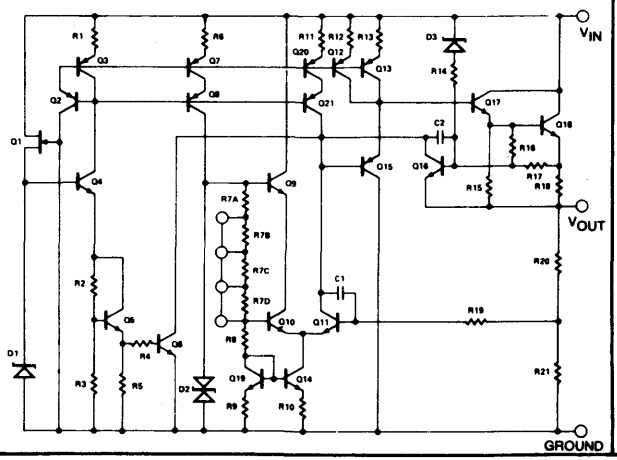
Operating Junction Temperature Range

SG7800A/7800/140	−55°C to +150°C
SG240	0°C to +150°C
SG7800AC/7800C/340	0°C to +125°C
Storage Temperature Range	−65°C to +150°C

Typical Power/Thermal Characteristics

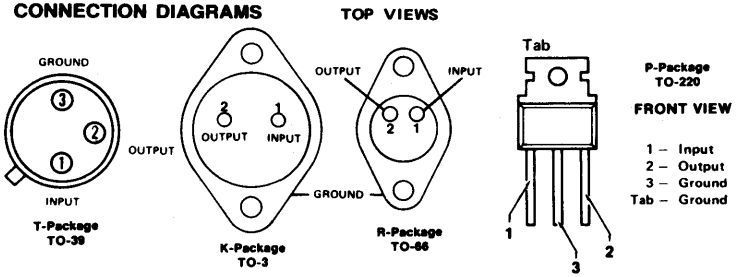
Package	K (TO-3)	R (TO-66)	P (TO-220)	T (TO-39)
25°C Case Rated Power	20W	15W	15W	2W
25°C Ambient Rated Power	4.3W	3.0W	2.0W	1.0W
Design Current	1.5A	1.5A	1.0A	0.5A
Therm. Res. θJC (°C/W)	3.0	5.0	3.0	15
θJA (°C/W)	35	40	60	120

SIMPLIFIED SCHEMATIC

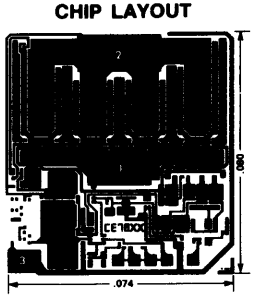


CONNECTION DIAGRAMS

TOP VIEWS

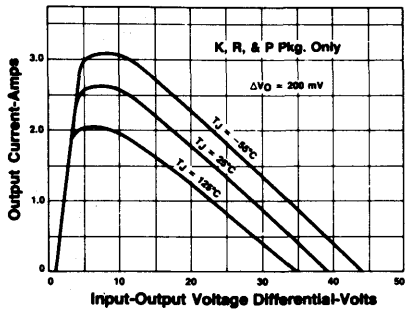


CHIP LAYOUT

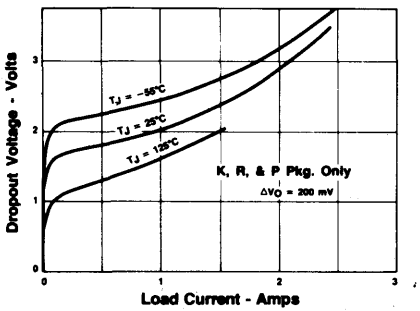


CHARACTERISTIC CURVES

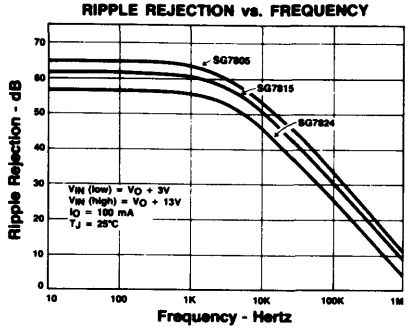
PEAK OUTPUT CURRENT vs. INPUT-OUTPUT DIFFERENTIAL



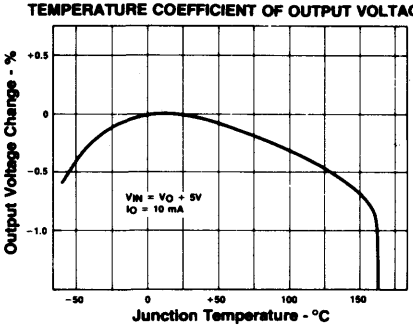
MINIMUM INPUT-OUTPUT VOLTAGE vs. LOAD CURRENT



RIPPLE REJECTION vs. FREQUENCY



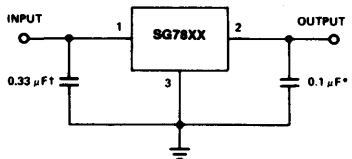
TEMPERATURE COEFFICIENT OF OUTPUT VOLTAGE



Note: Operation at high input voltages is dependent upon load current. When load current is less than 5 mA, output will rise out of regulation as input-output differential increases beyond 30 volts. Note also from curve above, that maximum load current is reduced at high voltages. The 50 volt input rating of the SG7800A series refers to ability to withstand high line or transient conditions without damage. Since the regulator's maximum current capability is reduced, the output may fall out of regulation at high input voltages under nominal loading.

APPLICATIONS

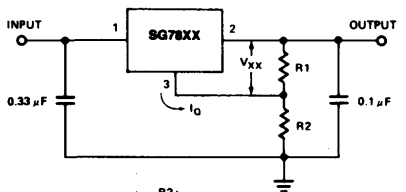
FIXED OUTPUT REGULATOR



*INCREASING VALUE OF OUTPUT CAPACITOR IMPROVES SYSTEM TRANSIENT RESPONSE

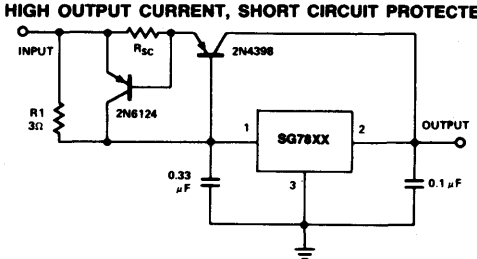
†REQUIRED ONLY IF REGULATOR IS LOCATED AN APPRECIABLE DISTANCE FROM POWER SUPPLY FILTER

CIRCUIT FOR INCREASING OUTPUT VOLTAGE

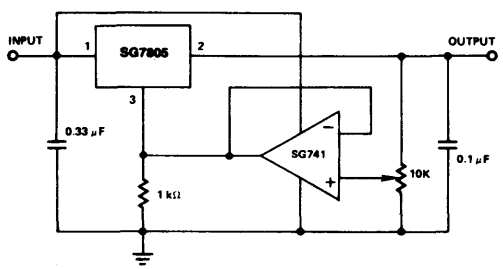


$$V_O = V_{XX}\left(1 + \frac{R2}{R1}\right) + I_Q R2$$

HIGH OUTPUT CURRENT, SHORT CIRCUIT PROTECTED



ADJUSTABLE OUTPUT REGULATOR, 7 to 30 VOLTS



DEVICE PART NUMBERS			SG7805A			SG140-05			SG7805(109)			SG7805AC			SG340-05(309)			SG7805C			
PACKAGE STYLES (P/N SUFFIX)			K,R,T			K,R,T			K,R,T			K,P,R,T			K,P,R,T			K,P,R,T			
OPERATING JUNCTION TEMPERATURE RANGE (Unless otherwise specified below)			−55°C to +150°C			−55°C to 150°C			−55°C to 150°C			0°C to 125°C			0°C to 125°C			0°C to 125°C			
PARAMETERS		**TEST CONDITIONS (See notes below)**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Output Voltage		T_J = 25°C	4.92		5.08	4.8		5.2	4.8		5.2	4.92		5.08	4.8		5.2	4.8		5.2	V
Line Regulation		T_J = 25°C, V_{IN} = 7 to 25V		5	25		5	50		5	50		5	50		5	50		10	100	mV
		T_J = 25°C, V_{IN} = 8 to 12V		2	12		2	25		2	25		2	25		2	25		4	50	mV
Load Regulation	P,R,K Pkg	T_J = 25°C, I_O = 5mA to 1.5A		15	50		15	50		15	50		15	50		15	50		25	100	mV
		T_J = 25°C, I_O = 250 to 750mA		5	25		5	25		5	25		5	25		5	25		10	50	mV
	T-Pkg	T_J = 25°C, I_O = 5mA to 500mA		5	25		5	25		5	25		5	25		5	25		20	100	mV
Total Output Voltage Tolerance V_{IN} = 8 to 20V		K-Pkg: I_O = 5 to 1.0A, P ≤ 20W	4.85		5.15	4.75		5.25	4.65		5.35	4.85		5.15	4.75		5.25	4.75		5.25	V
		R,P-Pkg: I_O = 5 to 1000mA, P ≤ 15W																			
		T-Pkg: I_O = 5 to 500mA, P ≤ 2W																			
Quiescent Current		T_J = 25°C		4	6		4	6		4	6		4	6		4	8		4	8	mA
		Over Temperature Range			7			7			7			7			8.5			8.5	mA
Quiescent Current Change		With line: V_{IN} = 8 to 25V			0.8			0.8			0.8			1.0			1.0			1.3	mA
		With load: I_O = 5 to 1000mA			0.5			0.5			0.5			0.5			0.5			0.5	mA
Dropout Voltage ΔV_O = 100mV		T_J = 25°C, K,R,P-Pkg: I_O = 1A		2			2			2			2			2			2		V
		T_J = 25°C, T-Pkg: I_O = 500mA		1.8			1.8			1.8			1.8			1.8			1.8		
Peak Output Current		T_J = 25°C, K,R,P-Pkg		2.5			2.5			2.5			2.5			2.5			2.5		A
		T_J = 25°C, T-Pkg		1.0			1.0			1.0			1.0			1.0			1.0		A
Short Circuit Current		T_J = 25°C, K,R,P-Pkg		2.1			2.1			2.1			2.1			2.1			2.1		A
		T_J = 25°C, T-Pkg		0.7			0.7			0.7			0.7			0.7			0.7		A
Temperature Coefficient		I_O = 5mA		−0.5			−0.5			−0.5			−0.5			−0.5			−0.5		mV /°C
Ripple Rejection		T_J = 25°C, f = 120Hz, ΔV_{IN} = 10V		70			70			70			70			70			70		dB
Output Noise Voltage		T_J = 25°C, f = 10Hz to 100 kHz		40			40			40			40			40			40		μV rms
Long Term Stability		1000 hrs. at T_J = 125°C		20			20			20			20			20			20		mV
Thermal Shutdown		I_O = 5mA		175			175			175			175			175			175		°C

NOTES:

1. Minimum load current for full line regulation is 5mA.
2. Maximum test current for T-Pkg is 500mA.
3. Unless otherwise specified, V_{IN} = 10V and I_O = 500mA for K,R,P-Pkg; I_O = 100mA for T-Pkg.
4. All regulation tests are made at constant junction temperature with low duty-cycle testing.
5. At T_J = −55°C, minimum (V_{IN} − V_O) = 2.5V.
6. Short circuit protection is only assured to V_{IN} = 35V.

DEVICE PART NUMBERS			SG7806A			SG140-06			SG7806			SG7806A			SG340-06			SG7806C			
PACKAGE STYLES (P/N SUFFIX)			K,R,T			K,R,T			K,R,T			K,P,R,T			K,P,R,T			K,P,R,T			
OPERATING JUNCTION TEMPERATURE RANGE (Unless otherwise specified below)			−55°C to +150°C			−55°C to 150°C			−55°C to 150°C			0°C to 125°C			0°C to 125°C			0°C to 125°C			
PARAMETERS		**TEST CONDITIONS (See notes below)**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Output Voltage		T_J = 25°C	5.9		6.1	5.75		6.25	5.75		6.25	5.9		6.1	5.75		6.25	5.75		6.25	V
Line Regulation		T_J = 25°C, V_{IN} = 8 to 25V		6	30		6	60		6	60		6	60		6	60		12	120	mV
		V_{IN} = 9 to 13V		3	15		3	30		3	30		3	30		3	30		6	60	mV
Load Regulation	P,R,K Pkg	T_J = 25°C, I_O = 5mA to 1.5A		20	60		20	60		20	60		20	60		20	60		40	120	mV
		I_O = 250 to 750mA		6	30		6	30		6	30		6	30		6	30		12	60	mV
	T-Pkg	I_O = 5mA to 500mA		6	30		6	30		6	30		6	30		6	30		12	60	mV
Total Output Voltage Tolerance V_{IN} = 9 to 21V		K-Pkg: I_O = 5 to 1.0A, P 20W	5.82		6.18	5.7		6.3	5.65		6.35	5.82		6.18	5.7		6.3	5.7		6.3	V
		R,P-Pkg: I_O = 5 to 1000mA, P ≤ 15W																			
		T-Pkg: I_O = 5 to 500mA, P ≤ 2W																			
Quiescent Current		T_J = 25°C		4	6		4	6		4	6		4	6		4	8		4	8	mA
		Over Temperature Range			7			7			7			7			8.5			8.5	mA
Quiescent Current Change		With line: V_{IN} = 8 to 25V			0.8			0.8			0.8			1.0			1.0			1.3	mA
		With load: I_O = 5 to 1000mA			0.5			0.5			0.5			0.5			0.5			0.5	mA
Dropout Voltage ΔV_O = 100mV		T_J = 25°C, K,R,P-Pkg: I_O = 1A		2			2			2			2			2			2		V
		T-Pkg: I_O = 500mA		1.8			1.8			1.8			1.8			1.8			1.8		
Peak Output Current		T_J = 25°C, K,R,P-Pkg		2.5			2.5			2.5			2.5			2.5			2.5		A
		T-Pkg		1.0			1.0			1.0			1.0			1.0			1.0		A
Short Circuit Current		T_J = 25°C, K,R,P-Pkg		2.0			2.0			2.0			2.0			2.0			2.0		A
		T-Pkg		0.6			0.6			0.6			0.6			0.6			0.6		A
Temperature Coefficient		I_O = 5mA		−0.5			−0.5			−0.5			−0.5			−0.5			−0.5		mV /°C
Ripple Rejection		T_J = 25°C, f = 120Hz, ΔV_{IN} = 10V		68			68			68			68			68			68		dB
Output Noise Voltage		T_J = 25°C, f = 10Hz to 100 kHz		45			45			45			45			45			45		μV rms
Long Term Stability		1000 hrs. at T_J = 125°C		24			24			24			24			24			24		mV
Thermal Shutdown		I_O = 5mA		175			175			175			175			175			175		°C

NOTES:

1. Minimum load current for full line regulation is 5mA.
2. Maximum test current for T-Pkg is 500mA.
3. Unless otherwise specified, V_{IN} = 11V and I_O = 500mA for K,R,P-Pkg; I_O = 100mA for T-Pkg.
4. All regulation tests are made at constant junction temperature with low duty-cycle testing.
5. At T_J = −55°C, minimum (V_{IN} − V_O) = 2.5V.
6. Short circuit protection is only assured to V_{IN} = 35V.

DEVICE PART NUMBERS			SG7808A			SG140-08			SG7808			SG7808AC			SG340-08			SG7808C			
PACKAGE STYLES (P/N SUFFIX)			K,R,T			K,R,T			K,R,T			K,P,R,T			K,P,R,T			K,P,R,T			
OPERATING JUNCTION TEMPERATURE RANGE (Unless otherwise specified below)			−55°C to +150°C			−55°C to 150°C			−55°C to 150°C			0°C to 125°C			0°C to 125°C			0°C to 125°C			
PARAMETERS		**TEST CONDITIONS (See notes below)**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Output Voltage		T_J = 25°C	7.88		8.12	7.7		8.3	7.7		8.3	7.88		8.12	7.7		8.3	7.7		8.3	V
Line Regulation		T_J = 25°C, V_{IN} = 10.5 to 25V		8	40		8	80		8	80		8	80		8	80		16	160	mV
		V_{IN} = 11 to 17V		4	20		4	40		4	40		4	40		4	40		8	80	mV
Load Regulation	P,R,K Pkg	T_J = 25°C, I_O = 5mA to 1.5A		24	70		24	80		24	80		24	80		24	80		40	160	mV
		I_O = 250 to 750mA		8	35		8	40		8	40		8	40		8	40		16	80	mV
	T-Pkg	I_O = 5mA to 500mA		8	35		8	40		8	40		8	40		8	40		16	80	mV
Total Output Voltage Tolerance V_{IN} = 11.5 to 23V		K-Pkg: I_O = 5 to 1.0A, P 20W	7.76		8.24	7.6		8.4	7.6		8.4	7.6		8.24	7.6		8.4	7.6		8.4	V
		R,P-Pkg: I_O = 5 to 1000mA, P ≤ 15W																			
		T-Pkg: I_O = 5 to 500mA, P ≤ 2W																			
Quiescent Current		T_J = 25°C		4	6		4	6		4	6		4	6		4	8		4	8	mA
		Over Temperature Range			7			7			7			7			8.5			8.5	mA
Quiescent Current Change		With line: V_{IN} = 11.5 to 25V			0.8			0.8			0.8			1.0			1.0			1.0	mA
		With load: I_O = 5 to 1000mA			0.5			0.5			0.5			0.5			0.5			0.5	mA
Dropout Voltage ΔV_O = 100mV		T_J = 25°C, K,R,P-Pkg: I_O = 1A		2			2			2			2			2			2		V
		T-Pkg: I_O = 500mA		1.8			1.8			1.8			1.8			1.8			1.8		
Peak Output Current		T_J = 25°C, K,R,P-Pkg		2.5			2.5			2.5			2.5			2.5			2.5		A
		T-Pkg		1.0			1.0			1.0			1.0			1.0			1.0		A
Short Circuit Current		T_J = 25°C, K,R,P-Pkg		1.8			1.8			1.8			1.8			1.8			1.8		A
		T-Pkg		0.6			0.6			0.6			0.6			0.6			0.6		A
Temperature Coefficient		I_O = 5mA		−0.6			−0.6			−0.6			−0.6			−0.6			−0.6		mV /°C
Ripple Rejection		T_J = 25°C, f = 120Hz, ΔV_{IN} = 10V		68			68			68			68			68			68		dB
Output Noise Voltage		T_J = 25°C, f = 10Hz to 100 kHz		52			52			52			52			52			52		μV rms
Long Term Stability		1000 hrs. at T_J = 125°C		32			32			32			32			32			32		mV
Thermal Shutdown		I_O = 5mA		175			175			175			175			1765			175		°C

NOTES:

1. Minimum load current for full line regulation is 5mA.
2. Maximum test current for T-Pkg is 500mA.
3. Unless otherwise specified, V_{IN} = 14V and I_O = 500mA for K,R,P-Pkg; I_O = 100mA for T-Pkg.
4. All regulation tests are made at constant junction temperature with low duty-cycle testing.
5. At T_J = −55°C, minimum (V_{IN} − V_O) = 2.5V.
6. Short circuit protection is only assured to V_{IN} = 35V.

DEVICE PART NUMBERS			SG7812A			SG140-12			SG7812			SG7812AC			SG340-12			SG7812C			
PACKAGE STYLES (P/N SUFFIX)			K,R,T			K,R,T			K,R,T			K,P,R,T			K,P,R,T			K,P,R,T			
OPERATING JUNCTION TEMPERATURE RANGE (Unless otherwise specified below)			−55°C to +150°C			−55°C to 150°C			−55°C to 150°C			0°C to 125°C			0°C to 125°C			0°C to 125°C			
PARAMETERS		**TEST CONDITIONS (See notes below)**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Output Voltage		T_J = 25°C	11.8		12.2	11.5		12.5	11.5		12.5	11.8		12.2	11.5		12.5	11.5		12.5	V
Line Regulation		T_J = 25°C, V_{IN} = 14.5 to 30V		12	60		12	120		12	120		12	120		12	120		24	240	mV
		T_J = 25°C, V_{IN} = 16 to 22V		6	30		6	60		6	60		6	60		6	60		12	120	mV
Load Regulation	P,R,K Pkg	T_J = 25°C, I_O = 5mA to 1.5A		28	120		28	120		28	120		28	120		28	120		80	240	mV
	P,R,K Pkg	T_J = 25°C, I_O = 250 to 750mA		10	40		10	60		10	60		10	60		10	60		24	120	mV
	T-Pkg	T_J = 25°C, I_O = 5mA to 500mA		10	40		10	60		10	60		10	60		10	60		24	120	mV
Total Output Voltage Tolerance V_{IN} =15.5 to 27V		K-Pkg: I_O = 5 to 1.0A, P 20W	11.7		12.3	11.4		12.6	11.4		12.6	11.7		12.3	11.4		12.6	11.4		12.6	V
		R,P-Pkg: I_O = 5 to 1000mA, P ≤ 15W																			
		T-Pkg: I_O = 5 to 500mA, P ≤ 2W																			
Quiescent Current		T_J = 25°C		4	6		4	6		4	6		4	6		4	8		4	8	mA
		Over Temperature Range			7			7			7			7			8.5			8.5	mA
Quiescent Current Change		With line: V_{IN} = 15 to 30V			0.8			0.8			0.8			1.0			1.0			1.0	mA
		With load: I_O = 5 to 1000mA			0.5			0.5			0.5			0.5			0.5			0.5	mA
Dropout Voltage ΔV_O = 100mV		T_J = 25°C, K,R,P-Pkg: I_O = 1A		2.0			2.0			2.0			2.0			2.0			2.0		V
		T_J = 25°C, T-Pkg: I_O = 500mA		1.8			1.8			1.8			1.8			1.8			1.8		
Peak Output Current		T_J = 25°C, K,R,P-Pkg		2.5			2.5			2.5			2.5			2.5			2.5		A
		T_J = 25°C, T-Pkg		1.0			1.0			1.0			1.0			1.0			1.0		A
Short Circuit Current		T_J = 25°C, K,R,P-Pkg		1.5			1.5			1.5			1.5			1.5			1.5		A
		T_J = 25°C, T-Pkg		0.5			0.5			0.5			0.5			0.5			0.5		A
Temperature Coefficient		I_O = 5mA		−0.8			−0.8			−0.8			−0.8			−0.8			−0.8		mV /°C
Ripple Rejection		T_J = 25°C, f = 120Hz, ΔV_{IN} = 10V		65			65			65			65			65			65		dB
Output Noise Voltage		T_J = 25°C, f = 10Hz to 100 kHz		75			75			75			75			75			75		μV rms
Long Term Stability		1000 hrs. at T_J = 125°C		48			48			48			48			48			48		mV
Thermal Shutdown		I_O = 5mA		175			175			175			175			175			175		°C

NOTES:

1. Minimum load current for full line regulation is 5mA.
2. Maximum test current for T-Pkg is 500mA.
3. Unless otherwise specified, V_{IN} = 19V and I_O = 500mA for K,R,P-Pkg; I_O = 100mA for T-Pkg.
4. All regulation tests are made at constant junction temperature with low duty-cycle testing.
5. At T_J = −55°C, minimum (V_{IN} − V_O) = 2.5V.
6. Short circuit protection is only assured to V_{IN} = 35V.

DEVICE PART NUMBERS			SG7815A			SG140-15			SG7815			SG7815AC			SG340-15			SG7815C			
PACKAGE STYLES (P/N SUFFIX)			K,R,T			K,R,T			K,R,T			K,P,R,T			K,P,R,T			K,P,R,T			
OPERATING JUNCTION TEMPERATURE RANGE (Unless otherwise specified below)			−55°C to +150°C			−55°C to 150°C			−55°C to 150°C			0°C to 125°C			0°C to 125°C			0°C to 125°C			
PARAMETERS		**TEST CONDITIONS (See notes below)**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Output Voltage		T_J = 25°C	14.8		15.2	14.4		15.6	14.4		15.6	14.8		15.2	14.4		15.6	14.4		15.6	V
Line Regulation		T_J = 25°C, V_{IN} = 17.5 to 30V		15	75		15	150		15	150		15	150		15	150		30	300	mV
		T_J = 25°C, V_{IN} = 20 to 26V		8	40		8	75		8	75		8	75		8	75		15	150	mV
Load Regulation	P,R,K Pkg	T_J = 25°C, I_O = 5mA to 1.5A		30	100		30	150		30	150		30	150		30	150		100	300	mV
	P,R,K Pkg	T_J = 25°C, I_O = 250 to 750mA		12	50		12	75		12	75		12	75		12	75		30	150	mV
	T-Pkg	T_J = 25°C, I_O = 5mA to 500mA		12	50		12	75		12	75		12	75		12	75		30	150	mV
Total Output Voltage Tolerance V_{IN} = 18.5 to 30V		K-Pkg: I_O = 5 to 1.0A, P 20W	14.6		15.4	14.3		15.7	14.3		15.7	14.6		15.4	14.3		15.7	14.3		15.7	V
		R,P-Pkg: I_O = 5 to 1000mA, P ≤ 15W																			
		T-Pkg: I_O = 5 to 500mA, P ≤ 2W																			
Quiescent Current		T_J = 25°C		4	6		4	6		4	6		4	6		4	8		4	8	mA
		Over Temperature Range			7			7			7			7			8.5			8.5	mA
Quiescent Current Change		With line: V_{IN} = 18.5 to 30V			0.8			0.8			0.8			1.0			1.0			1.0	mA
		With load: I_O = 5 to 1000mA			0.5			0.5			0.5			0.5			0.5			0.5	mA
Dropout Voltage ΔV_O = 100mV		T_J = 25°C, K,R,P-Pkg: I_O = 1A		2			2			2			2			2			2		V
		T_J = 25°C, T-Pkg: I_O = 500mA		1.8			1.8			1.8			1.8			1.8			1.8		
Peak Output Current		T_J = 25°C, K,R,P-Pkg		2.2			2.2			2.2			2.2			2.2			2.2		A
		T_J = 25°C, T-Pkg		0.9			0.9			0.9			0.9			0.9			0.9		A
Short Circuit Current		T_J = 25°C, K,R,P-Pkg		1.3			1.3			1.3			1.3			1.3			1.3		A
		T_J = 25°C, T-Pkg		0.4			0.4			0.4			0.4			0.4			0.4		A
Temperature Coefficient		I_O = 5mA		−1.0			−1.0			−1.0			−1.0			−1.0			−1.0		mV /°C
Ripple Rejection		T_J = 25°C, f = 120Hz, ΔV_{IN} = 10V		64			64			64			64			64			64		dB
Output Noise Voltage		T_J = 25°C, f = 10Hz to 100 kHz		90			90			90			90			90			90		μV rms
Long Term Stability		1000 hrs. at T_J = 125°C		60			60			60			60			60			60		mV
Thermal Shutdown		I_O = 5mA		175			175			175			175			175			175		°C

NOTES:

1. Minimum load current for full line regulation is 5mA.
2. Maximum test current for T-Pkg is 500mA.
3. Unless otherwise specified, V_{IN} = 23V and I_O = 500mA for K,R,P-Pkg; I_O = 100mA for T-Pkg.
4. All regulation tests are made at constant junction temperature with low duty-cycle testing.
5. At T_J = −55°C, minimum (V_{IN} − V_O) = 2.5V.
6. Short circuit protection is only assured to V_{IN} = 35V.

DEVICE PART NUMBERS			SG7818A			SG140-18			SG7818			SG7818AC			SG340-18			SG7818C			
PACKAGE STYLES (P/N SUFFIX)			K,R,T			K,R,T			K,R,T			K,P,R,T			K,P,R,T			K,P,R,T			
OPERATING JUNCTION TEMPERATURE RANGE (Unless otherwise specified below)			−55°C to +150°C			−55°C to 150°C			−55°C to 150°C			0°C to 125°C			0°C to 125°C			0°C to 125°C			
PARAMETERS		**TEST CONDITIONS (See notes below)**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Output Voltage		T_J = 25°C	17.7		18.3	17.3		18.7	17.3		18.7	17.7		18.3	17.3		18.7	17.3		18.7	V
Line Regulation		T_J = 25°C, V_{IN} = 21 to 33V		20	90		20	180		20	180		20	180		20	180		40	360	mV
		T_J = 25°C, V_{IN} = 24 to 30V		20	45		10	90		10	90		10	90		10	90		20	180	mV
Load Regulation	P,R,K Pkg	T_J = 25°C, I_O = 5mA to 1.5A		40	120		40	180		40	180		40	180		40	180		120	360	mV
	P,R,K Pkg	T_J = 25°C, I_O = 250 to 750mA		15	60		15	90		15	90		15	90		15	90		40	180	mV
	T-Pkg	T_J = 25°C, I_O = 5mA to 500mA		15	60		15	90		15	90		15	90		15	90		40	180	mV
Total Output Voltage Tolerance V_{IN} = 22 to 33V		K-Pkg: I_O = 5 to 1.0A, P 20W	17.5		18.5	17.1		18.9	17.1		18.9	17.5		18.5	17.1		18.9	17.1		18.9	V
		R,P-Pkg: I_O = 5 to 1000mA, P ≤ 15W																			
		T-Pkg: I_O = 5 to 500mA, P ≤ 2W																			
Quiescent Current		T_J = 25°C		4	6		4	6		4	6		4	6		4	8		4	8	mA
		Over Temperature Range			7			7			7			7			8.5			8.5	mA
Quiescent Current Change		With line: V_{IN} = 22 to 33V			0.8			0.8			0.8			1.0			1.0			1.0	mA
		With load: I_O = 5 to 1000mA			0.5			0.5			0.5			0.5			0.5			0.5	mA
Dropout Voltage ΔV_O = 100mV		T_J = 25°C, K,R,P-Pkg: I_O = 1A		2.0			2.0			2.0			2.0			2.0			2.0		V
		T_J = 25°C, T-Pkg: I_O = 500mA		1.8			1.8			1.8			1.8			1.8			1.8		
Peak Output Current		T_J = 25°C, K,R,P-Pkg		2.2			2.2			2.2			2.2			2.2			2.2		A
		T_J = 25°C, T-Pkg		0.9			0.9			0.9			0.9			0.9			0.9		A
Short Circuit Current		T_J = 25°C, K,R,P-Pkg		1.0			1.0			1.0			1.0			1.0			1.0		A
		T_J = 25°C, T-Pkg		0.3			0.3			0.3			0.3			0.3			0.3		A
Temperature Coefficient		I_O = 5mA		−1.2			−1.2			−1.2			−1.2			−1.2			−1.2		mV /°C
Ripple Rejection		T_J = 25°C, f = 120Hz, ΔV_{IN} = 10V		62			62			62			62			62			62		dB
Output Noise Voltage		T_J = 25°C, f = 10Hz to 100 kHz		110			110			110			110			110			110		μV rms
Long Term Stability		1000 hrs. at T_J = 125°C		72			72			72			72			72			72		mV
Thermal Shutdown		I_O = 5mA		175			175			175			175			175			175		°C

NOTES:

1. Minimum load current for full line regulation is 5mA.
2. Maximum test current for T-Pkg is 500mA.
3. Unless otherwise specified, V_{IN} = 27V and I_O = 500mA for K,R,P-Pkg; I_O = 100mA for T-Pkg.
4. All regulation tests are made at constant junction temperature with low duty-cycle testing.
5. At T_J = −55°C, minimum (V_{IN} − V_O) = 2.5V.
6. Short circuit protection is only assured to V_{IN} = 35V.

DEVICE PART NUMBERS			SG7820A			SG140-20			SG7820			SG7820AC			SG340-20			SG7820C			
PACKAGE STYLES (P/N SUFFIX)			K,R,T			K,R,T			K,R,T			K,P,R,T			K,P,R,T			K,P,R,T			
OPERATING JUNCTION TEMPERATURE RANGE (Unless otherwise specified below)			−55°C to +150°C			−55°C to 150°C			−55°C to 150°C			0°C to 125°C			0°C to 125°C			0°C to 125°C			
PARAMETERS		**TEST CONDITIONS (See notes below)**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Output Voltage		T_J = 25°C	19.7		20.3	19.2		20.8	19.2		20.8	19.7		20.3	19.2		20.8	19.2		20.8	V
Line Regulation		T_J = 25°C, V_{IN} = 23 to 35V		22	100		22	200		22	200		22	200		22	200		44	400	mV
		T_J = 25°C, V_{IN} = 26 to 32V		12	50		12	100		12	100		12	100		12	100		24	200	mV
Load Regulation	P,R,K Pkg	T_J = 25°C, I_O = 5mA to 1.5A		45	140		45	200		45	200		45	200		45	200		150	400	mV
	P,R,K Pkg	T_J = 25°C, I_O = 250 to 750mA		20	70		20	100		20	100		20	100		20	100		50	200	mV
	T-Pkg	T_J = 25°C, I_O = 5mA to 500mA		20	70		20	100		20	100		20	100		20	100		50	200	mV
Total Output Voltage Tolerance V_{IN} = 24 to 35V		K-Pkg: I_O = 5 to 1.0A, P 20W	19.4		20.6	19.0		21.0	19.0		21.0	19.4		20.6	19.0		21.0	19.0		21.0	V
		R,P-Pkg: I_O = 5 to 1000mA, P ≤ 15W																			
		T-Pkg: I_O = 5 to 500mA, P ≤ 2W																			
Quiescent Current		T_J = 25°C		4	6		4	6		4	6		4	6		4	8		4	8	mA
		Over Temperature Range			7			7			7			7			8.5			8.5	mA
Quiescent Current Change		With line: V_{IN} = 24 to 35V			0.8			0.8			0.8			1.0			1.0			1.0	mA
		With load: I_O = 5 to 1000mA			0.5			0.5			0.5			0.5			0.5			0.5	mA
Dropout Voltage ΔV_O = 100mV		T_J = 25°C, K,R,P-Pkg: I_O = 1A		2.0			2.0			2.0			2.0			2.0			2.0		V
		T_J = 25°C, T-Pkg: I_O = 500mA		1.8			1.8			1.8			1.8			1.8			1.8		
Peak Output Current		T_J = 25°C, K,R,P-Pkg		2.2			2.2			2.2			2.2			2.2			2.2		A
		T_J = 25°C, T-Pkg		0.9			0.9			0.9			0.9			0.9			0.9		A
Short Circuit Current		T_J = 25°C, K,R,P-Pkg		0.9			0.9			0.9			0.9			0.9			0.9		A
		T_J = 25°C, T-Pkg		0.2			0.2			0.2			0.2			0.2			0.2		A
Temperature Coefficient		I_O = 5mA		−1.3			−1.3			−1.3			−1.3			−1.3			−1.3		mV /°C
Ripple Rejection		T_J = 25°C, f = 120Hz, ΔV_{IN} = 10V		60			60			60			60			60			60		dB
Output Noise Voltage		T_J = 25°C, f = 10Hz to 100 kHz		140			140			140			140			140			140		μV rms
Long Term Stability		1000 hrs. at T_J = 125°C		80			80			80			80			80			80		mV
Thermal Shutdown		I_O = 5mA		175			175			175			175			175			175		°C

NOTES:

1. Minimum load current for full line regulation is 5mA.
2. Maximum test current for T-Pkg is 500mA.
3. Unless otherwise specified, V_{IN} = 29V and I_O = 500mA for K,R,P-Pkg; I_O = 100mA for T-Pkg.
4. All regulation tests are made at constant junction temperature with low duty-cycle testing.
5. At T_J = −55°C, minimum (V_{IN} − V_O) = 2.5V.
6. Short circuit protection is only assured to V_{IN} = 35V.

DEVICE PART NUMBERS			SG7824A			SG140-24			SG7824			SG7824AC			SG340-24			SG7824C			
PACKAGE STYLES (P/N SUFFIX)			K,R,T			K,R,T			K,R,T			K,P,R,T			K,P,R,T			K,P,R,T			
OPERATING JUNCTION TEMPERATURE RANGE (Unless otherwise specified below)			−55°C to +150°C			−55°C to 150°C			−55°C to 150°C			0°C to 125°C			0°C to 125°C			0°C to 125°C			
PARAMETERS		**TEST CONDITIONS (See notes below)**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Output Voltage		T_J = 25°C	23.6		24.4	23.0		25.0	23.0		25.0	23.6		24.4	23.0		25.0	23.0		25.0	V
Line Regulation		T_J = 25°C, V_{IN} = 27 to 38V		25	120		25	240		25	240		25	240		25	240		50	480	mV
		T_J = 25°C, V_{IN} = 30 to 36V		14	60		14	120		14	120		14	120		14	120		28	240	mV
Load Regulation	P,R,K Pkg	T_J = 25°C, I_O = 5mA to 1.5A		50	160		50	240		50	240		50	240		50	240		180	480	mV
	P,R,K Pkg	T_J = 25°C, I_O = 250 to 750mA		25	80		25	120		25	120		25	120		25	120		70	240	mV
	T-Pkg	T_J = 25°C, I_O = 5mA to 500mA		25	80		25	120		25	120		25	120		25	120		70	240	mV
Total Output Voltage Tolerance V_{IN} = 28 to 38V		K-Pkg: I_O = 5 to 1.0A, P 20W	23.3		24.7	22.8		25.2	22.8		25.2	23.3		24.7	22.8		25.2	22.8		25.2	V
		R,P-Pkg: I_O = 5 to 1000mA, P ≤ 15W																			
		T-Pkg: I_O = 5 to 500mA, P ≤ 2W																			
Quiescent Current		T_J = 25°C		4	6		4	6		4	6		4	6		4	8		4	8	mA
		Over Temperature Range			7			7			7			7			8.5			8.5	mA
Quiescent Current Change		With line: V_{IN} = 28 to 38V			0.8			0.8			0.8			1.0			1.0			1.0	mA
		With load: I_O = 5 to 1000mA			0.5			0.5			0.5			0.5			0.5			0.5	mA
Dropout Voltage ΔV_O = 100mV		T_J = 25°C, K,R,P-Pkg: I_O = 1A		2.0			2.0			2.0			2.0			2.0			2.0		V
		T_J = 25°C, T-Pkg: I_O = 500mA		1.8			1.8			1.8			1.8			1.8			1.8		
Peak Output Current		T_J = 25°C, K,R,P-Pkg		2.2			2.2			2.2			2.2			2.2			2.2		A
		T_J = 25°C, T-Pkg		0.9			0.9			0.9			0.9			0.9			0.9		A
Short Circuit Current		T_J = 25°C, K,R,P-Pkg		0.7			0.7			0.7			0.7			0.7			0.7		A
		T_J = 25°C, T-Pkg		0.2			0.2			0.2			0.2			0.2			0.2		A
Temperature Coefficient		I_O = 5mA		−1.5			−1.5			−1.5			−1.5			−1.5			−1.5		mV /°C
Ripple Rejection		T_J = 25°C, f = 120Hz, ΔV_{IN} = 10V		56			56			56			56			56			56		dB
Output Noise Voltage		T_J = 25°C, f = 10Hz to 100 kHz		170			170			170			170			170			170		μV rms
Long Term Stability		1000 hrs. at T_J = 125°C		96			96			96			96			96			96		mV
Thermal Shutdown		I_O = 5mA		175			175			175			175			175			175		°C

NOTES:

1. Minimum load current for full line regulation is 5mA.
2. Maximum test current for T-Pkg is 500mA.
3. Unless otherwise specified, V_{IN} = 33V and I_O = 500mA for K,R,P-Pkg; I_O = 100mA for T-Pkg.
4. All regulation tests are made at constant junction temperature with low duty-cycle testing.
5. At T_J = −55°C, minimum (V_{IN} − V_O) = 2.5V.
6. Short circuit protection is only assured to V_{IN} = 40V

Silicon General
LINEAR INTEGRATED CIRCUITS

SG7900A/7900AC
SG120/220/320
SG7900/7900C

THREE TERMINAL NEGATIVE REGULATORS

DESCRIPTION

The SG7900A/7900/120/220/320 series of negative regulators offer self-contained, fixed-voltage capability with up to 1.5 amps of load current. With a variety of output voltages and four package options this regulator series is an optimum complement to the SG7800A/7800/140/240/340 line of three terminal regulators.

These units feature a unique band gap reference which allows the SG7900A series to be specified with an output voltage tolerance of ±1.5%. The SG7900A versions also offer much improved line regulation characteristics.

All protective features of thermal shutdown, current limiting, and safe-area control have been designed into these units and since these regulators require only a single output capacitor (7900 series) or a capacitor and 5 mA minimum load (SG120 series) for satisfactory performance, ease of application is assured.

Although designed as fixed-voltage regulators, the output voltage can be increased through the use of a simple voltage divider. The low quescent drain current of the device insures good regulation when this method is used, especially for the SG120 series.

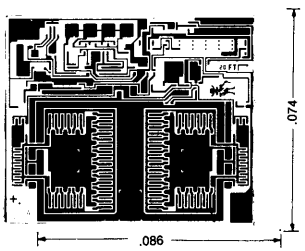
These devices are available in hermetically sealed TO-3, TO-39 and TO-66 power packages as well as the plastic comercial power TO-220 package.

Silicon General specializes in testing parts for unique customer requirements. If certain parameters are required for your application, contact factory for testing to your specification.

FEATURES

- **Output voltages set internally to ±1.5% (SG7900A)**
- **Output current to 1.5 amp**
- **Excellent line and load regulation**
- **Foldback current limiting**
- **Thermal overload protection**
- **Voltages available — −5 V, −5.2V, −8V, −12V, −15V, −18V, −20V**
- **Contact factory for other voltage options.**

CHIP LAYOUT



ABSOLUTE MAXIMUM RATINGS

Device Output Voltage	Input Voltage	Input-Output Differential
−5V	−35V	25V
−5.2V	−35V	25V
−8 V	−35V	30V
−12V	−35V	30V
−15V	−40V	30V
−18V	−40V	30V
−20V	−40V	35V

Operating Junction Temperature Range
SG7900A/7900/120 ..... −55°C to +150°C
SG220 ..... 0°C to +150°C
SG7900AC/7900/320 ..... 0°C to +125°C

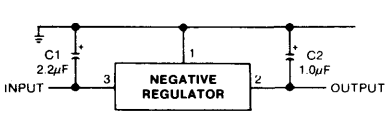
Storage Temperature Range ..... −65°C to +150°C
Lead Temperature (Soldering, 10 Sec) ..... +300°C

Power/Thermal Characteristics

Package	K (TO-3)	R (TO-66)	P (TO-220)	T (TO-39)
25°C Case Rated Power	20W	15W	15W	2W
25°C Ambient Rated Power	4.3W	3.0W	2.0W	1.0W
Design Current	1.5A	1.5A	1.0A	0.5A
Therm. Res θJC (°C/W)	3.0	5.0	3.0	15
θJA (°C/W)	35	40	60	120

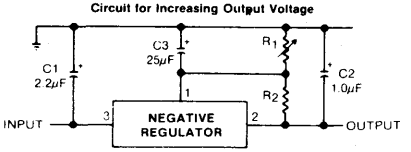
APPLICATIONS

Fixed Output Regulator



NOTE: 1. C1 is required only if regulator is separated from rectifier filter.
2. Both C1 and C2 should be low E.S.R. types such as solid tantalum. If aluminum electrolitics are used, at least 10 times values shown should be selected.
3. If large output capacities are used, the regulators must be protected from momentary input shorts. A high current diode from output to input will suffice.

Circuit for Increasing Output Voltage

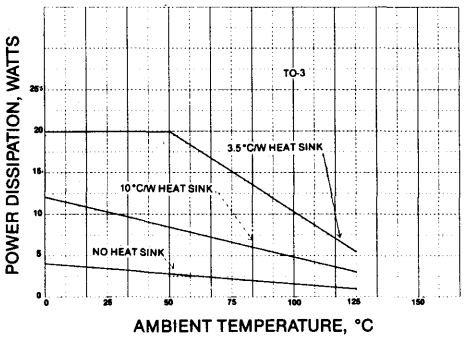


NOTE: C3 optional for improved transient response and ripple rejection.

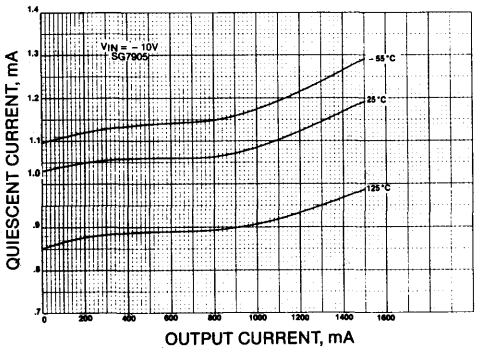
V_{OUT} V(REGULATOR) $\frac{R_1 + R_2}{R_1}$ R_2 $\frac{V(REG)}{15mA}$

TYPICAL PERFORMANCE CHARACTERISTICS

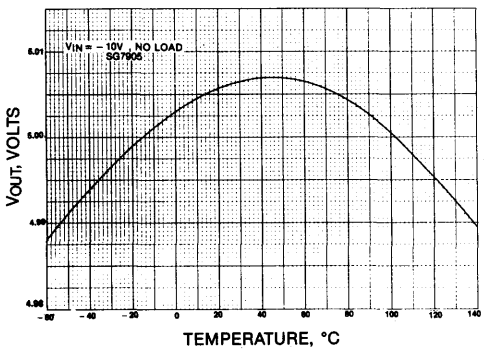
MAXIMUM AVERAGE POWER DISSIPATION



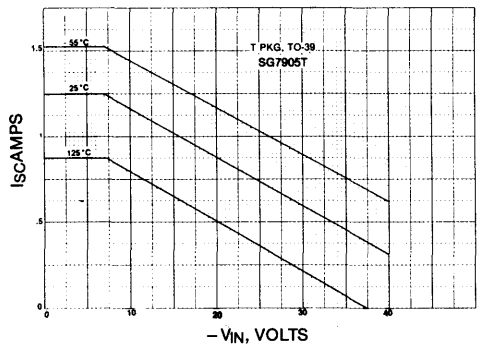
QUIESCENT CURRENT vs. LOAD



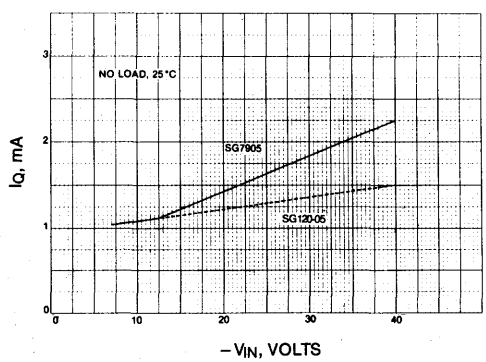
TEMPERATURE COEFFICIENT



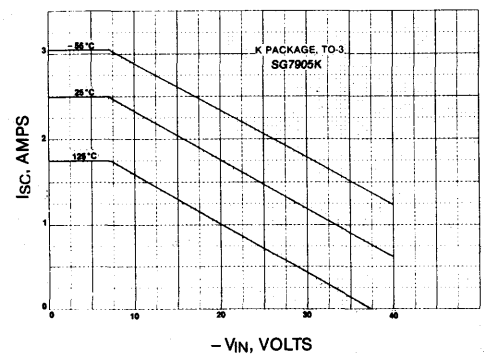
SHORTCIRCUIT CURRENT vs. VIN



QUIESCENT CURRENT vs. VIN

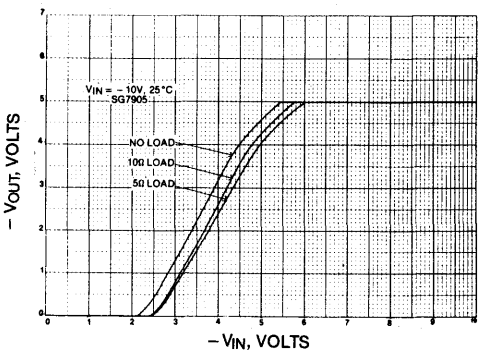


SHORT CIRCUIT CURRENT vs. VIN

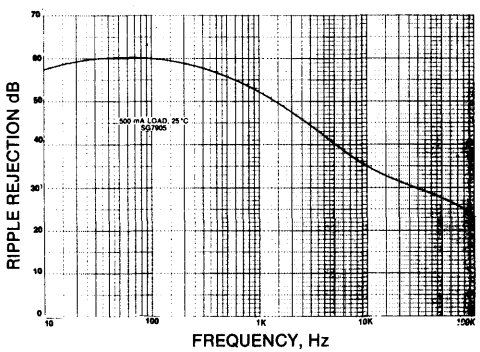


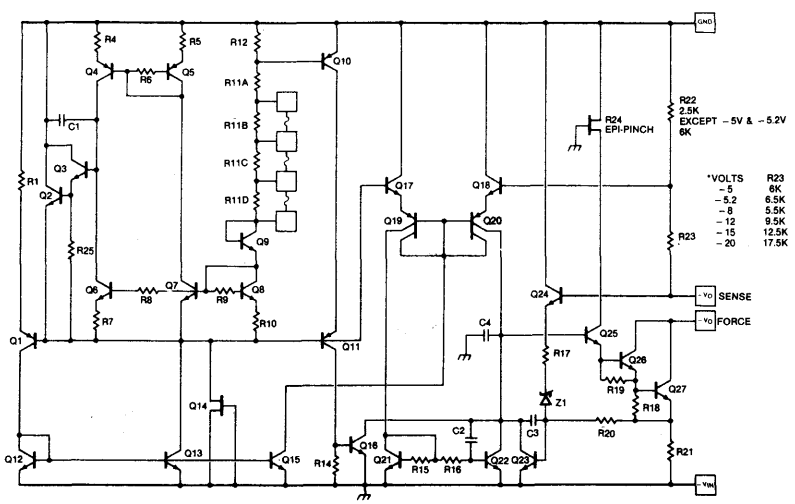
1

DROPOUT CHARACTERISTICS

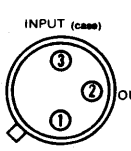


RIPPLE REJECTION vs. FREQ.





PACKAGE ORDER INFORMATION



T-Package TO-39

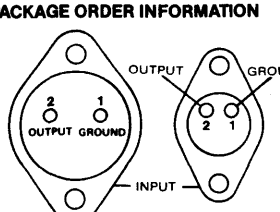
SG79XXAT
SG79XXT

SG120XXT
SG220XXT
SG320XXT

K-Package TO-3
TOP VIEWS

SG79XXAK
SG79XXK

SG120XXK
SG220XXK
SG320XXK



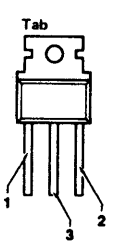
K-Package TO-3
TOP VIEWS

R-Package TO-66

SG79XXAR
SG79XXR
SG120XXR
SG220XXR
SG320XXR

PACKAGES
P-Package TO-220
Front View
1 - Ground
2 - Output
3 - Input
Tab - Input

SG79XXACP
SG79XXCP
SG320XXP



DEVICE PART NUMBERS			SG7905A			SG120-05			SG7905			SG7905AC			SG320-05			SG7905C			
PACKAGE STYLES (P/N SUFFIX)			K,R,T			K,R,T			K,R,T			K,P,R,T			K,P,R,T			K,P,R,T			
OPERATING JUNCTION TEMPERATURE RANGE (Unless otherwise specified below)			−55°C to 150°C			−55°C to 150°C			−55°C to 150°C			0°C to 125°C			0°C to 125°C			0°C to 125°C			
PARAMETERS	**TEST CONDITIONS (See notes below)**		**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Output Voltage	T_J = 25°C		−4.92	−5.0	−5.08	−4.9	−5.0	−5.1	−4.8	−5.0	−5.2	−4.92	−5.0	−5.08	−4.8	−5.0	−5.2	−4.8	−5.0	−5.2	V
Line Regulation (Note 7)	T_J = 25°C	V_{IN} = −7 to −25V		5	25		10	25		3	50		5	40		10	40		3	100	mV
		V_{IN} = −8 to −12V		3	15					1	25		3	25					1	50	mV
Load Regulation P,R,K Pkg.	T_J = 25°C	I_O = 5mA to 1.5A		15	75		50	75		15	100		15	75		50	100		15	100	mV
		I_O = 250 to 750mA		15	25					5	25		5	50					5	50	mV
Load Regulation T-Pkg.		I_O = 5mA to 500mA		5	40		30	50		5	100		5	50		30	50		15	100	mV
Total Output Voltage Tolerance V_{IN} = −8 to −20V	K,R,P-Pkg: I_O = 5 to 1000mA, P ≤ 15W		−4.85		−5.15	−4.8		−5.2	−4.70		−5.30	−4.85		−5.15	−4.75		−5.25	−4.75		−5.25	V
	T-Pkg: I_O = 5 to 500mA, P ≤ 2W																				
Quiescent Current	T_J = 25°C			1	2		1	2		1	2		1	2		1	2		1	2	mA
	Over Temperature Range				2.0			2.0			2.5			2.0			2.0			3	mA
Quiescent Current Change	With line: V_{IN} = −7 to −25V				1.3			0.4			1.3			1.3			0.4			1.3	mA
	With load: I_O = 5 to 1000mA				0.5			0.4			0.5			0.5			0.4			0.5	mA
Dropout Voltage ΔV_O = 100mV	T_J = 25°C	K,R,P-Pkg.: I_O = 1A		1.1	2.0		1.1	2.0		1.1	2.0		1.1	2.0		1.1	2.0		1.1	2.0	V
		T-Pkg: I_O = 100mA		1.1	2.0		1.1	2.0		1.1	2.0		1.1	2.0		1.1	2.0		1.1	2.0	
Peak Output Current	T_J = 25°C	K,R,P-Pkg.:	1.5	2.1	3.3	1.5	2.5	3.3	1.5	2.1	3.3	1.5	2.5	3.3	1.5	2.5	3.3	1.5	2.1	3.3	A
		T-Pkg:	0.5	1.0		0.5	1.0		0.5	1.0		0.5	1.0		0.5	1.0		0.5	1.0		A
Short Circuit Current	T_J = 25°C	K,R,P-Pkg.:		2.1			2.1			2.1			2.1			2.1			2.1		A
		T-Pkg:		0.7			0.7			0.7			0.7			0.7			0.7		A
Ripple Rejection	T_J = 25°C, f = 120Hz, ΔV_{IN} = 10V		54	60		54	60		54	60		54	60		54	60		54	60		dB
Output Noise Voltage	T_J = 25°C, f = 10Hz to 100 kHz			25	80		150			25	80		125			150			125		μV rms
Long Term Stability	1000 hrs at T_J = 125°C			20			5	50		20			20			5	50		20		mV
Thermal Shutdown	I_O = 5mA			175			175			175			175			175			175		°C

NOTES:

1. Minimum load current for full line regulation is 5mA. (SG120/220/320 only)
2. Maximum test current for T-Pkg. is 500mA.
3. Unless otherwise specified, V_{IN} = −10V and I_O = 500mA for K,R,P-Package (SG7900 Series). I_O = 1A for K,R,P Pkg (SG120 Series), I_O = 100mA for T-Pkg. C_{IN} = 2μF, C_{OUT} = 1μF.
4. All regulation tests are made at constant junction temperature with low duty-cycle testing.
5. At T_J = −55°C, minimum (V_{IN} − V_O) = 2.5V.
6. Short circuit protection is only assured to V_{IN} = −35V.
7. Line regulation @ I_O = 5mA = 10mV (120-05) and 20mV (320-05).

DEVICE PART NUMBERS			SG7905.2A			SG120-5.2			SG7905.2			SG7905.2AC			SG320-5.2			SG7905.2C			
PACKAGE STYLES (P/N SUFFIX)			K,R,T			K,R,T			K,R,T			K,P,R,T			K,P,R,T			K,P,R,T			
OPERATING JUNCTION TEMPERATURE RANGE (Unless otherwise specified below)			−55°C to 150°C			−55°C to 150°C			−55°C to 150°C			0°C to 125°C			0°C to 125°C			0°C to 125°C			
PARAMETERS	**TEST CONDITIONS (See notes below)**		**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Output Voltage	T_J = 25°C		−5.12	−5.2	−5.28	−5.1	−5.2	−5.3	−5.0	−5.2	−5.4	−5.12	−5.2	−5.28	−5.0	−5.2	−5.4	−5.0	−5.2	−5.4	V
Line Regulation (Note 7)	T_J = 25°C	V_{IN} = −8 to −25V		5	25		5	25		5	50		5	40		5	40		10	50	mV
		V_{IN} = −9 to −13V		3	15		3	15		3	25		3	25		3	25		5		
Load Regulation P,R,K Pkg.	T_J = 25°C	I_O = 5mA to 1.5A		15	75		15	75		15	100		15	75		15	100		15	100	mV
		I_O = 250 to 750mA		5	30		5	30		5	30		5	50		5	50		5	50	mV
Load Regulation T-Pkg.	T_J = 25°C	I_O = 5mA to 500mA		5	50		5	50		5	50		5	50		5	50		5	100	mV
Total Output Voltage Tolerance V_{IN} = −9 to −21V	K,R,P-Pkg: I_O = 5 to 1000mA, P ≤ 15W		−5.05		−5.35	−5.00		−5.40	−4.90		−5.50	−5.05		−5.35	−4.95		−5.45	−4.95		−5.45	V
	T-Pkg: I_O = 5 to 500mA, P ≤ 2W																				
Quiescent Current	T_J = 25°C			1	2		1	2		1	2		1	2		1	2		1	2	mA
	Over Temperature Range				2.0			2.0			2.5			2.0			2.0			3.0	mA
Quiescent Current Change	With line: V_{IN} = 9 to −25V				1.3			0.4			1.3			1.3			0.4			1.3	mA
	With load: I_O = 5 to 1000mA				0.5			0.4			0.5			0.5			0.4			0.5	mA
Dropout Voltage ΔV_O = 100mV	T_J = 25°C	K,R,P-Pkg.: I_O = 1A		1.1	2.3					1.1	2.3		1.1	2.3					1.1	2.3	V
		T-Pkg: I_O = 500mA		1.1	2.3		1.1	2.3		1.1	2.3		1.1	2.3		1.1	2.3		1.1	2.3	
Peak Output Current	T_J = 25°C	K,R,P-Pkg.:	1.5	2.1	3.3	1.5	2.5	3.3	1.5	2.5	3.3	1.5	2.5	3.3	1.5	2.5	3.3	1.5	2.1	3.3	A
		T-Pkg:	0.5	1.0		0.5	1.0		0.5	1.0		0.5	1.0		0.5	1.0		0.5	1.0		A
Short Circuit Current	T_J = 25°C	K,R,P-Pkg.:		2.0			2.0			2.0			2.0			2.0			2.0		A
		T-Pkg:		0.6			0.6			0.6			0.6			0.6			0.6		A
Ripple Rejection	T_J = 25°C, f = 120Hz, ΔV_{IN} = 10V		54	60		54	60		54	60		54	60		54	60		54	60		dB
Output Noise Voltage	T_J = 25°C, f = 10Hz to 100 kHz			25	80		150			25	80		25	80		150		25	80		μV rms
Long Term Stability	1000 hrs at T_J = 125°C			24			5	50		24			24			5	50		24		mV
Thermal Shutdown	I_O = 5mA			175			175			175			175			175			175		°C

NOTES:

1. Minimum load current for full line regulation is 5mA. (SG120/220/320 only)
2. Maximum test current for T-Pkg. is 500mA.
3. Unless otherwise specified, V_{IN} = −10V and I_O = 500mA for K,R,P-Package (7900 Series). I_O = 1A for K,R,P Pkg (120 Series), I_O = 100mA for T-Pkg. C_{IN} = 2μF, C_{OUT} = 1μF.
4. All regulation tests are made at constant junction temperature with low duty-cycle testing.
5. At T_J = −55°C, minimum (V_{IN} − V_O) = 2.5V.
6. Short circuit protection is only assured to V_{IN} = −35V.
7. Line regulation @ I_O = 5mA = 10 mV (120-5.2) and 20mV (320-5.2).

DEVICE PART NUMBERS			SG7908A			SG120-08			SG7908			SG7908AC			SG320-08			SG7908C			
PACKAGE STYLES (P/N SUFFIX)			K,R,T			K,R,T			K,R,T			K,P,R,T			K,P,R,T			K,P,R,T			
OPERATING JUNCTION TEMPERATURE RANGE (Unless otherwise specified below)			−55°C to 150°C			−55°C to 150°C			−55°C to 150°C			0°C to 125°C			0°C to 125°C			0°C to 125°C			
PARAMETERS	TEST CONDITIONS (See notes below)		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Output Voltage	T_J = 25°C		−7.88	−8.0	−8.12	−7.8	−8.0	−8.2	−7.7	−8.0	−8.3	−7.88	−8.0	−8.12	−7.7	−8.0	−8.3	−7.7	−8.0	−8.3	V
Line Regulation (Note 7)	T_J = 25°C	V_{IN} = −10.5 to −25V		6	25		10	25		6	80		6	40		10	40		6	160	mV
		V_{IN} = −11 to −17V		2	15					2	40		4	25					2	80	mV
Load Regulation P,R,K Pkg.	T_J = 25°C	I_O = 5mA to 1.5A		12	80		20	80		12	100		20	100		20	100		12	160	mV
		I_O = 250 to 750mA		4	40					4	40		10	50					4	80	mV
Load Regulation T-Pkg.		I_O = 5mA to 500mA		10	25		10	25		10	80		10	40		10	40		10	160	mV
Total Output Voltage Tolerance V_{IN} = −11.5 to −23V	K,R,P-Pkg: I_O = 5 to 1000mA, P ≤ 15W		−7.76		−8.24	−7.65		−8.35	−7.60		−8.40	−7.76		−8.24	−7.60		−8.40	−7.60		−8.40	V
	T-Pkg: I_O = 5 to 500mA, P ≤ 2W																				
Quiescent Current	T_J = 25°C			1	2		1	2		1	2		1	2		1	2		1	2	mA
	Over Temperature Range				2.5			2.5			2.5			2.5			2.5			2.5	mA
Quiescent Current Change	With line: V_{IN} = −11.5 to −25V				1.0			0.4			1.0			1.0			0.4			1.0	mA
	With load: I_O = 5 to 1000mA				0.5			0.4			0.5			0.5			0.4			0.5	mA
Dropout Voltage ΔV_O = 500mV	T_J = 25°C	K,R,P-Pkg.: I_O = 1A		1.1	2.3		1.1	2.3		1.1	2.3		1.1	2.3		1.1	2.3		1.1	2.3	V
		T-Pkg: I_O = 500mA		1.0	2.3		1.0	2.3		1.0	2.3		1.0	2.3		1.0	2.3		1.0	2.3	V
Peak Output Current	T_J = 25°C	K,R,P-Pkg.:	1.5	2.1	3.3	1.5	2.1	3.3	1.5	2.1	3.3	1.5	2.1	3.3	1.5	2.1	3.3	1.5	2.1	3.3	A
		T-Pkg:	0.5	1.0		0.5	1.0		0.5	1.0		0.5	1.0		0.5	1.0		0.5	1.0		A
Short Circuit Current	T_J = 25°C	K,R,P-Pkg.:		1.5			1.5			1.5			1.5			1.5			1.5		A
		T-Pkg:		0.5			0.5			0.5			0.5			0.5			0.5		A
Ripple Rejection	T_J = 25°C, f = 120Hz, ΔV_{IN} = 10V		54	60		54	60		54	60		54	60		54	60		54	60		dB
Output Noise Voltage	T_J = 25°C, f = 10Hz to 100 kHz			25	80		150			25	80		200			150			200		μV rms
Long Term Stability	1000 hrs at T_J = 125°C			32			5	50		32			32			5	50		32		mV
Thermal Shutdown	I_O = 5mA			175			175			175			175			175			175		°C

NOTES:

1. Minimum load current for full line regulation is 5mA. (SG120/220/320 only)
2. Maximum test current for T-Pkg. is 500mA.
3. Unless otherwise specified, V_{IN} = −14V and I_O = 500mA for K,R,P-Package (SG7900 Series). I_O = 1A for K,R,P Pkg (SG120 Series), I_O = 100mA for T-Pkg. C_{IN} = 2μF, C_{OUT} = 1μF.
4. All regulation tests are made at constant junction temperature with low duty-cycle testing.
5. At T_J = −55°C, minimum (V_{IN} − V_O) = 2.5V.
6. Short circuit protection is only assured to V_{IN} = −35V.
7. Line regulation @I_O = 5mA = 10 mV (120-08) and 20mV (320-08).

DEVICE PART NUMBERS			SG7912A			SG120-12			SG7912			SG7912AC			SG320-12			SG7912C			
PACKAGE STYLES (P/N SUFFIX)			K,R,T			K,R,T			K,R,T			K,P,R,T			K,P,R,T			K,P,R,T			
OPERATING JUNCTION TEMPERATURE RANGE (Unless otherwise specified below)			−55°C to 150°C			−55°C to 150°C			−55°C to 150°C			0°C to 125°C			0°C to 125°C			0°C to 125°C			
PARAMETERS	**TEST CONDITIONS (See notes below)**		**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Output Voltage	T_J = 25°C		−11.8	−12.0	−12.2	−11.7	−12.0	−12.3	−11.5	−12.0	−12.5	−11.8	−12.0	−12.2	−11.6	−12.0	−12.4	−11.5	−12.0	−12.5	V
Line Regulation (Note 7)	T_J = 25°C	V_{IN} = −14.5 to −30V		4	10		4	10		10	120		4	20		4	20		10	240	mV
		V_{IN} = −16 to −22V		3	8					3	60		3	16					3	120	mV
Load Regulation P,R,K Pkg.	T_J = 25°C	I_O = 5mA to 1.5A		20	80		4	10		12	120		20	80		4	20		12	240	mV
		I_O = 250 to 750mA		10	40					4	60		10	40					4	120	mV
Load Regulation T-Pkg.		I_O = 5mA to 500mA		10	25		10	25		10	120		10	40		10	40		10	240	mV
Total Output Voltage Tolerance V_{IN} = −15.5 to −27V	K,R,P-Pkg: I_O = 5 to 1000mA, P ≤ 15W		−11.7		−12.3	−11.5		−12.5	−11.4		−12.6	−11.7		−12.3	−11.4		−12.6	−11.4		−12.6	V
	T-Pkg: I_O = 5 to 500mA, P ≤ 2W																				
Quiescent Current	T_J = 25°C			1.5	3		1.5	3		1.5	3		1.5	3		1.5	3		1.5	3	mA
	Over Temperature Range				4			4			4			4			4			4	mA
Quiescent Current Change	With line: V_{IN} = −15 to −30V				1.0		0.1	0.4			1.0			1.0		0.1	0.4			1.0	mA
	With load: I_O = 5 to 1000mA				0.5		0.1	0.4			0.5			0.5		0.1	0.4			0.5	mA
Dropout Voltage ΔV_O = 100mV	T_J = 25°C	K,R,P-Pkg.: I_O = 1A		1.1	2.3		1.1	2.3		1.1	2.3		1.1	2.3		1.1	2.3		1.1	2.3	V
		T-Pkg: I_O = 100mA		1.1	2.3		1.1	2.3		1.1	2.3		1.1	2.3		1.1	2.3		1.1	2.3	V
Peak Output Current	T_J = 25°C	K,R,P-Pkg.:	1.5	2.1	3.3	1.5	2.1	3.3	1.5	2.1	3.3	1.5	2.1	3.3	1.5	2.1	3.3	1.5	2.1	3.3	A
		T-Pkg:	0.5	1.0		0.5	1.0		0.5	1.0		0.5	1.0		0.5	1.0		0.5	1.0		A
Short Circuit Current	T_J = 25°C	K,R,P-Pkg.:		1.2			1.5			1.2			1.2			1.5			1.2		A
		T-Pkg:		0.5			0.5			0.5			0.5			0.5			0.5		A
Ripple Rejection	T_J = 25°C, f = 120Hz, ΔV_{IN} = 10V		56	60		56	60		54	60		54	60		56	60		54	60		dB
Output Noise Voltage	T_J = 25°C, f = 10Hz to 100 kHz			25	80		400			25	80		300			400			300		μV rms
Long Term Stability	1000 hrs at T_J = 125°C			48			12	120		48			48			12	120		48		mV
Thermal Shutdown	I_O = 5mA			175			175			175			175			175			175		°C

NOTES:

1. Minimum load current for full line regulation is 5mA. (SG120/220/320 only)
2. Maximum test current for T-Pkg. is 500mA.
3. Unless otherwise specified, V_{IN} = −9V and I_O = 500mA for K,R,P-Package. (7900 Series). I_O = 1A for K,R,P Pkg (120 Series), I_O = 100mA for T-Pkg. C_{IN} = 2μF, C_{OUT} = 1μF.
4. All regulation tests are made at constant junction temperature with low duty-cycle testing.
5. At T_J = −55°C, minimum (V_{IN} − V_O) = 2.5V.
6. Short circuit protection is only assured to V_{IN} = −35V.
7. Line regulation @ I_O = 5 mA = 10mV (120-12) and 20mV (320-12).

DEVICE PART NUMBERS			SG7915A			SG120-15			SG7915			SG7915AC			SG320-15			SG7915C			
PACKAGE STYLES (P/N SUFFIX)			K,R,T			K,R,T			K,R,T			K,P,R,T			K,P,R,T			K,P,R,T			
OPERATING JUNCTION TEMPERATURE RANGE (Unless otherwise specified below)			−55°C to 150°C			−55°C to 150°C			−55°C to 150°C			0°C to 125°C			0°C to 125°C			0°C to 125°C			
PARAMETERS	**TEST CONDITIONS (See notes below)**		**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Output Voltage	T_J = 25°C		−14.8	−15.0	−15.2	−14.7	−15.0	−15.3	−14.4	−15.0	−15.6	−14.8	−15.0	−15.2	−14.6	−15.0	−15.4	−14.4	−15.0	−15.6	V
Line Regulation (Note 7)	T_J = 25°C	V_{IN} = −17.5 to −30V		5	10		5	10		11	150		5	20		5	20		12	300	mV
		V_{IN} = −20 to −25V		3	8					3	75		4	16					3	150	mV
Load Regulation P,R,K Pkg.	T_J = 25°C	I_O = 5mA to 1.5A		30	80		30	80		12	150		30	80		30	80		12	300	mV
		I_O = 250 to 750mA		4	40					4	75		4	40					4	150	mV
Load Regulation T-Pkg.	T_J = 25°C	I_O = 5mA to 500mA		10	25		10	25		10	120		10	40		10	40		10	240	mV
Total Output Voltage Tolerance V_{IN} = −18.5 to −30V	K,R,P-Pkg: I_O = 5 to 1000mA, P ≤ 15W		−14.6		−15.4	−14.5		−15.5	−14.25		−15.75	−14.6		−15.4	−14.4		−15.6	−14.25		−15.75	V
	T-Pkg: I_O = 5 to 500mA, P ≤ 2W																				
Quiescent Current	T_J = 25°C			1.5	3		1.5	3		1.5	3		1.5	3		1.5	3		1.5	3	mA
	Over Temperature Range				4		2	4			4			4		2	4			4	mA
Quiescent Current Change	With line: V_{IN} = 22 to −33V				1.0		0.1	0.4			1.0			1.0		0.1	0.4			1.0	mA
	With load: I_O = 5 to 1000mA				0.5		0.1	0.4			0.5			0.5		0.1	0.4			0.5	mA
Dropout Voltage ΔV_O = 100mV	T_J = 25°C	K,R,P-Pkg.: I_O = 1A		1.1	2.3		1.1	2.3		1.1	2.3		1.1	2.3		1.1	2.3		1.1	2.3	V
		T-Pkg: I_O = 500mA		1.1	2.3		1.1	2.3		1.1	2.3		1.1	2.3		1.1	2.3		1.1	2.3	V
Peak Output Current	T_J = 25°C	K,R,P-Pkg.:	1.5	2.1	3.3	1.5	2.1	3.3	1.5	2.1	3.3	1.5	2.1	3.3	1.5	2.1	3.3	1.5	2.1	3.3	A
		T-Pkg:	0.5	0.9		0.5	0.9		0.5	0.9		0.5	0.9		0.5	0.9		0.5	0.9		A
Short Circuit Current	T_J = 25°C	K,R,P-Pkg.:		1.3			1.3			1.3			1.3			1.3			1.3		A
		T-Pkg:		0.4			0.4			0.4			0.4			0.4			0.4		A
Ripple Rejection	T_J = 25°C, f = 120Hz, ΔV_{IN} = 10V		54	60		56	60		54	60		54	60		56	60		54	60		dB
Output Noise Voltage	T_J = 25°C, f = 10Hz to 100 kHz			25	80		400			25	80		375			400			375		μV rms
Long Term Stability	1000 hrs at T_J = 125°C			60			15	150		60			60			15	150		60		mV
Thermal Shutdown	I_O = 5mA			175			175			175			175			175			175		°C

NOTES:

1. Minimum load current for full line regulation is 5mA. (SG120/220/320 only)
2. Maximum test current for T-Pkg. is 500mA.
3. Unless otherwise specified, V_{IN} = −23V and I_O = 500mA for K,R,P-Package (SG7900 Series). I_O = 1A for K,R,P Pkg (SG120 Series), I_O = 100mA for T-Pkg. C_{IN} = 2μF, C_{OUT} = 1μF.
4. All regulation tests are made at constant junction temperature with low duty-cycle testing.
5. At T_J = −55°C, minimum (V_{IN} − V_O) = 2.5V.
6. Short circuit protection is only assured to V_{IN} = −35V.
7. Line regulation @ I_O = 5mA = 10mV (120-15) and 20mV (320-15).

DEVICE PART NUMBERS			SG7918A			SG120-18			SG7918			SG7918AC			SG320-18			SG7918C			
PACKAGE STYLES (P/N SUFFIX)			K,R,T			K,R,T			K,R,T			K,P,R,T			K,P,R,T			K,P,R,T			
OPERATING JUNCTION TEMPERATURE RANGE (Unless otherwise specified below)			−55°C to 150°C			−55°C to 150°C			−55°C to 150°C			0°C to 125°C			0°C to 125°C			0°C to 125°C			
PARAMETERS	**TEST CONDITIONS (See notes below)**		**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Output Voltage	T_J = 25°C		−17.7	−18.0	−18.3	−17.6	−18.0	−18.4	−17.3	−18.0	−18.7	−17.7	−18.0	−18.3	−17.4	−18.0	−18.6	−17.4	−18.0	−18.6	V
Line Regulation (Note 7)	T_J = 25°C	V_{IN} = −21 to −33V		5	10		5	10		6	180		5	20		5	20		12	300	mV
		V_{IN} = −24 to −30V		3	8					3	75		4	16					3	150	mV
Load Regulation P,R,K Pkg.	T_J = 25°C	I_O = 5mA to 1.5A		30	80		30	80		12	180		30	80		30	80		12	360	mV
		I_O = 250 to 750mA		4	40					4	90		4	40					4	180	mV
Load Regulation T-Pkg.		I_O = 5mA to 500mA		10	25		10	25		10	120		10	40		10	40		10	300	mV
Total Output Voltage Tolerance V_{IN} = −22 to −33V	K,R,P-Pkg: I_O = 5 to 1000mA, P ≤ 15W		−17.5		−18.5	−17.4		−18.6	−17.1		−18.9	−17.5		−18.5	−17.1		−18.9	−17.1		−18.9	V
	T-Pkg: I_O = 5 to 500mA, P ≤ 2W																				
Quiescent Current	T_J = 25°C			1.5	3		1.5	3		1.5	3		1.5	3		1.5	3		1.5	3	mA
	Over Temperature Range				4		2	4			4			4		2	4			4	mA
Quiescent Current Change	With line: V_{IN} = −18.5 to −30V				1.0		0.1	0.4			1.0			1.0		0.1	0.4			1.0	mA
	With load: I_O = 5 to 100mA				0.5		0.1	0.4			0.5			0.5		0.1	0.4			0.5	mA
Dropout Voltage ΔV_O = 100mV	T_J = 25°C	K,R,P-Pkg.: I_O = 1A		1.1	2.3		1.1	2.3		1.1	2.3		1.1	2.3		1.1	2.3		1.1	2.3	V
		T-Pkg: I_O = 500mA		1.1	2.3		1.1	2.3		1.1	2.3		1.1	2.3		1.1	2.3		1.1	2.3	V
Peak Output Current	T_J = 25°C	K,R,P-Pkg.:	1.5	2.1	3.3	1.5	2.1	3.3	1.5	2.1	3.3	1.5	2.1	3.3	1.5	2.1	3.3	1.5	2.1	3.3	A
		T-Pkg:	0.5	0.9		0.5	0.9		0.5	0.9		0.5	0.9		0.5	0.9		0.5	0.9		A
Short Circuit Current	T_J = 25°C	K,R,P-Pkg.		1.1			1.1			1.1			1.1			1.1			1.1		A
		T-Pkg.		0.3			0.3			0.3			0.3			0.3			0.3		A
Ripple Rejection	T_J = 25°C, f = 120Hz, ΔV_{IN} = 10V		54	60		54	60		54	60		54	60		54	60		54	60		dB
Output Noise Voltage	T_J = 25°C, f = 10Hz to 100 kHz			25	80		400			25	80		375			400			375		μV rms
Long Term Stability	1000 hrs at T_J = 125°C			72			72			72			72			72			72		mV
Thermal Shutdown	I_O = 5mA			175			175			175			175			175			175		°C

NOTES:

1. Minimum load current for full line regulation is 5mA. (SG120/220/320 only)
2. Maximum test current for T-Pkg. is 500mA.
3. Unless otherwise specified, V_{IN} = −27V and I_O = 500mA for K,R,P-Package (SG7900 Series). I_O = 1A for K,R,P Pkg (SG120 Series), I_O = 100mA for T-Pkg. C_{IN} = 2μF, C_{OUT} = 1μF.
4. All regulation tests are made at constant junction temperature with low duty-cycle testing.
5. At T_J = −55°C, minimum (V_{IN} − V_O) = 2.5V.
6. Short circuit protection is only assured to V_{IN} = −35V.
7. Line regulation @ I_O = 5mA = 10mV (120-18) and 20mV (320-18).

DEVICE PART NUMBERS			SG7920A			SG120-20			SG7920			SG7920AC			SG320-20			SG7920C			
PACKAGE STYLES (P/N SUFFIX)			K,R,T			K,R,T			K,R,T			K,P,R,T			K,P,R,T			K,P,R,T			
OPERATING JUNCTION TEMPERATURE RANGE (Unless otherwise specified below)			−55°C to 150°C			−55°C to 150°C			−55°C to 150°C			0°C to 125°C			0°C to 125°C			0°C to 125°C			
PARAMETERS	**TEST CONDITIONS (See notes below)**		**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Output Voltage	T_J = 25°C		−19.7	−20.0	−20.3	−19.5	−20.0	−18.5	−19.2	−20.0	−20.8	−19.7	−20.0	−20.3	−19.2	−20.0	−20.8	−19.2	−20.0	−20.8	V
Line Regulation (Note 7)	T_J = 25°C	V_{IN} = −23 to −35V		5	10		5	10		11	150		6	20		5	20		11	300	mV
		V_{IN} = −26 to −32V		4	8					3	75		4	16					3	150	mV
Load Regulation P,R,K Pkg.	T_J = 25°C	I_O = 5mA to 1.5A		30	80		30	80		12	200		30	80		30	80		12	400	mV
		I_O = 250 to 750mA		4	40					4	100		4	40					10	200	mV
T-Pkg.		I_O = 5mA to 500mA		10	25		10	25		10	150		10	40		10	80		10	300	mV
Total Output Voltage Tolerance V_{IN} = −24 to −35V	K,R,P-Pkg: I_O = 5 to 1000mA, P ≤ 15W		−19.4		−20.6	−19.3		−20.7	−19.0		−21.0	−19.4		−20.6	−19.0		−21.0	−19.0		−21.0	V
	T-Pkg: I_O = 5 to 500mA, P ≤ 2W																				
Quiescent Current	T_J = 25°C			1.5	3		1.5	3		1.5	3		1.5	3		1.5	3		1.5	3	mA
	Over Temperature Range				4		2	4			4			4	2		4			4	mA
Quiescent Current Change	With line: V_{IN} = −24 to −35V				1.0		0.1	0.4			1.0			1.0		0.1	0.4			1.0	mA
	With load: I_O = 5 to 1000mA				0.5		0.1	0.4			0.5			0.5		0.1	0.4			0.5	mA
Dropout Voltage ΔV_O = 100mV	T_J = 25°C	K,R,P-Pkg.: I_O = 1A		1.1	2.3		1.1	2.3		1.1	2.3		1.1	2.3		1.1	2.3		1.1	2.3	V
		T-Pkg: I_O = 500mA		1.1	2.3		1.1	2.3		1.1	2.3		1.1	2.3		1.1	2.3		1.1	2.3	V
Peak Output Current	T_J = 25°C	K,R,P-Pkg.:	1.5	2.1	3.3	1.5	2.1	3.3	1.5	2.1	3.3	1.5	2.1	3.3	1.5	2.1	3.3	1.5	2.1	3.3	A
		T-Pkg:	0.5	0.9		0.5	1.0		0.5	1.0		0.5	1.0		0.5	1.0		0.5	1.0		A
Short Circuit Current	T_J = 25°C	K,R,P-Pkg.:		0.9			0.9			0.9			0.9			0.9			0.9		A
		T-Pkg:		0.2			0.2			0.2			0.2			0.2			0.2		A
Ripple Rejection	T_J = 25°C, f = 120Hz, ΔV_{IN} = 10V		54	60		54	60		54	60		54	60		54	60		54	60		dB
Output Noise Voltage	T_J = 25°C, f = 10Hz to 100 kHz			375			400			375			375			400			375		μV rms
Long Term Stability	1000 hrs at T_J = 125°C			80			15	150		80			80			15	150		80		mV
Thermal Shutdown	I_O = 5mA			175			175			175			175			175			175		°C

NOTES:

1. Minimum load current for full line regulation is 5mA. (SG120/220/320 only)
2. Maximum test current for T-Pkg. is 500mA.
3. Unless otherwise specified, V_{IN} = −29V and I_O = 500mA for K,R,P-Package (SG7900 Series). I_O = 1A for K,R,P Pkg (120 Series), I_O = 100mA for T-Pkg. C_{IN} = 2μF, C_{OUT} = 1μF.
4. All regulation tests are made at constant junction temperature with low duty-cycle testing.
5. At T_J = −55°C, minimum (V_{IN} − V_O) = 2.5V.
6. Short circuit protection is only assured to V_{IN} = −35V.
7. Line regulation @ I_O = 5mA = 10mV (120-20) and 20mV (320-20).

PULSE WIDTH MODULATORS

SG1524 / SG2524 / SG3524

Regulating Pulse Width Modulator

Description

This monolithic integrated circuit contains all the control circuitry for a regulating power supply inverter or switching regulator. Included in a 16-pin dual-in-line package is the voltage reference, error-amplifier, oscillator, pulse width modulator, pulse steering flip-flop, dual alternating output switches and current limiting and shut-down circuitry. This device can be used for switching regulators of either polarity, transformer coupled DC to DC converters, transformerless voltage doublers and polarity converters, as well as other power control applications. The SG1524 is specified for operation over the full military temperature range of −55°C to +125°C, while the SG2524 and SG3524 are designed for commercial applications of 0°C to +70°C.

Features

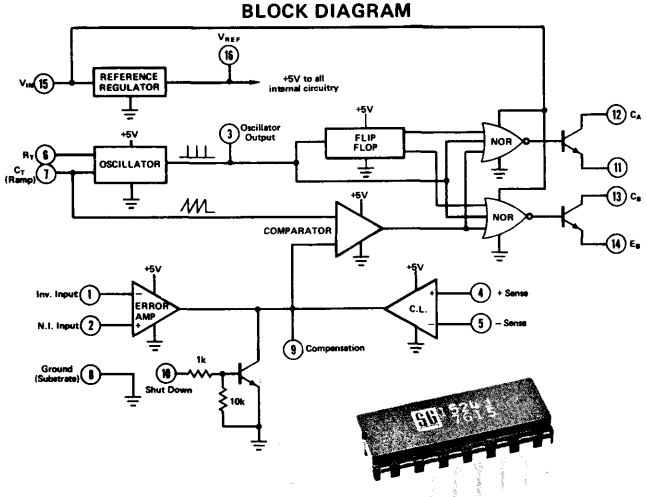
- Complete PWM power control circuitry
- Single ended or push-pull outputs
- Line and load regulation of 0.2%
- 1% maximum temperature variation
- Total supply current less than 10mA
- Operation beyond 100kHz

Absolute Maximum Ratings

Input Voltage	40V
Output Current (each output)	100mA
Reference Output Current	50mA
Oscillator Charging Current	5mA
Power Dissipation (package limitation)	1000mW
Derate above 25°C	8mW/°C

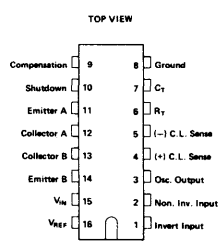
Operating Temperature Range	
SG1524J	-55°C to +125°C
SG2524J	-25°C to +85°C
SG3524J	0°C to +70°C
Storage Temperature Range	-65°C to +150°C

BLOCK DIAGRAM

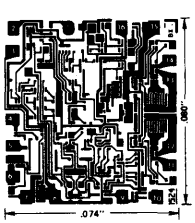


CONNECTION DIAGRAM

TOP VIEW



CHIP LAYOUT

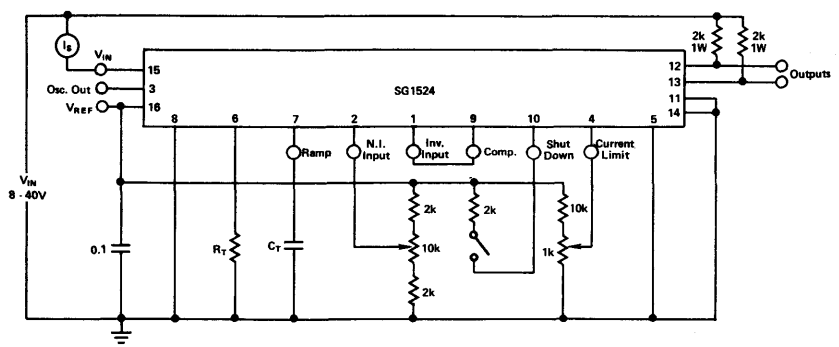


Regulating Pulse Width Modulator

Electrical Characteristics (Unless otherwise stated, these specifications apply for T_A = −55°C to +125°C for the SG1524 and 0°C to +70°C for the SG2524 and SG3524, V_{IN} = 20V, and f = 20kHz)

PARAMETER	CONDITIONS	SG1524			SG2524			SG3524			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Reference Section:											
Output Voltage:		4.8	5.0	5.2	4.6	5.0	5.4				V
Line Regulation	V_{IN} = 8 to 40 Volts	–	10	20	–	10	30				mV
Load Regulation	I_L = 0 to 20mA	–	20	50	–	20	50				mV
Ripple Rejection	f = 120 Hz, T_A = 25°C	–	66	–	–	66	–				dB
Short Circuit Current Limit	V_{REF} = 0, T_A = 25°C	–	100	–	–	100	–				mA
Temperature Stability	Over Operating Temperature Range	–	0.3	1	–	0.3	1				%
Long Term Stability	T_A = 25°C	–	20	–	–	20	–				mV/khr
Oscillator Section:											
Maximum Frequency	C_T = .001 mfd, R_T = 2kΩ	–	300	–	–	300	–				kHz
Initial Accuracy	R_T and C_T constant	–	5	–	–	5	–				%
Voltage Stability	V_{IN} = 8 to 40 Volts, T_A = 25°C	–	–	1	–	–	1				%
Temperature Stability	Over Operating Temperature Range	–	–	2	–	–	2				%
Output Amplitude	Pin 3, T_A = 25°C	–	3.5	–	–	3.5	–				V
Output Pulse Width	C_T = .01 mfd, T_A = 25°C	–	0.5	–	–	0.5	–				μS
Error Amplifier Section:											
Input Offset Voltage	V_{CM} = 2.5 Volts	–	0.5	5	–	2	10				mV
Input Bias Current	V_{CM} = 2.5 Volts	–	2	10	–	2	10				μA
Open Loop Voltage Gain		72	80	–	60	80	–				dB
Common Mode Voltage	T_A = 25°C	1.8	–	3.4	1.8	–	3.4				V
Common Mode Rejection Ratio	T_A = 25°C	–	70	–	–	70	–				dB
Small Signal Bandwidth	A_V = 0dB, T_A = 25°C	–	3	–	–	3	–				MHz
Output Voltage	T_A = 25°C	0.5	–	3.8	0.5	–	3.8				V
Comparator Section:											
Duty Cycle	% Each Output On	0	–	45	0	–	45				%
Input Threshold	Zero Duty Cycle	–	1	–	–	1	–				V
Input Threshold	Max. Duty Cycle	–	3.5	–	–	3.5	–				V
Input Bias Current		–	1	–	–	1	–				μA
Current Limiting Section:	Pin 9 = 2V with Error Amplifier Set for Max Out, T_A = 25°C										
Sense Voltage		190	200	210	180	200	220				mV
Sense Voltage T.C.		–	0.2	–	–	0.2	–				mV/°C
Common Mode Voltage		−0.3	–	+0.3	−0.3	–	+0.3				V
Output Section: (Each Output)											
Collector-Emitter Voltage		40	–	–	40	–	–				V
Collector Leakage Current	V_{CE} = 40V	–	0.1	50	–	0.1	50				μA
Saturation Voltage	I_C = 50mA	–	1	2	–	1	2				V
Emitter Output Voltage	V_{IN} = 20V	17	18	–	17	18	–				V
Rise Time	R_C = 2K ohm, T_A = 25°C	–	0.2	–	–	0.2	–				μS
Fall Time	R_C = 2K ohm, T_A = 25°C	–	0.1	–	–	0.1	–				μS
Total Standby Current: (Excluding oscillator charging current, error and current limit dividers, and with outputs open)	V_{IN} = 40V	–	8	10	–	8	10				mA

OPEN LOOP TEST CIRCUIT



Oscillator

The oscillator in the SG1524 uses an external resistor (R_T) to establish a constant charging current into an external capacitor (C_T). While this uses more current than a series connected RC, it provides a linear ramp voltage on the capacitor which is also used as a reference for the comparator. The charging current is equal to $3.6V \div R_T$ and should be kept within the range of approximately 30 μA to 2 mA, i.e., $1.8k < R_T < 100k$. The range of values for C_T also has limits as the discharge time of C_T determines the pulse width of the oscillator output pulse. This pulse is used (among other things) as a blanking pulse to both outputs to insure that there is no possibility of having both outputs on simultaneously during transitions. This output dead time relationship is shown in Figure 1. A pulse width below approximately 0.5 microseconds may allow false triggering of one output by removing the blanking pulse prior to the flip-flop's reaching a stable state. If small values of C_T must be used, the pulse width may still be expanded by adding a shunt capacitance ($\approx$ 100 pf) to ground at the oscillator output. (Note: Although the oscillator output is a convenient oscilloscope sync input, the cable and input capacitance may increase the blanking pulse width slightly.) Obviously, the upper limit to the pulse width is determined by the maximum duty cycle acceptable. Practical values of C_T fall between .001 and 1.0 mfd.

The oscillator period is approximately $t = R_T C_T$ where t is in microseconds when R_T = ohms and C_T = microfarads.

The use of Figure 2 will allow selection of R_T and C_T for a wide range of operating frequencies. Note that for series regulator applications, the two outputs can be connected in parallel for an effective 0 - 90% duty cycle and the frequency of the oscillator is the frequency of the output. For push-pull applications, the outputs are separated and the flip-flop divides the frequency such that each output's duty cycle is 0 - 45% and the overall frequency is ½ that of the oscillator.

If it is desired to synchronize the SG1524 to an external clock, a pulse of $\approx$ + 3 volts may be applied to the oscillator output terminal with $R_T C_T$ set slightly greater than the clock period. The same considerations of pulse width apply. The impedance to ground at this point is approximately 2k ohms.

If two or more SG1524's must be synchronized together, the easiest method is to interconnect all pin 3 terminals, tie all pin 7's together and to a single C_T, leave all pin 6's open except one which is connected to a single R_T.

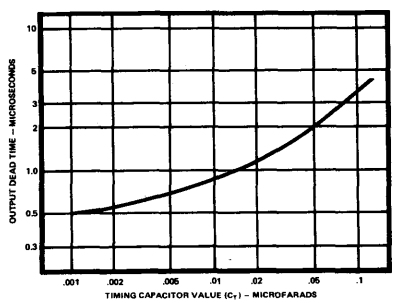


FIGURE 1. Output stage dead time as a function of the timing capacitor value.

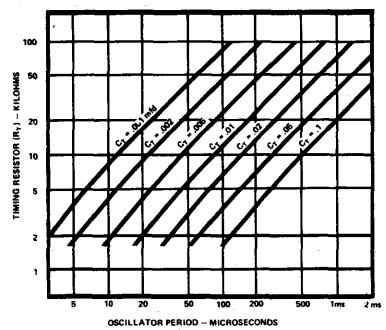


FIGURE 2. Oscillator period as a function of R_T and C_T.

Regulating Pulse Width Modulator

Current Limiting

The current limiting circuitry of the SG1524 is shown in Figure 3.

By matching the base-emitter voltages of Q1 and Q2, and assuming negligible voltage drop across R_1,

$$\text{Threshold} = V_{BE}\,(Q1) + I_1 R_2 - V_{BE}\,(Q2) = I_1 R_2$$
$$\approx 200\,\text{mV}$$

Although this curcuit provides a relatively small threshold with a negligible temperature coefficient, there are some limitations to its use, the most important of which is the ±1 volt common mode range which requires sensing in the ground line. Another factor to consider is that the frequency compensation provided by R_1C_1 and Q1 provides a roll-off pole at approximately 300 Hertz.

Since the gain of this circuit is relatively low, there is a transition region as the current limit amplifier takes over pulse width control from the error amplifier. For testing purposes, threshold is defined as the input voltage to get 25% duty cycle with the error amplifier signaling maximum duty cycle.

If this current limit circuitry is unused, pins 4 and 5 should both be grounded.

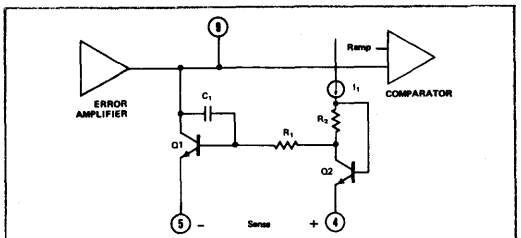
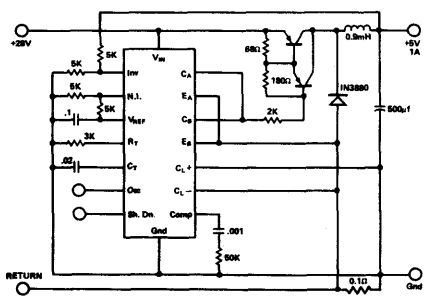
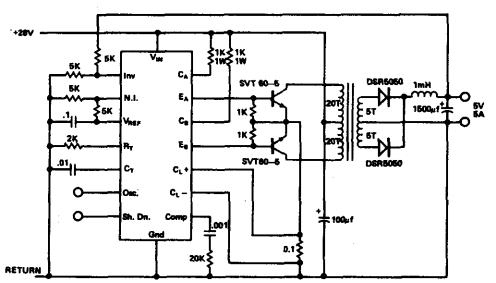


FIGURE 3. Current Limiting Circuitry of the SG1524.



In this conventional single-ended regulator circuit, the two outputs of the SG1524 are connected in parallel for effective 0 - 90% duty-cycle modulation. The use of an output inductor requires and R-C phase compensation network for loop stability.



Push-pull outputs are used in this transformer-coupled DC-DC regulating converter. Note that the oscillator must be set at twice the desired output frequency as the SG1524's internal flip-flop divides the frequency by 2 as it switches the P.W.M. signal from one output to the other. Current limiting is done here in the primary so that the pulse width will be reduced should transformer saturation occur.

See Applications Notes for additional information.

SG1524B/SG2524B/SG3524B

REGULATING PULSE WIDTH MODULATOR

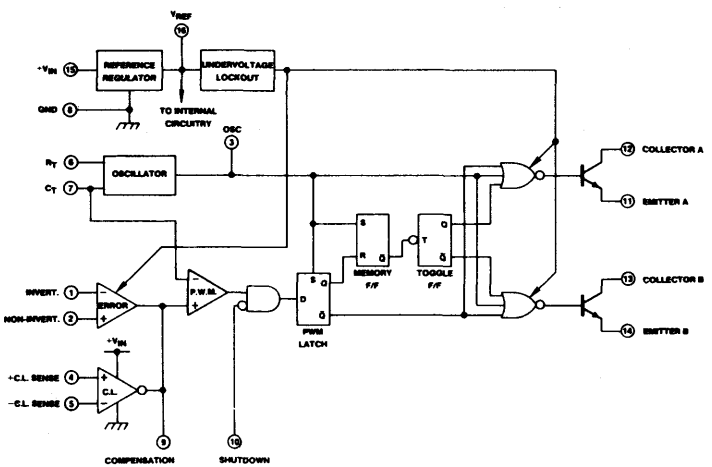
DESCRIPTION

The SG1524B is a pulse width modulator for switching power supplies which features improved performance over industry standards like the SG1524. A direct pin-for-pin replacement for the earlier device, it combines advanced processing techniques and circuit design to provide improved reference accuracy, and extended common mode range at the error amplifier and current limit inputs. A DC-coupled flip-flop eliminates triggering and glitch problems, and a PWM data latch prevents edge oscillations. The circuit incorporates true digital shutdown for high speed response, while an undervoltage lockout circuit prevents spurious outputs when the supply voltage is too low for stable operation. Full double-pulse suppression logic insures alternating output pulses when the Shutdown pin is used for pulse-by-pulse current limiting. The SG1524B is specified for operation over the full military ambient temperature range of −55°C to +125°C. The SG2524B is characterized for the industrial range of −25°C to +85°C, and the SG3524B is designed for the commercial range of 0°C to +70°C.

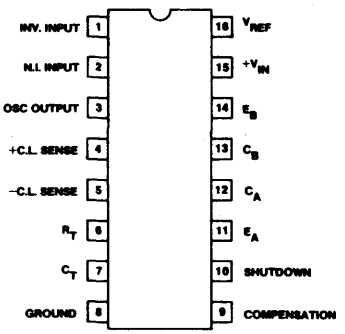
FEATURES

- **7 to 40 volt operation**
- **5 volt reference trimmed to ±1%**
- **100 Hz to 400 kHz oscillator range**
- **Excellent external sync capability**
- **Dual 100 mA output transistors**
- **Wide current limit common mode range**
- **DC-coupled toggle flip-flop**
- **PWM data latch**
- **Undervoltage lockout**
- **Full double-pulse suppression logic**
- **60 volt output collectors**

BLOCK DIAGRAM

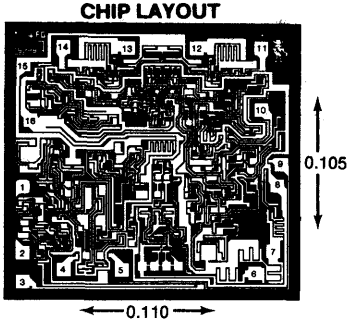


CONNECTION DIAGRAM (TOP VIEW)



J AND N PACKAGE
TO-116

CHIP LAYOUT



ORDER INFORMATION

Part Number	Temperature Range	Package
SG1524BJ	−55°C to +125°C	16 Pin Ceramic DIP
SG2524BJ	−25°C to +85°C	16 Pin Ceramic DIP
SG3524BJ	0°C to +70°C	16 Pin Ceramic DIP
SG3524BN	0°C to +70°C	16 Pin Plastic DIP

ABSOLUTE MAXIMUM RATINGS (Note 1)

Input Voltage ($+V_{IN}$)	+42V	Power Dissipation at T_A = +25°C (Note 2)	1000mW
Collector Voltage	+60V	Thermal Resistance: Junction to Ambient	100°C/W
Logic Inputs	−0.3V to +5.5V	Power Dissipation at T_C = +25°C (Note 3)	2000mW
Current Limit Sense Inputs	−0.3V to $+V_{IN}$	Thermal Resistance: Junction to Case	60°C/W
Output Current (each transistor)	200mA	Operating Junction Temperature	+150°C
Reference Load Current	50mA	Storage Temperature Range	−65°C to +150°C
Oscillator Charging Current	5mA	Lead Temperature (Soldering, 10 seconds)	+300°C

Note 1. Values beyond which damage may occur.
Note 2. Derate at 10 mW/°C for ambient temperatures above +50°C.
Note 3. Derate at 16 mW/°C for case temperatures above +25°C.

RECOMMENDED OPERATING CONDITIONS (Note 4)

Input Voltage ($+V_{IN}$)	+7V to +40V	Oscillator Frequency Range	100Hz to 400kHz
Collector Voltage	0V to +60V	Oscillator Timing Resistor (R_T)	2kΩ to 150kΩ
Error Amp Common Mode Range	+2.3V to +5.2V	Oscillator Timing Capacitor (C_T)	1nF to 0.1μF
Current Limit Sense Common Mode Range	0V to V_{IN}-2.5V	Operating Ambient Temperature Range	
Ouput Current (each transistor)	0 to 100mA	SG1524B	−55°C to +125°C
Reference Load Current	0 to 20mA	SG2524B	−25°C to +85°C
Oscillator Charging Current	25μA to 1.8mA	SG3524B	0°C to +70°C

Note 4. Range over which the device is functional and parameter limits are guaranteed.

ELECTRICAL CHARACTERISTICS ($+V_{IN}$ = 20 volts, and over operating temperature, unless otherwise specified)

PARAMETER	CONDITIONS	SG1524B/2524B			SG3524B			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
REFERENCE SECTION (Note 5)								
Output Voltage	T_J = +25°C	4.95	5.00	5.05	4.90	5.00	5.10	V
Line Regulation	$+V_{IN}$ = 7 to 40 volts		3	20		3	30	mV
Load Regulation	I_L = 0 to 20 mA		5	30		5	50	mV
Temperature Stability (Note 9)	Over Operating Temperature Range		15	50		15	50	mV
Total Output Voltage Range	Over Line, Load and Temperature	4.90		5.10	4.80		5.20	V
Short Circuit Current	V_{REF} = 0 volts	25	50	100	25	50	100	mA
UNDERVOLTAGE LOCKOUT								
Threshold Voltage		4.3	4.5	4.7	4.3	4.5	4.7	V
OSCILLATOR SECTION (Note 6)								
Initial Accuracy	T_J = +25°C	40	43	46	38	43	48	kHz
Voltage Stability	$+V_{IN}$ = 7 to 40 volts		0.1	1		0.1	1	%
Temperature Stability (Note 9)	Over Operating Temperature Range		1	2		1	2	%
Minimum Frequency	R_T = 300kΩ, C_T = 0.1μF		50	100		50	100	Hz
Maximum Frequency	R_T = 2kΩ, C_T = 470 pF	400	600		400	600		kHz
Sawtooth Peak Voltage	$+V_{IN}$ = 40 volts		3.5	3.9		3.5	3.9	V
Sawtooth Valley Voltage	$+V_{IN}$ = 7 volts	0.6	1		0.6	1		V
Clock Amplitude		3.0	4.0		3.0	4.0		V
Clock Pulse Width (Note 9)		0.2	0.5	1.2	0.2	0.5	1.2	μSec

Note 5. I_L = 0 mA
Note 6. F_{OSC} = 43 kHz (R_T = 2700 Ω, C_T = .01 μF)

ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	CONDITIONS	SG1524B/2524B			SG3524B			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
ERROR AMPLIFIER SECTION (Note 7)								
Input Offset Voltage	$R_S \leq 2k\Omega$		0.5	5		2	10	mV
Input Bias Current			1	5		1	10	μA
Input Offset Current				1			1	μA
DC Open Loop Gain	$R_L \geq 10$ Megohms	60	78		60	78		dB
Output Low Level	$I_{SINK} = 100\mu A$; $V_{PIN\ 1} - V_{PIN\ 2} \geq 150$ mV		0.2	0.5		0.2	0.5	V
Output High Level	$I_{SOURCE} = 100\mu A$; $V_{PIN\ 2} - V_{PIN\ 1} \geq 150$ mV	3.8	4.2		3.8	4.2		V
Common Mode Rejection	$V_{CM} = +2.3$ to 5.2 volts	70	90		70	90		dB
Supply Voltage Rejection	$+V_{IN} = 7$ to 40 volts	76	100		76	100		dB
Gain-Bandwidth Product (Note 9)	$T_J = +25°C$	1	2		1	2		MHz
P.W.M. COMPARATOR (Note 6)								
Minimum Duty Cycle	$V_{COMP} = +0.5$ volts			0			0	%
Maximum Duty Cycle	$V_{COMP} = +3.9$ volts	45	49		45	49		%
CURRENT LIMIT AMPLIFIER (Note 8)								
Sense Voltage		180	200	220	170	200	230	mV
Input Bias Current			−3	−10		−3	−10	μA
SHUTDOWN INPUT								
HIGH Input Voltage		2.0			2.0			V
HIGH Input Current	$V_{SHUTDOWN} = +5.0$ volts		0.1	1		0.1	1	mA
LOW Input Voltage				0.6			0.6	V
OUTPUT SECTION (Each transistor)								
Collector Leakage Current	$V_{CE} = 60$ volts			50			50	μA
Collector Saturation Voltage	$I_C = 10$ mA		0.2	0.4		0.2	0.4	V
	$I_C = 100$ mA		1.0	2.0		1.0	2.0	V
Emitter Output Voltage	$I_E = 10$ mA	17.5	19		17.5	19		V
	$I_E = 100$ mA	17	18		17	18		V
Emitter Voltage Rise Time (Note 9)	$R_E = 2k\Omega$, $T_A = +25°C$		0.2	0.5		0.2	0.5	μSec
Collector Voltage Fall Time (Note 9)	$R_C = 2k\Omega$, $T_A = +25°C$		0.1	0.2		0.1	0.2	μSec
POWER CONSUMPTION								
Standby Current	$+V_{IN} = 40$ volts, $V_{SHUTDOWN} = 2.0V$		5	10		5	10	mA

Note 7. $V_{CM} = +2.3V$ to $+5.2V$
Note 8. $V_{CM} = 0$ to $+17.5V$
Note 9. These parameters, although guaranteed over the recommended operating conditions, are not 100% tested in production.

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SG1525A / SG2525A / SG3525A
SG1527A / SG2527A / SG3527A

Regulating Pulse Width Modulators

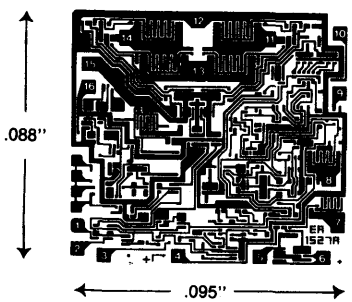
DESCRIPTION

The SG1525A/1527A series of pulse width modulator integrated circuits are designed to offer improved performance and lowered external parts count when used to implement all types of switching power supplies. The on-chip +5.1 volt reference is trimmed to ±1% initial accuracy and the input common-mode range of the error amplifier includes the reference voltage, eliminating external potentiometers and divider resistors. A Sync input to the oscillator allows multiple units to be slaved together, or a single unit to be synchronized to an external system clock. A single resistor between the C_T pin and the Discharge pin provides a wide range of deadtime adjustment. These devices also feature built-in soft-start circuitry with only a timing capacitor required externally. A Shutdown pin controls both the soft-start circuitry and the output stages, providing instantaneous turn-off with soft-start recycle for slow turn-on. These functions are also controlled by an undervoltage lockout which keeps the outputs off and the soft-start capacitor discharged for input voltages less than that required for normal operation. Another unique feature of these PWM circuits is a latch following the comparator. Once a PWM pulse has been terminated for any reason, the outputs will remain off for the duration of the period. The latch is reset with each clock pulse. The output stages are totem-pole designs capable of sourcing or sinking in excess of 200 mA. The SG1525A output stage features NOR logic, giving a LOW output for an OFF state. The SG1527A utilizes OR logic which results in a HIGH output level when OFF.

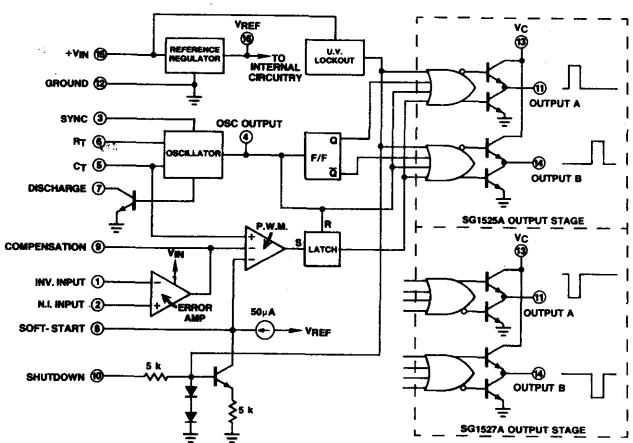
FEATURES

- **8 to 35 volt operation**
- **5.1 volt reference trimmed to ± 1%**
- **100 Hz to 500 kHz oscillator range**
- **Separate oscillator sync terminal**
- **Adjustable deadtime control**
- ***Internal soft-start***
- **Input undervoltage lockout**
- **Latching P.W.M. to prevent multiple pulses**
- **Dual source/sink output drivers**

CHIP LAYOUT



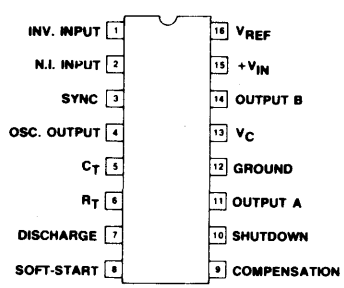
BLOCK DIAGRAM



CONNECTION DIAGRAM
TOP VIEW

J-PACKAGE

TO-116



Note: Pins 9 and 10 are interchanged from non-"A" versions.

Regulating Pulse Width Modulators

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage (+V_{IN})	+40V	Power Dissipation at T_A = +25°C (Note 2)	1000 mW
Collector Supply Voltage (V_C)	+40V	Thermal Resistance: junction to ambient	100°C/W
Logic Inputs	-0.3V to +5.5V	Power Dissipation at T_C = +25°C (Note 3)	2000 mW
Analog Inputs	-0.3V to +V_{IN}	Thermal Resistance: junction to case	60°C/W
Output Current, Source or Sink	500 mA	Operating Junction Temperature	+150°C
Reference Output Current	50 mA	Storage Temperature Range	-65°C to 150°C
Oscillator Charging Current	5 mA	Lead Temperature (Soldering, 10 seconds)	+300°C

Note 1. Values beyond which damage may occur.
Note 2. Derate at 10 mW/°C for ambient temperatures above +50°C.
Note 3. Derate at 16 mW/°C for case temperatures above +25°C.

RECOMMENDED OPERATING CONDITIONS (Note 4)

Input Voltage (+V_{IN})	+8V to +35V	Oscillator Timing Capacitor	.001 μF to 0.1 μF
Collector Supply Voltage (V_C)	+4.5V to +35V	Deadtime Resistor Range	0 to 500Ω
Sink/Source Load Current (steady state)	0 to 100 mA	Operating Ambient Temperature Range	
Sink/Source Load Current (peak)	0 to 400 mA	SG1525A, SG1527A	-55°C to +125°C
Reference Load Current	0 to 20 mA	SG2525A, SG2527A	-25°C to +85°C
Oscillator Frequency Range	100 Hz to 400 kHz	SG3525A, SG3527A	0°C to +70°C
Oscillator Timing Resistor	2kΩ to 150kΩ		

Note 4. Range over which the device is functional and parameter limits are guaranteed.

ELECTRICAL CHARACTERISTICS (+V_{IN} = 20V, and over operating temperature, unless otherwise specified)

PARAMETER	CONDITIONS	SG1525A / 2525A SG1527A / 2527A			SG3525A SG3527A			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
REFERENCE SECTION								
Output Voltage	T_j = 25°C	5.05	5.10	5.15	5.00	5.10	5.20	V
Line Regulation	V_{IN} = 8 to 35V		10	20		10	20	mV
Load Regulation	I_L = 0 to 20 mA		20	50		20	50	mV
Temperature Stability[5]	Over Operating Range		20	50		20	50	mV
Total Output Variation[5]	Line, Load, and Temp	5.00		5.20	4.95		5.25	V
Short Circuit Current	V_{REF} = 0, T_j = 25°C		80	100		80	100	mA
Output Noise Voltage[5]	10 Hz ≤ f ≤ 10 kHz, T_j = 25°C		40	200		40	200	μVrms
Long Term Stability[5]	T_j = 125°C		20	50		20	50	mV/khr
OSCILLATOR SECTION (Note 6)								
Initial Accuracy[5,6]	T_j = 25°C		±2	± 6		± 2	± 6	%
Voltage Stability[5,6]	V_{IN} = 8 to 35V		± 0.3	± 1		± 1	± 2	%
Temperature Stability[5]	Over Operating Range		± 3	± 6		± 3	± 6	%
Minimum Frequency	R_T = 150 kΩ, C_T = 0.1 μF			100			100	Hz
Maximum Frequency	R_T = 2 kΩ, C_T = 1 nF	400			400			kHz
Current Mirror	I_{RT} = 2 mA	1.7	2.0	2.2	1.7	2.0	2.2	mA
Clock Amplitude[5,6]		3.0	3.5		3.0	3.5		V
Clock Width[5,6]	T_j = 25°C	0.3	0.5	1.0	0.3	0.5	1.0	μ sec
Sync Threshold		1.2	2.0	2.8	1.2	2.0	2.8	V
Sync Input Current	Sync Voltage = 3.5V		1.0	2.5		1.0	2.5	mA

Regulating Pulse Width Modulators

ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	CONDITIONS	SG1525A / 2525A SG1527A / 2527A			SG3525A SG3527A			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
ERROR AMPLIFIER SECTION (V_{CM} = 5.1 Volts)								
Input Offset Voltage			0.5	5		2	10	mV
Input Bias Current			1	10		1	10	µA
Input Offset Current				1			1	µA
DC Open Loop Gain	$R_L \geq 10$ Meg Ω	60	75		60	75		dB
Gain-Bandwidth Product[5]	A_V = 0 dB, T_j = 25°C	1	2		1	2		MHz
Output Low Level			0.2	0.5		0.2	0.5	V
Output High Level		3.8	5.6		3.8	5.6		V
Common Mode Rejection	V_{CM} = 1.5 to 5.2V	60	75		60	75		dB
Supply Voltage Rejection	V_{IN} = 8 to 35V	50	60		50	60		dB
P.W.M. COMPARATOR								
Minimum Duty Cycle				0			0	%
Maximum Duty Cycle		45	49		45	49		%
Input Threshold[6]	Zero Duty Cycle	0.6	0.9		0.6	0.9		V
Input Threshold[6]	Max Duty Cycle		3.3	3.6		3.3	3.6	V
Input Bias Current[5]			.05	1.0		.05	1.0	µA
SOFT—START SECTION								
Soft Start Current	$V_{SHUTDOWN}$ = 0V	25	50	80	25	50	80	µA
Soft Start Voltage	$V_{SHUTDOWN}$ = 2V		0.4	0.6		0.4	0.6	V
Shutdown Input Current	$V_{SHUTDOWN}$ = 2.5V		0.4	1.0		0.4	1.0	mA
OUTPUT DRIVERS (Each Output) (V_C = 20 Volts)								
Output Low Level	I_{SINK} = 20 mA		0.2	0.4		0.2	0.4	V
	I_{SINK} = 100 mA		1.0	2.0		1.0	2.0	V
Output High Level	I_{SOURCE} = 20 mA	18	19		18	19		V
	I_{SOURCE} = 100 mA	17	18		17	18		V
Undervoltage Lockout	V_{Comp} and V_{SS}=high	6	7	8	6	7	8	V
Collector Leakage[7]	V_C = 35V			200			200	µA
Rise Time[5]	C_L = 1 nF, T_j = 25°C		100	600		100	600	nsec
Fall Time[5]	C_L = 1 nF, T_j = 25°C		50	300		50	300	nsec
Shutdown Delay[5]	V_{SD}=3V, C_S = 0, T_j = 25°C		0.2	0.5		0.2	0.5	µsec
TOTAL STANDBY CURRENT								
Supply Current	V_{IN} = 35V		14	20		14	20	mA

Note 5. These parameters, although guaranteed over the recommended operating conditions, are not 100% tested in production.
Note 6. Tested at f_{OSC} = 40 kHz (R_T = 3.6 kΩ, C_T = .01 µF, R_D = 0Ω).
Note 7. Applies to SG1525A/2525A/3525A only, due to polarity of output pulses.

Regulating Pulse Width Modulators

APPLICATIONS

SHUTDOWN OPTIONS (See Block Diagram, Page 1)

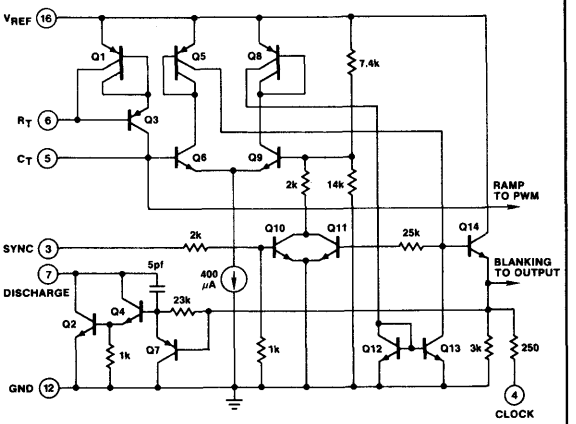
1. Use an external transistor or open-collector comparator to pull down on the Comp Terminal (pin 9). This will set the PWM latch turning off both outputs. If the shutdown signal is momentary, pulse-by-pulse protection can be accomplished as the PWM latch will be reset with each clock pulse.

2. The same results can be accomplished by pulling down on the Soft-Start terminal (pin 8) with the difference that on this pin, shutdown will not affect the amplifier compensation network but must discharge any Soft-Start capacitor.

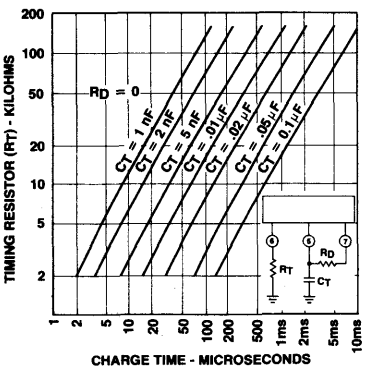
3. Apply a positive-going signal to the Shutdown terminal (pin 10). This will provide most rapid shutdown of the outputs but will not immediately set the PWM latch if there is a Soft-Start capacitor. This capacitor will discharge but with a current of approximately twice the charging current.

4. The shutdown terminal (pin 10) can be used to set the PWM latch on a pulse-by-pulse basis if there is no external capacitance on pin 8. Slow turn-on may still be accomplished by applying an external capacitor, blocking diode, and charging resistor to the comp terminal (pin 9). (See SG1524 Application Note).

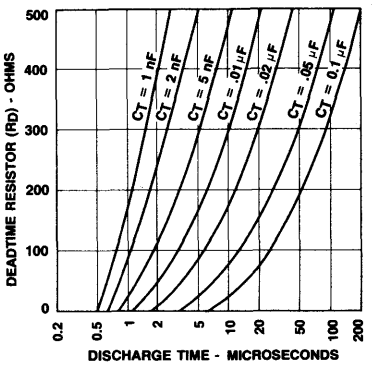
SG1525A OSCILLATOR SCHEMATIC



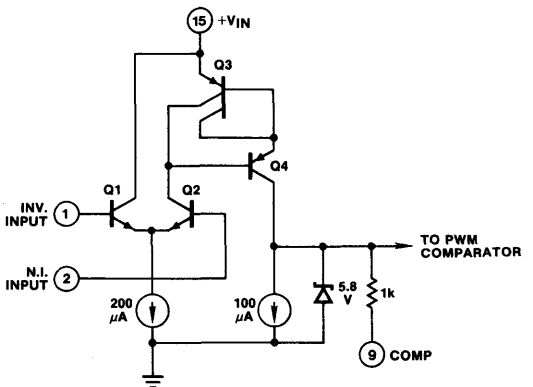
OSCILLATOR CHARGE TIME VS. R_T AND C_T



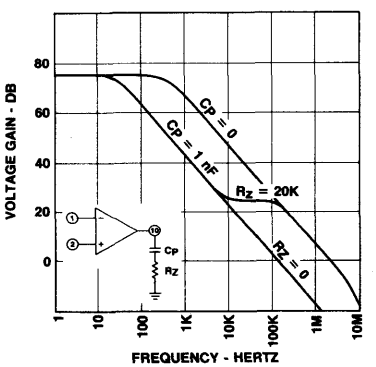
OSCILLATOR DISCHARGE TIME VS. R_D AND C_T



SG1525A ERROR AMPLIFIER



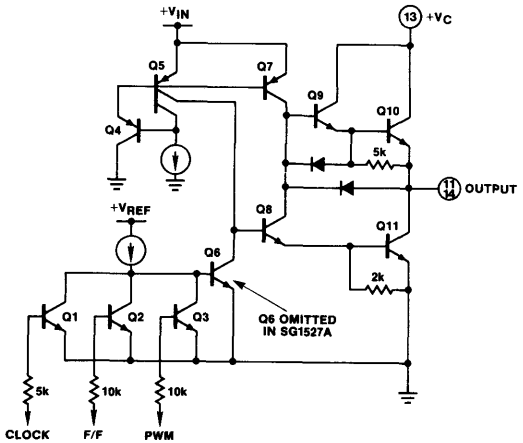
ERROR AMPLIFIER OPEN-LOOP FREQUENCY RESPONSE



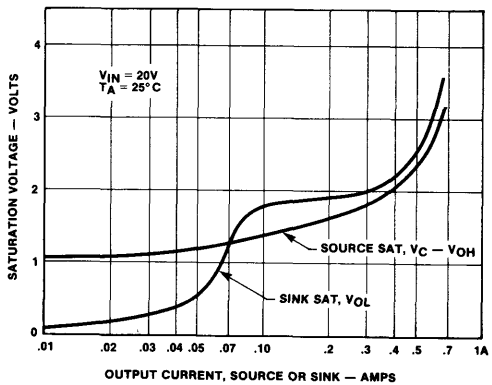
Regulating Pulse Width Modulators

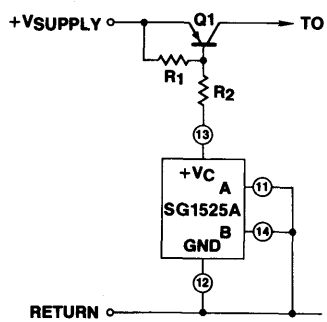
OUTPUT APPLICATIONS (OUTPUT CIRCUITS)

SG1525A OUTPUT CIRCUIT (½ CIRCUIT SHOWN)

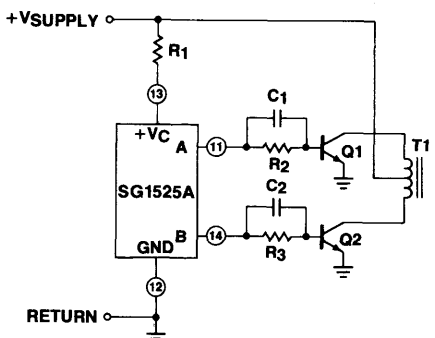


SG1525A OUTPUT SATURATION CHARACTERISTICS

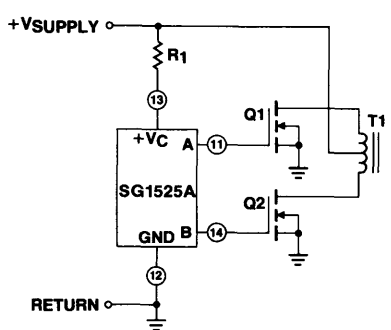




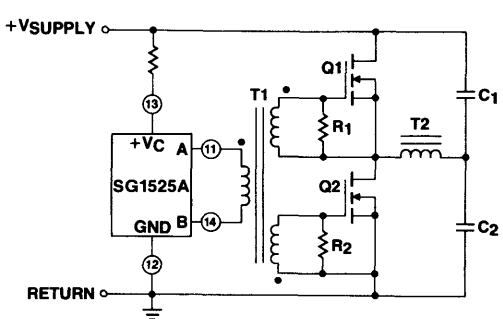
For single-ended supplies, the driver outputs are grounded. The V_C terminal is switched to ground by the totem-pole source transistors on alternate oscillator cycles.



In conventional push-pull bipolar designs, forward base drive is controlled by R_1-R_3. Rapid turn-off times for the power devices are achieved with speed-up capacitors C_1 and C_2.



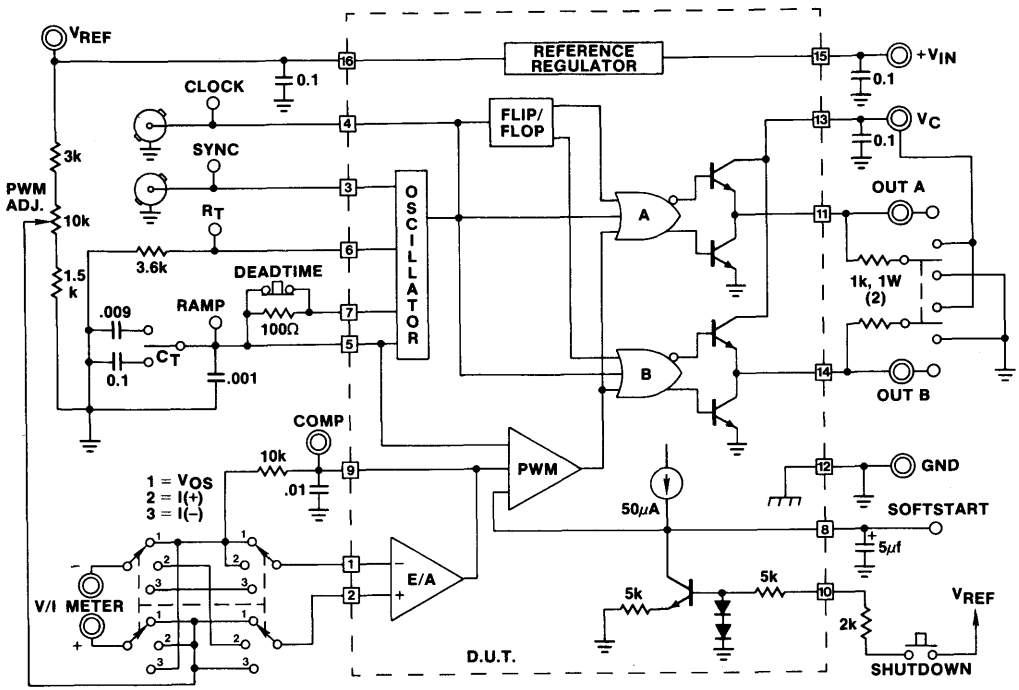
The low source impedance of the output drivers provides rapid charging of power FET input capacitance while minimizing external components.



Low power transformers can be driven directly by the SG1525A. Automatic reset occurs during deadtime, when both ends of the primary winding are switched to ground.

Regulating Pulse Width Modulators

SG1525A/1527A LAB TEST FIXTURE



SG1526/SG2526/SG3526

REGULATING PULSE WIDTH MODULATOR

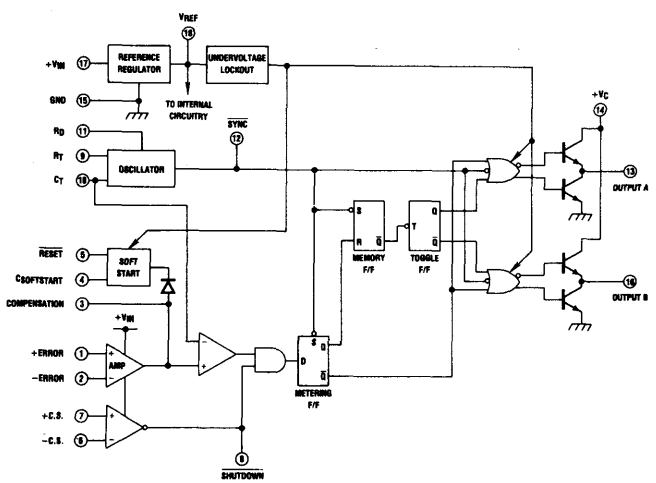
DESCRIPTION

The 1526 is a high performance monolithic pulse width modulator circuit designed for fixed-frequency switching regulators and other power control applications. Included in an 18-pin dual-in-line package are a temperature compensated voltage reference, sawtooth oscillator, error amplifier, pulse width modulator, pulse metering and steering logic, and two low impedance power drivers. Also included are protective features such as soft-start and under-voltage lockout, digital current limiting, double pulse inhibit, a data latch for single pulse metering, adjustable deadtime, and provision for symmetry correction inputs. For ease of interface, all digital control ports are TTL and B-series CMOS compatible. Active LOW logic design allows wired-OR connections for maximum flexibility. This versatile device can be used to implement single-ended or push-pull switching regulators of either polarity, both transformerless and transformer coupled. The SG1526 is characterized for operation over the full military junction temperature range of −55° C to +150° C. The SG2526 is characterized for operation from −25° C to +150° C, and the SG3526 is characterized for operation from 0° C to +125° C.

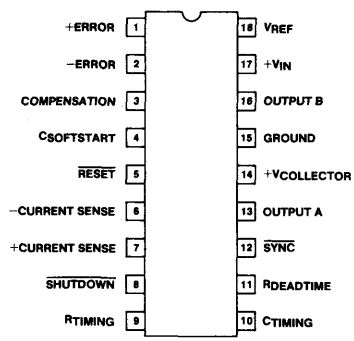
FEATURES

- **8 to 35 volt operation**
- **5 volt reference trimmed to ±1%**
- **1 Hz to 400 kHz oscillator range**
- **Dual 100 mA source/sink outputs**
- **Digital current limiting**
- **Double pulse suppression**
- **Programmable deadtime**
- **Undervoltage lockout**
- **Single pulse metering**
- **Programmable soft-start**
- **Wide current limit common mode range**
- **TTL/CMOS compatible logic ports**
- **Symmetry correction capability**
- **Guaranteed 6 unit synchronization**

BLOCK DIAGRAM

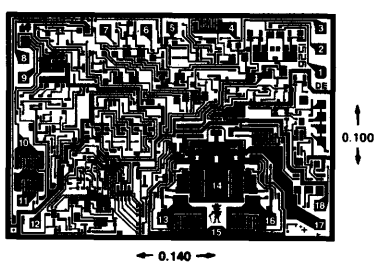


CONNECTION DIAGRAM (TOP VIEW)



J PACKAGE
TO-116 STYLE

CHIP LAYOUT



ORDER INFORMATION

Part Number	Junction Temperature Range	Package
SG1526J	−55° C to +150° C	18-pin Ceramic DIP
SG2526J	−25° C to +150° C	18-pin Ceramic DIP
SG3526J	0° C to +125° C	18-pin Ceramic DIP
SG3526N	0° C to +125° C	18-pin Plastic DIP

Regulating Pulse Width Modulator

ABSOLUTE MAXIMUM RATINGS (Note 1)

Input Voltage (+VIN)	+40V	Power Dissipation at T_A = +25°C (Note 2)	1000 mW
Collector Supply Voltage (+ VC)	+40V	Thermal Resistance: junction to ambient	100°C/W
Logic Inputs	−0.3V to +5.5V	Power Dissipation at T_C = +25°C (Note 3)	3000 mW
Analog Inputs	−0.3V to +VIN	Thermal Resistance: junction to case	42°C/W
Source/Sink Load Current (each output)	200 mA	Operating Junction Temperature	+150°C
Reference Load Current	50 mA	Storage Temperature Range	−65°C to +150°C
Logic Sink Current	15 mA	Lead Temperature (soldering, 10 seconds)	+300°C

Note 1. Values beyond which damage may occur.
Note 2. Derate at 10 mW/°C for ambient temperaures above +50° C.
Note 3. Derate at 24 mW/°C for case temperatures above +25° C.

RECOMMENDED OPERATING CONDITIONS (Note 4)

Input Voltage	+8V to +35V	Oscillator Timing Capacitor	1nF to 20μF
Collector Supply Voltage	+4.5V to +35V	Available Deadtime Range at 40kHz	3% to 50%
Sink/Source Load Current (each output)	0 to 100 mA	guaranteed.	
Reference Load Current	0 to 20 mA	SG1526	−55°C to +150°C
Oscillator Frequency Range	1 Hz to 400 kHz	SG2526	−25°C to +150°C
Oscillator Timing Resistor	2 kΩ to 150 kΩ	SG3526	0°C to +125°C

Note 4. Range over which the device is functional and parameter limits are

ELECTRICAL CHARACTERISTICS

(+VIN = 15V, and over operating junction temperature, unless otherwise specified)

PARAMETER	CONDITIONS	SG1526/2526			SG3526			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
REFERENCE SECTION (Note 5)								
Output Voltage	T_j = +25°C	4.95	5.00	5.05	4.90	5.00	5.10	V
Line Regulation	+VIN = 8 to 35V		10	20		10	30	mV
Load Regulation	I_L = 0 to 20 mA		10	30		10	50	mV
Temperature Stability	Over Operating T_j		15	50		15	50	mV
Total Output Voltage Range	Over Recommended Operating Conditions	4.90	5.00	5.10	4.85	5.00	5.15	V
Short Circuit Current	VREF = 0V	25	50	100	25	50	100	mA
UNDERVOLTAGE LOCKOUT								
$\overline{\text{RESET}}$ Output Voltage	VREF = 3.8V		0.2	0.4		0.2	0.4	V
$\overline{\text{RESET}}$ Output Voltage	VREF = 4.8V	2.4	4.8		2.4	4.8		V
OSCILLATOR SECTION (Note 6)								
Initial Accuracy	T_j = +25°C		±3	±8		±3	±8	%
Voltage Stability	+VIN = 8 to 35V		0.5	1		0.5	1	%
Temperature Stability	Over Operating T_j		7	10		3	5	%
Minimum Frequency	RT = 150 kΩ, CT = 20 μF			1			1	Hz
Maximum Frequency	RT = 2 kΩ, CT = 1.0 nF	400			400			kHz
Sawtooth Peak Voltage	+VIN = 35V		3.0	3.5		3.0	3.5	V
Sawtooth Valley Voltage	+ VIN = 8V	0.5	1.0		0.5	1.0		V

Note 5. I_L = 0 mA.
Note 6. FOSC = 40 kHz (RT = 4.12 kΩ ± 1%, CT = .01 μF ± 1%, RD = 0Ω

Regulating Pulse Width Modulator

ELECTRICAL CHARACTERISTICS (continued)

PARAMETER	CONDITIONS	SG1526/2526			SG3526			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
ERROR AMPLIFIER SECTION (Note 7)								
Input Offset Voltage	RS ≤ 2 kΩ		2	5		2	10	mV
Input Bias Current			−350	−1000		−350	−2000	nA
Input Offset Current			35	100		35	200	nA
DC Open Loop Gain	RL ≥ 10 Meg Ω	64	72		60	72		dB
High Output Voltage	Vpin1 −Vpin2≥150mV, I_{source} = 100μA	3.6	4.2		3.6	4.2		V
Low Output Voltage	Vpin2 −Vpin1≥150mV, I_{sink} = 100μA		0.2	0.4		0.2	0.4	V
Common Mode Rejection	RS ≤ 2kΩ	70	94		70	94		dB
Supply Voltage Rejection	+VIN = 12 to 18V	66	80		66	80		dB
P.W.M. COMPARATOR (Note 6)								
Minimum Duty Cycle	Vcompensation = +0.4V			0			0	%
Maximum Duty Cycle	Vcompensation = +3.6V	45	49		45	49		%
DIGITAL PORTS (SYNC, SHUTDOWN, and RESET)								
HIGH Ouput Voltage	Isource = 40 μA	2.4	4.0		2.4	4.0		V
LOW Output Voltage	Isink = 3.6 mA		0.2	0.4		0.2	0.4	V
HIGH Input Current	VIH = +2.4V		−125	−200		−125	−200	μA
LOW Input Current	VIL = +0.4V		−225	−360		−225	−360	μA
CURRENT LIMIT COMPARATOR (Note 8)								
Sense Voltage	RS ≤ 50 Ω	90	100	110	80	100	120	mV
Input Bias Current			−3	−10		−3	−10	μA
SOFT-START SECTION								
Error Clamp Voltage	RESET = +0.4V		0.1	0.4		0.1	0.4	V
CS Charging Current	RESET = +2.4V	50	100	150	50	100	150	μA
OUTPUT DRIVERS (Each Output) (Note 9)								
HIGH Output Voltage	Isource = 20 mA	12.5	13.5		12.5	13.5		V
	Isource = 100 mA	12	13		12	13		V
LOW Output Voltage	Isink = 20 mA		0.2	0.3		0.2	0.3	V
	Isink = 100 mA		1.2	2.0		1.2	2.0	V
Collector Leakage	VC = 40V		50	150		50	150	μA
Rise Time	CL = 1000 pF		0.3	0.6		0.3	0.6	μSec
Fall Time	CL = 1000 pF		0.1	0.2		0.1	0.2	μSec
POWER CONSUMPTION (Note 10)								
Standby Current	SHUTDOWN = +0.4V		18	30		18	30	mA

Note 7. V_{CM} = 0 to +5.2V

Note 8. V_{CM} = 0 to +12V

Note 9. V_C = +15V

Note 10. $+V_{IN}$ = + 35V, R_T = 4.12kΩ

Regulating Pulse Width Modulator

TYPICAL CHARACTERISTICS

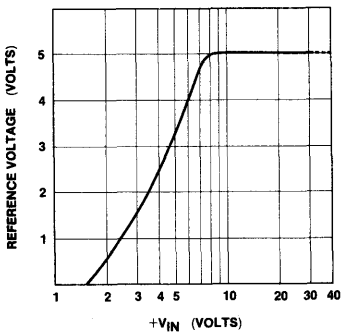


FIGURE 1.
REFERENCE VOLTAGE VS. SUPPLY VOLTAGE

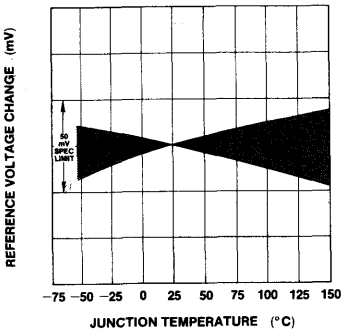


FIGURE 2.
REFERENCE TEMPERATURE STABILITY

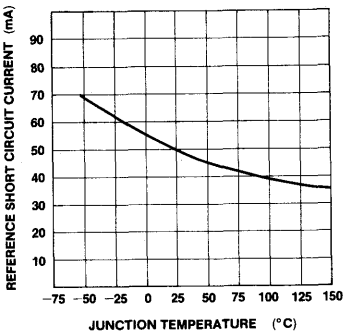


FIGURE 3.
REFERENCE SHORT CIRCUIT CURRENT

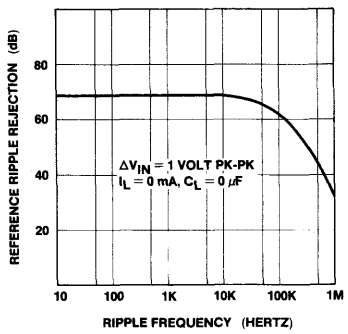


FIGURE 4.
REFERENCE RIPPLE REJECTION

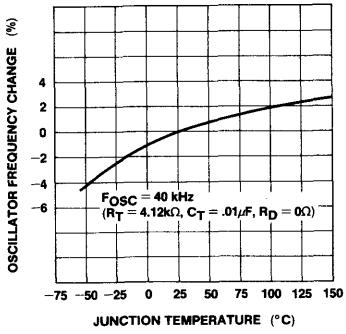


FIGURE 5.
OSCILLATOR FREQUENCY TEMPERATURE STABILITY

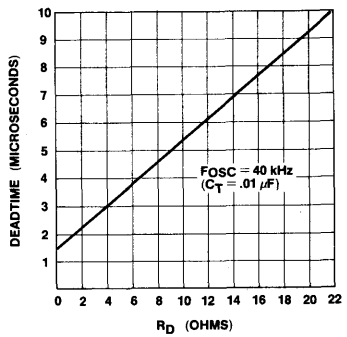


FIGURE 6.
OUTPUT DRIVER DEADTIME VS. R_D VALUE

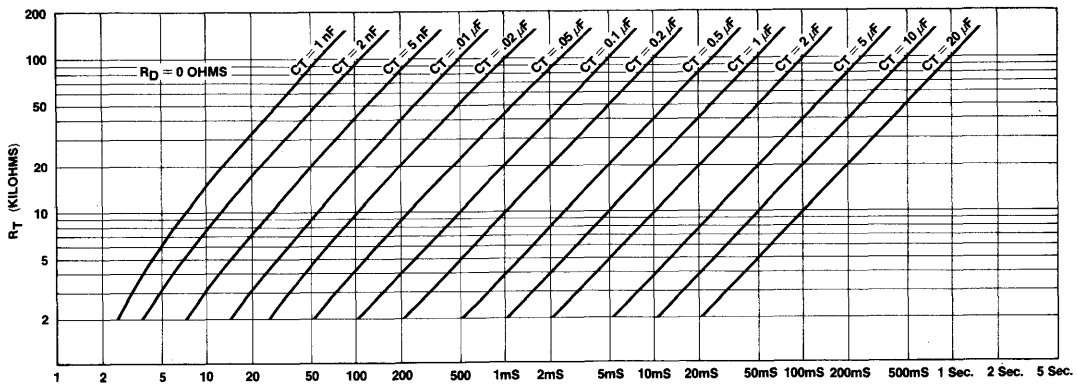


FIGURE 7.
OSCILLATOR PERIOD VS. R_T AND C_T

Regulating Pulse Width Modulator

TYPICAL CHARACTERISTICS

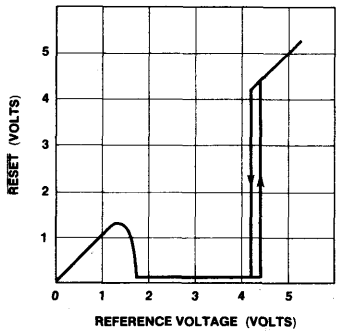


FIGURE 8.
UNDERVOLTAGE LOCKOUT CHARACTERISTIC

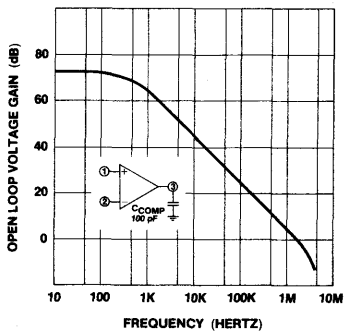


FIGURE 9.
ERROR AMPLIFIER OPEN LOOP GAIN vs FREQUENCY

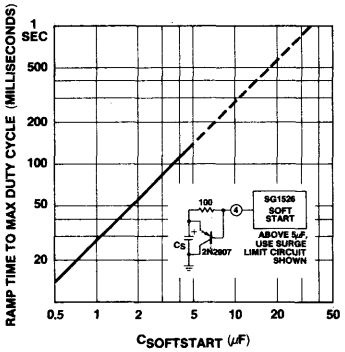


FIGURE 10.
SOFTSTART TIME CONSTANT vs C_S

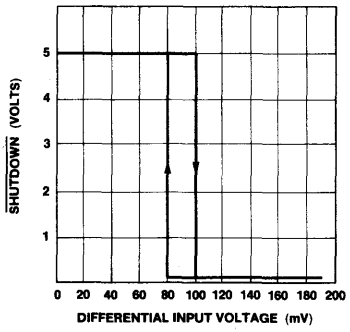


FIGURE 11.
CURRENT LIMIT TRANSFER FUNCTION

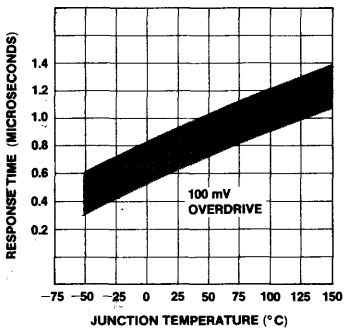


FIGURE 12.
COMPARATOR INPUT TO DRIVER OUTPUT DELAY

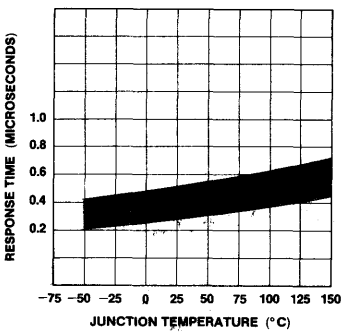


FIGURE 13.
$\overline{\text{SHUTDOWN}}$ INPUT TO DRIVER OUTPUT DELAY

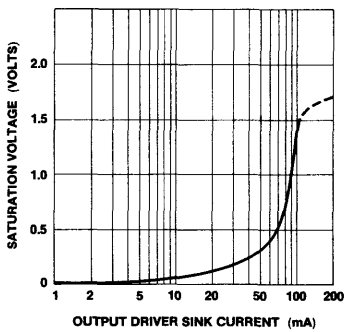


FIGURE 14.
OUTPUT DRIVER SATURATION VOLTAGE vs I_{SINK}

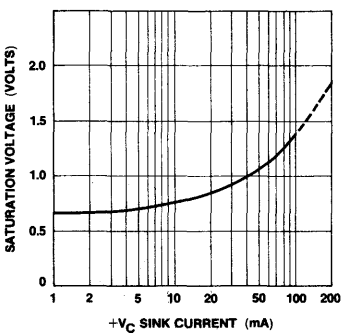


FIGURE 15.
COLLECTOR SUPPLY SATURATION VOLTAGE vs I_{SINK}

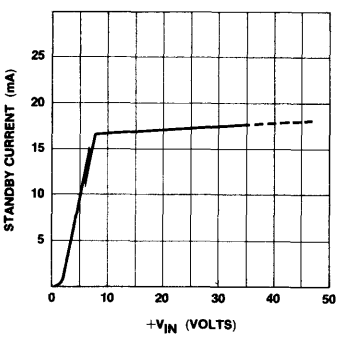


FIGURE 16.
STANDBY CURRENT vs SUPPLY VOLTAGE

ALL CHARACTERISTICS SHOWN ARE NOMINAL VALUES AT +25°C, UNLESS INDICATED OTHERWISE ON THE GRAPHS.

Regulating Pulse Width Modulator

VOLTAGE REFERENCE

The reference regulator of the SG1526 is based on a temperature compensated zener diode. The circuitry is fully active at supply voltages above +8 volts, and provides up to 20 mA of load current to external circuitry at +5.0 volts. In systems where additional current is required, an external PNP transistor can be used to boost the available current. A rugged low frequency audio-type transistor should be used, and lead lengths between the PWM and transistor should be as short as possible to minimize the risk of oscillations. Even so, some types of transistors may require collector-base capacitance for stability. Up to 1 amp of load current can be obtained with excellent regulation if the device selected maintains high current gain.

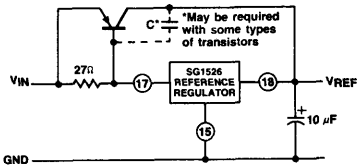


FIGURE 17.
EXTENDING REFERENCE OUTPUT CURRENT

UNDERVOLTAGE LOCKOUT

The undervoltage lockout circuit protects the SG1526 and the power devices it controls from inadequate supply voltage. If $+V_{IN}$ is too low, the circuit disables the output drivers and holds the $\overline{\text{RESET}}$ pin LOW. This prevents spurious output pulses while the control circuitry is stabilizing, and holds the soft-start timing capacitor in a discharged state.

The circuit consists of a +1.2 volt bandgap reference and comparator circuit which is active when the reference voltage has risen to 3 V_{BE}, or +1.8 volts at 25°C. When the reference voltage rises to approximately +4.4 volts, the circuit enables the output drivers and releases the $\overline{\text{RESET}}$ pin, allowing a normal soft-start. The comparator has 200 mV of hysteresis to minimize oscillation at the trip point. When $+V_{IN}$ to the PWM is removed and the reference drops to +4.2 volts, the undervoltage circuit pulls $\overline{\text{RESET}}$ LOW again. The soft-start capacitor is immediately discharged, and the PWM is ready for another soft-start cycle.

The SG1526 can operate from a +5 volt supply by connecting the V_{REF} pin to the $+V_{IN}$ pin and maintaining the supply between +4.8 and +5.2 volts.

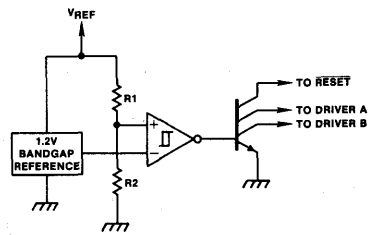


FIGURE 18.
SIMPLIFIED UNDERVOLTAGE LOCKOUT

SOFT-START CIRCUIT

The soft-start circuit protects the power transistors and rectifier diodes from high current surges during power supply turn-on. When supply voltage is first applied to the SG1526, the undervoltage lockout circuit holds $\overline{\text{RESET}}$ LOW with Q3. Q1 is turned on, which holds the soft-start capacitor voltage at zero. The second collector of Q1 clamps the output of the error amplifier to ground, guaranteeing zero duty cycle at the driver outputs. When the supply voltage reaches normal operating range, $\overline{\text{RESET}}$ will go HIGH. Q1 turns off, allowing the internal 100 µA current source to charge C_S. Q2 clamps the error amplifier output to 1 V_{BE} above the voltage on C_S. As the soft-start voltage ramps up to +5 volts, the duty cycle of the PWM linearly increases to whatever value the voltage regulation loop requires for an error null. Figure 10 gives the timing relationship between C_S and ramp time to 100% duty cycle.

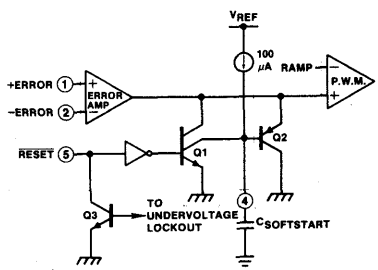


FIGURE 19.
SOFT-START CIRCUIT SCHEMATIC

DIGITAL CONTROL PORTS

The three digital control ports of the SG1526 are bi-directional. Each pin can drive TTL and 5 volt CMOS logic directly, up to a fan-out of 10 low-power Schottky gates. Each pin can also be directly driven by open-collector TTL, open-drain CMOS, and open-collector voltage comparators; fan-in is equivalent to 1 low-power Schottky gate. Each port is normally HIGH; the pin is pulled LOW to activate the particular function. Driving $\overline{\text{SYNC}}$ LOW initiates a discharge cycle in the oscillator. Pulling $\overline{\text{SHUTDOWN}}$ LOW immediately inhibits all PWM output pulses. Holding $\overline{\text{RESET}}$ LOW discharges the soft-start capacitor. The logic threshold is +1.1 volts at +25°C. Noise immunity can be gained at the expense of fan-out with an external 2K pullup resistor to +5 volts.

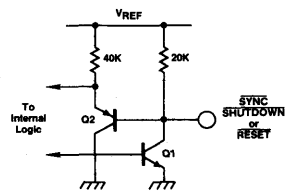


FIGURE 20.
DIGITAL CONTROL PORT SCHEMATIC

Regulating Pulse Width Modulator

OSCILLATOR

The oscillator is programmed for frequency and dead time with three components: R_T, C_T, and R_D. Two waveforms are generated: a sawtooth waveform at pin 10 for pulse width modulation, and a logic clock at pin 12. The following procedure is recommended for choosing timing values:

1. With R_D = 0 ohms (pin 11 shorted to ground) select values for R_T and C_T from Figure 7 to give the desired oscillator period. Remember that the frequency at each driver output is half the oscillator frequency, and the frequency at the $+V_C$ terminal is the same as the oscillator frequency.
2. If more dead time is required, select a larger value of R_D using Figure 6 as a guide. At 40 KHz dead time increases by 400 nSec/ohm.
3. Increasing the dead time will cause the oscillator frequency to decrease slightly. Go back and decrease the value of R_T slightly to bring the frequency back to the nominal design value.

The SG1526 can be synchronized to an external logic clock by programming the oscillator to free-run at a frequency 10% slower than the sync frequency. A periodic LOW logic pulse approximately 0.5 μSec wide at the $\overline{SYNC}$ pin will then lock the oscillator to the external frequency.

Multiple devices can be synchronized together by programming one master unit for the desired frequency, and then sharing its sawtooth and clock waveforms with the slave units. All C_T terminals are connected to the C_T pin of the master, and all $\overline{SYNC}$ terminals are likewise connected to the $\overline{SYNC}$ pin of the master. Slave R_T terminals are left open or connected to V_{REF}. Slave R_D terminals may be either left open or grounded.

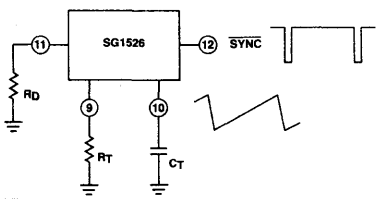


FIGURE 21
OSCILLATOR CONNECTIONS AND WAVEFORMS

ERROR AMPLIFIER

The error amplifier is a transconductance design, with an output impedance of 2 megohms. Since all voltage gain takes place at the output pin, the open-loop gain/frequency characteristics can be controlled with shunt reactance to ground. When compensated for unity-gain stability with 100 pF, the amplifier has an open-loop pole at 400 Hz.

The input connections to the error amplifier are determined by the polarity of the switching supply output voltage. For positive supplies, the common-mode voltage is +5.0 volts and the feedback connections in Figure 22A are used. With negative supplies, the common-mode voltage is ground and the feedback divider is connected between the negative output and the +5.0 volt reference voltage, as shown in Figure 22B.

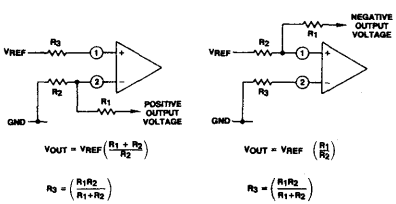


FIGURE 22A FIGURE 22B
ERROR AMPLIFIER CONNECTIONS

OUTPUT DRIVERS

The totem-pole output drivers of the SG1526 are designed to source and sink 100 mA continuously and 200 mA peak. Loads can be driven either from the output pins 13 and 16, or from the $+V_C$ pin, as required. Curves for the saturation voltage at these outputs as a function of load current are found in Figures 14 and 15.

Since the bottom transistor of the totem-pole is allowed to saturate, there is a momentary conduction path from the $+V_C$ terminal to ground during switching. To limit the resulting current spikes a small resistor in series with pin 14 is always recommended. The resistor value is determined by the driver supply voltage, and should be chosen for 200 mA peak currents, as shown in Figure 25.

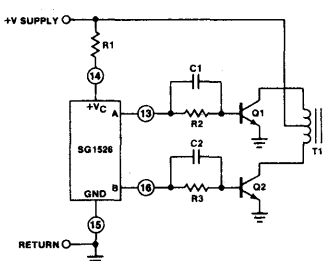


FIGURE 23
PUSH-PULL CONFIGURATION

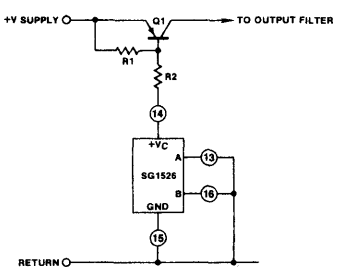


FIGURE 24
SINGLE-ENDED CONFIGURATION

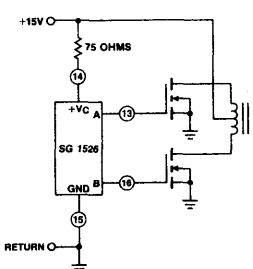
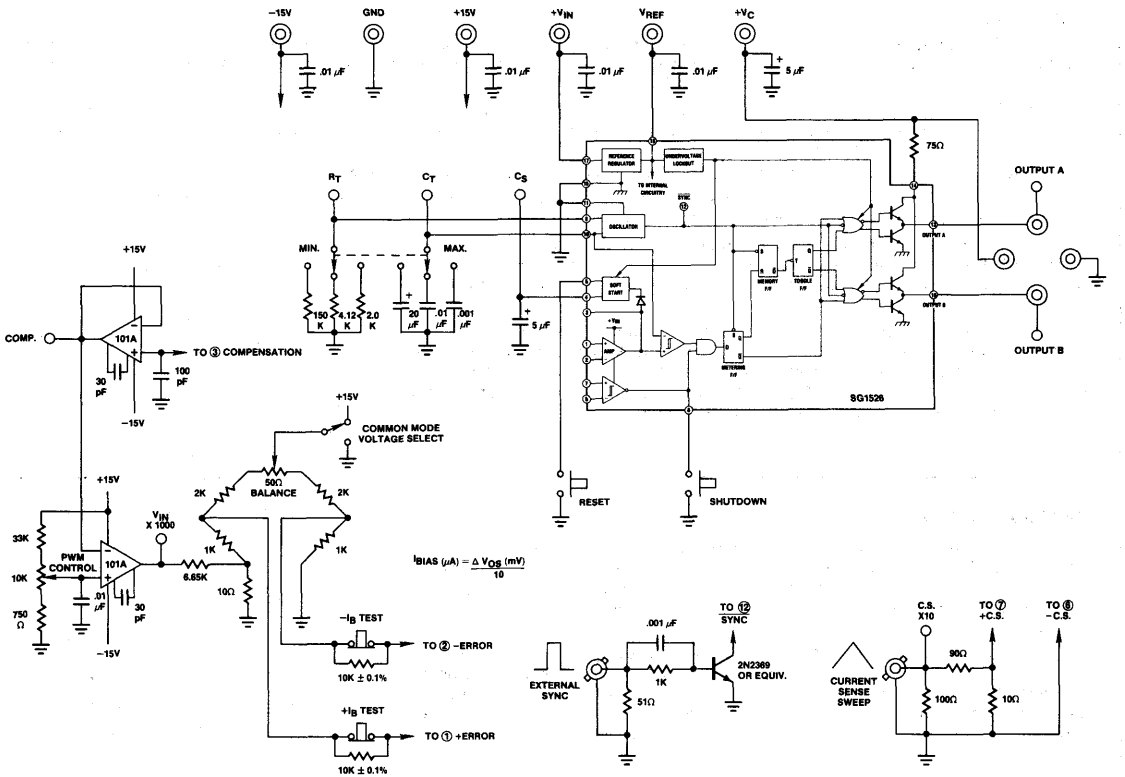


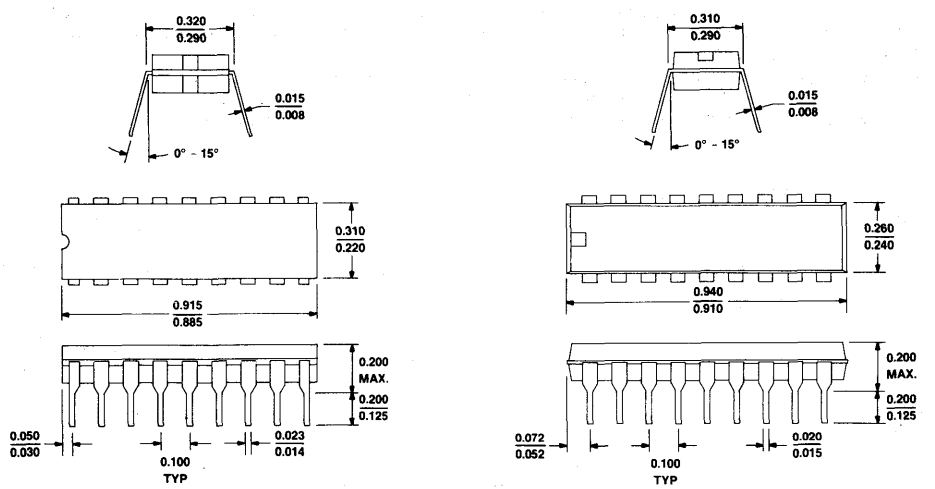
FIGURE 25
DRIVING N-CHANNEL POWER MOSFETS

Regulating Pulse Width Modulator

SG1526 LAB TEST FIXTURE



PACKAGE DIMENSIONS



J PACKAGE
18 PIN CERDIP
ALLOY 42 LEADFRAME

N PACKAGE
18 PIN PLASTIC DIP
COPPER ALLOY LEADFRAME

ADVANCED DATA
SG1526A/SG2526A/SG3526A

Performance Data described herein represent design goals. Final device specifications are subject to change.

REGULATING PULSE WIDTH MODULATOR

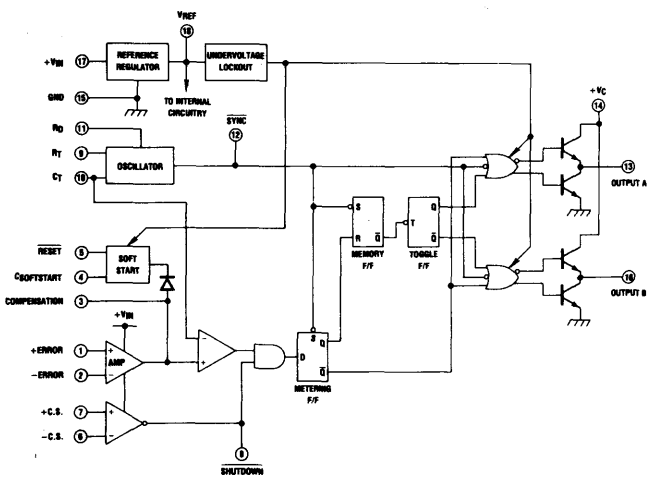
DESCRIPTION

The SG1526A high performance pulse width modulator (PWM) circuit is a direct replacement for the SG1526 in all applications and features improved parametric performance in several key areas. Included are a temperature compensated voltage reference, sawtooth oscillator, error amplifier, pulse width modulator, pulse metering and steering logic, and two low impedance power drivers. Also included are protective features such as soft-start and under-voltage lockout, digital current limiting, double pulse inhibit, a data latch for single pulse metering, adjustable deadtime, and provision for symmetry correction inputs. For ease of interface, all digital control ports are TTL and B-series CMOS compatible. Active LOW logic design allows wired-OR connections for maximum flexibility. This versatile device can be used to implement single-ended or push-pull switching regulators of either polarity, both transformerless and transformer coupled. The SG1526A is characterized for operation over the full military junction temperature range of −55°C to +150°C. The SG2526A is characterized for operation from −25°C to +150°C, and the SG 3526A is characterized for operation from 0°C to +125°C.

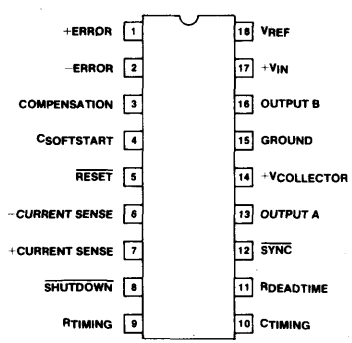
FEATURES

- **Low drain and switching currents**
- **7 to 35V operation**
- **High performance 5V ± 1% reference**
- **Low tempco 1 Hz to 400 kHz oscillator**
- **Dual 100 mA source/sink outputs**
- **Digital current limiting**
- **Double pulse suppression**
- **Programmable deadtime**
- **Undervoltage lockout**
- **Single pulse metering**
- **Programmable soft-start**
- **Wide current limit common mode range**
- **TTL/CMOS compatible logic ports**
- **Symmetry correction capability**
- **Guaranteed 6 unit synchronization**

BLOCK DIAGRAM

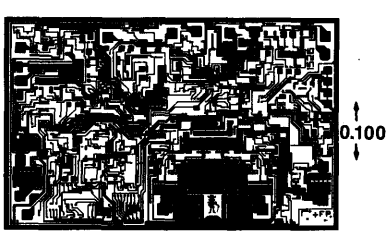


CONNECTION DIAGRAM (TOP VIEW)



J PACKAGE
TO-116 STYLE

CHIP LAYOUT



ORDER INFORMATION

Part Number	Junction Temperature Range	Package
SG1526AJ	−55°C to +150°C	18-pin Ceramic DIP
SG2526AJ	−25°C to +150°C	18-pin Ceramic DIP
SG3526AJ	0°C to +125°C	18-pin Ceramic DIP
SG3526AN	0°C to +125°C	18-pin Plastic DIP

Regulating Pulse Width Modulator

ABSOLUTE MAXIMUM RATINGS (Note 1)

Input Voltage (+VIN)	+40V	Power Dissipation at T_A = +25°C (Note 2)	1000 mW
Collector Supply Voltage (+ VC)	+40V	Thermal Resistance: junction to ambient	100°C/W
Logic Inputs	−0.3V to +5.5V	Power Dissipation at T_C = +25°C (Note 3)	3000 mW
Analog Inputs	−0.3V to +VIN	Thermal Resistance: junction to case	42°C/W
Source/Sink Load Current (each output)	200 mA	Operating Junction Temperature	+150°C
Reference Load Current	50 mA	Storage Temperature Range	−65°C to +150°C
Logic Sink Current	15 mA	Lead Temperature (soldering, 10 seconds)	+300°C

Note 1. Values beyond which damage may occur.
Note 2. Derate at 10 mW/°C for ambient temperaures above +50°C.
Note 3. Derate at 24 mW/°C for case temperatures above +25°C.

RECOMMENDED OPERATING CONDITIONS (Note 4)

Input Voltage	+ 7V to + 35V	Oscillator Timing Capacitor	1nF to 20μF
Collector Supply Voltage	+4.5V to +35V	Available Deadtime Range at 40kHz	3% to 50%
Sink/Source Load Current (each output)	0 to 100 mA	Operating Junction Temperature Range	
Reference Load Current	− 5 to 20 mA	SG1526A	−55°C to +150°C
Oscillator Frequency Range	1 Hz to 400 kHz	SG2526A	−25°C to +150°C
Oscillator Timing Resistor	2 kΩ to 150 kΩ	SG3526A	0°C to +125°C

Note 4. Range over which the device is functional and parameter limits are guaranteed.

ELECTRICAL CHARACTERISTICS

(+VIN = 15V, and over operating junction temperature, unless otherwise specified)

PARAMETER	CONDITIONS	SG1526A/2526A			SG3526A			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
REFERENCE SECTION (Note 5)								
Output Voltage	T_j = +25°C	4.95	5.00	5.05	4.90	5.00	5.10	V
Line Regulation	+VIN = 7 to 35V		2	10		2	15	mV
Load Regulation	I_L = −5 to +20 mA		5	10		5	20	mV
Temperature Stability	Over Operating T_j		15	50		15	50	mV
Total Output Voltage Range	Over Recommended Operating Conditions	4.90	5.00	5.10	4.85	5.00	5.15	V
Short Circuit Current	VREF = 0V	25	50	100	25	50	100	mA
UNDERVOLTAGE LOCKOUT								
$\overline{\text{RESET}}$ Output Voltage	VREF = 3.8V		0.2	0.4		0.2	0.4	V
$\overline{\text{RESET}}$ Output Voltage	VREF = 4.8V	2.4	4.8		2.4	4.8		V
OSCILLATOR SECTION (Note 6)								
Initial Accuracy	T_j = +25°C		±3	±8		±3	±8	%
Voltage Stability	+VIN = 7 to 35V		0.5	1		0.5	1	%
Temperature Stability	Over Operating T_j		1	3		1	3	%
Minimum Frequency	R_T = 150 kΩ, C_T = 20 μF			1			1	Hz
Maximum Frequency	R_T = 2 kΩ, C_T = 1.0 nF	400			400			kHz
Sawtooth Peak Voltage	+VIN = 35V		3.0	3.5		3.0	3.5	V
Sawtooth Valley Voltage	+ VIN = 7V	0.5	1.0		0.5	1.0		V

Note 5. I_L = 0 mA.
Note 6. FOSC = 40 kHz (R_T = 4.12 kΩ ± 1%, C_T = .01 μF ± 1%, R_D = 0Ω

Regulating Pulse Width Modulator

ELECTRICAL CHARACTERISTICS (continued)

PARAMETER	CONDITIONS	SG1526A/2526A			SG3526A			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
ERROR AMPLIFIER SECTION (Note 7)								
Input Offset Voltage	$R_S \leq 2\ k\Omega$		2	5		2	10	mV
Input Bias Current			−350	−1000		−350	−2000	nA
Input Offset Current			35	100		35	200	nA
DC Open Loop Gain	$R_L \geq 10$ Meg Ω	64	72		60	72		dB
High Output Voltage	Vpin1 −Vpin2≥150mV, $I_{source} = 100\mu A$	3.6	4.2		3.6	4.2		V
Low Output Voltage	Vpin2 −Vpin1≥150mV, $I_{sink} = 100\mu A$		0.2	0.4		0.2	0.4	V
Common Mode Rejection	$R_S \leq 2k\Omega$	70	94		70	94		dB
Supply Voltage Rejection	$+V_{IN}$ = 12 to 18V	66	80		66	80		dB
P.W.M. COMPARATOR (Note 6)								
Minimum Duty Cycle	$V_{compensation} = +0.4V$			0			0	%
Maximum Duty Cycle	$V_{compensation} = +3.6V$	45	49		45	49		%
DIGITAL PORTS ($\overline{SYNC}$, $\overline{SHUTDOWN}$, and $\overline{RESET}$)								
HIGH Ouput Voltage	$I_{source} = 40\ \mu A$	2.4	4.0		2.4	4.0		V
LOW Output Voltage	$I_{sink} = 3.6$ mA		0.2	0.4		0.2	0.4	V
HIGH Input Current	$V_{IH} = +2.4V$		−125	−200		−125	−200	μA
LOW Input Current	$V_{IL} = +0.4V$		−225	−360		−225	−360	μA
CURRENT LIMIT COMPARATOR (Note 8)								
Sense Voltage	$R_S \leq 50\ \Omega$	90	100	110	80	100	120	mV
Input Bias Current			−3	−10		−3	−10	μA
SOFT-START SECTION								
Error Clamp Voltage	$\overline{RESET} = +0.4V$		0.1	0.4		0.1	0.4	V
C_S Charging Current	$\overline{RESET} = +2.4V$	50	100	150	50	100	150	μA
OUTPUT DRIVERS (Each Output) (Note 9)								
HIGH Output Voltage	$I_{source} = 20$ mA	12.5	13.5		12.5	13.5		V
	$I_{source} = 100$ mA	12	13		12	13		V
LOW Output Voltage	$I_{sink} = 20$ mA		0.2	0.3		0.2	0.3	V
	$I_{sink} = 100$ mA		1.2	2.0		1.2	2.0	V
Collector Leakage	$V_C = 40V$		50	150		50	150	μA
Rise Time	$C_L = 1000$ pF		0.3	0.6		0.3	0.6	μSec
Fall Time	$C_L = 1000$ pF		0.1	0.2		0.1	0.2	μSec
POWER CONSUMPTION (Note 10)								
Standby Current	$\overline{SHUTDOWN} = +0.4V$		14	20		14	20	mA

Note 7. $V_{CM} = 0$ to $+5.2V$

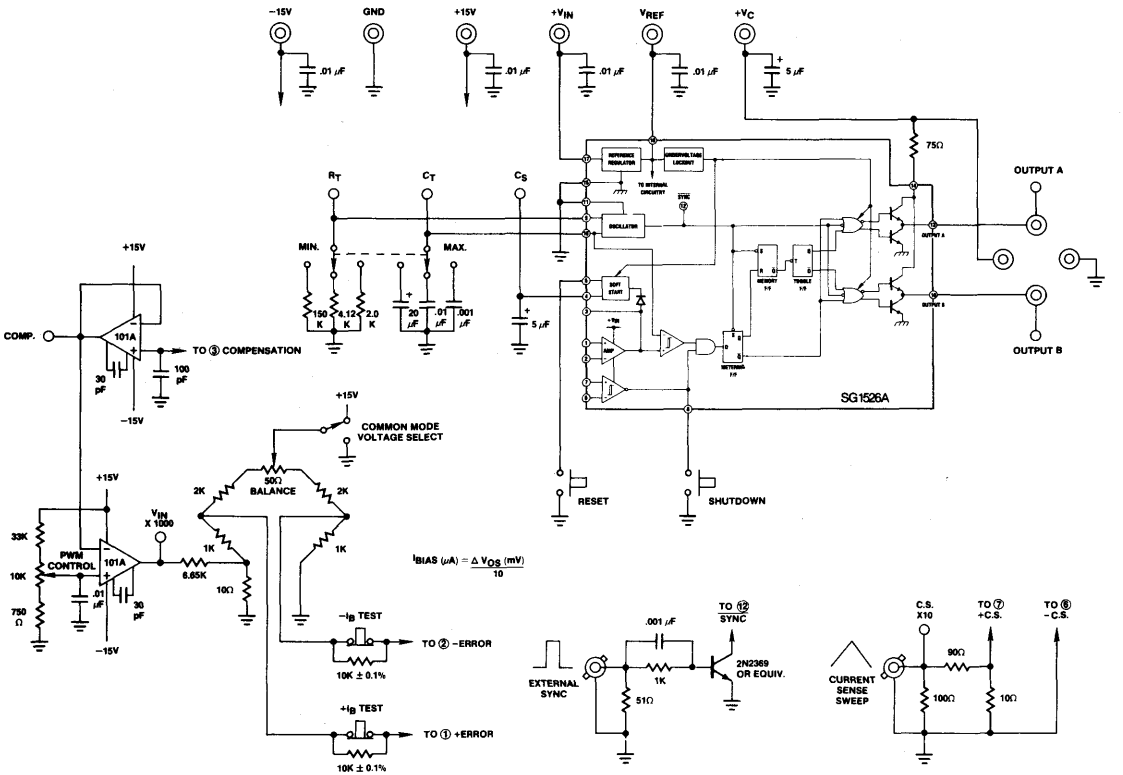
Note 8. $V_{CM} = 0$ to $V_{IN} - 2.5V$

Note 9. $V_C = +15V$

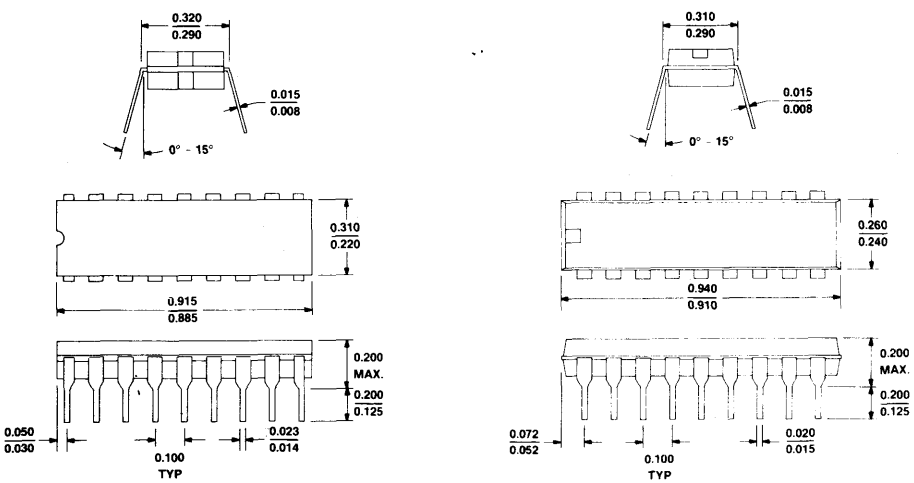
Note 10. $+V_{IN} = +35V$, $R_T = 4.12k\Omega$

Regulating Pulse Width Modulator

SG1526A LAB TEST FIXTURE



PACKAGE DIMENSIONS



J PACKAGE
18 PIN CERDIP
ALLOY 42 LEADFRAME

N PACKAGE
18 PIN PLASTIC DIP
COPPER ALLOY LEADFRAME

ADVANCED DATA
SG1540/SG2540/SG3540

Performance data described herein represent design goals. Final device specifications are subject to change.

OFF-LINE START-UP CONTROLLER

DESCRIPTION

The SG1540 is an integrated circuit designed to efficiently provide start-up power from a high-voltage bus to a PWM control circuit in a switching power supply. When used on the primary side, it reduces start-up current to less than 1 mA and allows any standard PWM control circuit to be used as a primary-side controller. When used to power a controller on the secondary side, it effectively eliminates the need for a heavy 50/60 Hz line transformer with its associated low frequency magnetic fields.

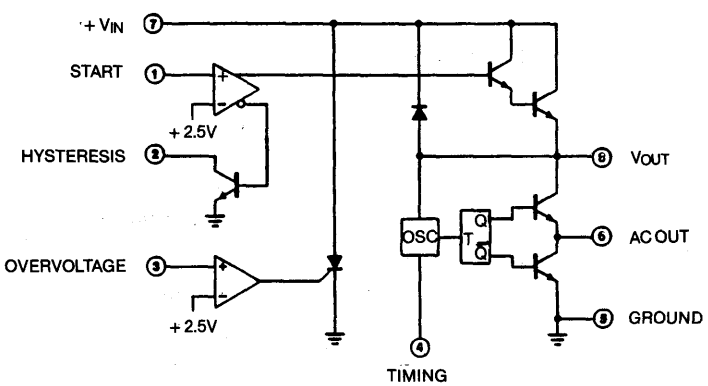
The circuit consists of three sections: a micropower bandgap comparator/power switch referenced to +2.5 volts which isolates the start-up capacitor from its load; a high frequency square-wave oscillator with 200 mA totem-pole output for driving an isolation transformer; and a second bandgap comparator with latching crowbar to protect against overvoltage faults while starting or running.

The SG1540 is specified for operation over the full military ambient temperature range of −55°C to +125°C. The SG2540 is characterized for the industrial range of −25°C to +85°C, and the SG3540 is designed for the commercial range of 0°C to +70°C.

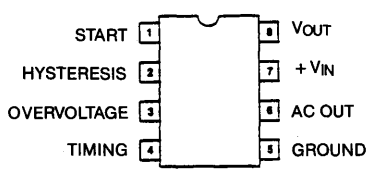
FEATURES

- **Eliminates bulky 50/60 Hz transformer**
- **Minimizes high voltage bleeder current**
- **Usable with primary or secondary control PWM**
- **Programmable start voltage and hysteresis**
- **Programmable overvoltage latch**

BLOCK DIAGRAM



CONNECTION DIAGRAM (TOP VIEW)



Y or M PACKAGE
TO-116 STYLE

ORDERING INFORMATION

Part Number	Temperature Range	Package
SG1540Y	−55°C to +125°C	8 Pin Ceramic DIP
SG2540Y	−25°C to + 85°C	8 Pin Ceramic DIP
SG3540Y	0°C to + 70°C	8 Pin Ceramic DIP
SG3540M	0°C to + 70°C	8 Pin Plastic DIP

DC MOTOR PULSE WIDTH MODULATOR

DESCRIPTION

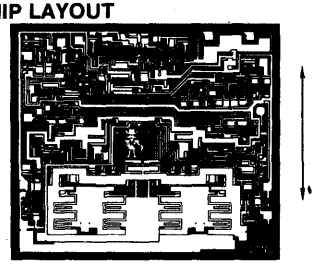
The SG1731 is a pulse width modulator circuit designed specifically for DC motor control. It provides a bi-directional pulse train output in response to the magnitude and polarity of an analog error signal input. The device is useful as the control element in motor-driven servo systems for precision positioning and speed control, as well as in audio modulators and amplifiers using carrier frequencies to 350 kHz.

The circuit contains a triangle waveform oscillator, a wideband operational amplifier for error voltage generation, a summing/scaling network for level-shifting the triangle waveform, externally programmable PWM comparators and dual ±100 mA, ±22 volt totem pole drivers with commutation diodes for full bridge output. A $\overline{\text{SHUTDOWN}}$ terminal forces the drivers into a floating high-impedance state when driven LOW. Supply voltage to the control circuitry and to the output drivers may be from either dual positive and negative supplies, or single-ended.

FEATURES

- **±3.5 to ±15 volt control supply**
- **±2.5 to ±22 volt driver supply**
- **50Hz source/sink output drivers**
- **5kHz to 350kHz oscillator range**
- **High slew rate error amplifier**
- **Adjustable deadband operation**
- **Digital $\overline{\text{SHUTDOWN}}$ input**

CHIP LAYOUT



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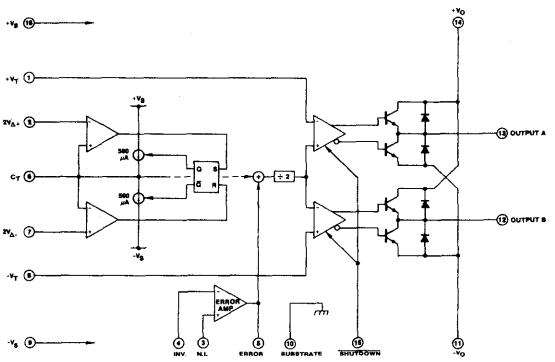
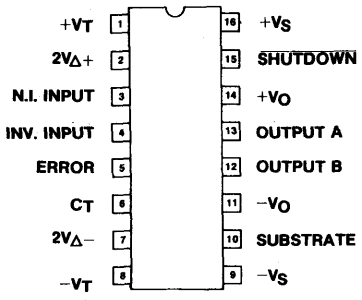


CONNECTION DIAGRAM

TOP VIEW



J PACKAGE
TO-116 CERDIP

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage ($\pm V_S$)	±18V	Power Dissipation at T_A = +25°C (Note 2)	1000 mW
Analog Inputs	$\pm V_S$	Thermal Resistance, junction to ambient	125°C/W
Output Driver Voltage ($\pm V_O$)		Power Dissipation at T_C = +25°C (Note 3)	3000 mW
SG1731/SG2731	±35V	Thermal Resistance, junction to case	42°C/W
SG3731	±25V	Operating Junction Temperature	+150°C
Source/Sink Load Current (Continuous)	200 mA	Storage Temperature Range	−65°C to +150°C
Source/Sink Load Current (Peak, 1μSec)	400 mA	Lead Temperature (Soldering, 10 seconds)	+300°C

Note 1. Values beyond which damage may occur.
Note 2. Derate at 8 mW/°C for ambient temperatures above +25°C.
Note 3. Derate at 24 mW/°C for case temperatures above +25°C.

RECOMMENDED OPERATING CONDITIONS (Note 4)

Supply Voltage Range	±3.5V to ±15V	Oscillator Frequency Range	5 kHz to 350 kHz
Error Amp Common Mode Range	±0.5V to ±12V	Oscillator Voltage (Peak-to-Peak)	1V to 10V
Output Driver Voltage Range		Oscillator Timing Capacitor (C_T)	200 pF to 0.5 μF
SG1731/SG2731	±2.5V to ±22V	Operating Junction Temperature Range	
SG3731	±2.5V to ±22V	SG1731	−55°C to +125°C
Source/Sink Load Current (Continuous)	100 mA	SG2731	−25°C to +85°C
Source/Sink Load Current (Peak, 1μSec)	200 mA	SG3731	0°C to +70°C

Note 4. Range over which the device is functional and parameter limits are guaranteed.

ELECTRICAL CHARACTERISTICS ($V_S = V_O = \pm 15V$, and over operating junction temperature, unless otherwise specified)

PARAMETER	CONDITIONS	SG1731/SG2731			SG3731			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
OSCILLATOR SECTION								
C_T Charging Current	T_J = +25°C	450	500	550	400	500	600	μA
	Over Operating Temperature	400		600	350		650	μA
$2V_{\Delta\pm}$ Input Bias Current	V_{CM} = −5V to +5V		−5			−5		μA
ERROR AMPLIFIER								
Input Offset Voltage			1	6		2	10	mV
Input Bias Current			0.2	1.0		0.4	2.0	μA
Input Offset Current			30	500		60	800	nA
Open Loop Voltage Gain	R_L = 2K	80	106		75	106		dB
Output Voltage Swing	R_L = 2K	±10	±13		±10	±13		V
Short Circuit Output Current	V_{ERROR} = 0V	10		35	10		35	mA
Slew Rate	Unity Gain Inverting		15			15		V/μSec
Unity Gain Bandwidth	10K Feedback Resistance		1			1		MHz
PWM COMPARATORS								
$\pm V_T$ Input Bias Current	V_{CM} = −3V to +3V		1			1		μA
$\overline{\text{SHUTDOWN}}$ HIGH Voltage	Pin 15 Open			15			15	V
$\overline{\text{SHUTDOWN}}$ LOW Current	Pin 15 = $-V_S$		−0.6	−1.0		−0.6	−1.0	mA
OUTPUT DRIVERS (Each Output) (Note 5)								
HIGH Output Voltage	I_{SOURCE} = 20 mA		+21			+21		V
	I_{SOURCE} = 100 mA	+19	+20		+19	+20		V
LOW Output Voltage	I_{SINK} = 20 mA		−21			−21		V
	I_{SINK} = 100 mA		−20	−19		−20	−19	V
Rise Time	C_L = 1000 pF		200			200		nSec
Fall Time	C_L = 1000 pF		200			200		nSec
POWER CONSUMPTION (Note 5)								
V_S Supply Current	F_{OSC} = 50kHz		7			7		mA
V_O Supply Current	$\overline{\text{SHUTDOWN}}$ LOW		1			1		mA

Note 5. $\pm V_O = \pm 22$ volts.

APPLICATION NOTES

Supply Voltage

The SG1731 requires a supply voltage for the control circuitry (V_S) and for the power output drivers (V_O). Each supply may be either balanced positive and negative with respect to ground, or single-ended. The only restrictions are:

1. The voltage between $+V_S$ and $-V_S$ must be at least 7.0 volts, but no more than 30 volts.
2. The voltage between $+V_O$ and $-V_O$ must be at least 5.0 volts; but no more than 44 volts.
3. $+V_O$ must be at least 5 volts more positive than $-V_S$. This eliminates the combination of a single-ended positive control supply with a single-ended negative driver supply.

Substrate Connection

The substrate connection (Pin 10) must *always* be connected to either $-V_S$ or $-V_O$, whichever is more negative. The substrate must also be well bypassed to ground with a high quality capacitor.

Oscillator

The triangle oscillator consists of two voltage comparators, a set/reset flip-flop, a bi-directional 500 μA current source, and an external timing capacitor C_T. A positive reference voltage ($2V_{\Delta+}$) applied to Pin 2 determines the positive peak value of the triangle, and a negative reference voltage ($2V_{\Delta-}$) at Pin 7 sets the negative peak value of the triangle waveform.

Since the value of the internal current source is fixed at a nominal $\pm 500\ \mu A$, the oscillator period is a function of the selected peak-to-peak voltage excursion and the value of C_T. The theoretical expression for the oscillator period is:

$$T_{OSC} = \frac{2C_T\ dV}{5 \times 10^{-4}} \qquad \text{(Eq. 1)}$$

where C_T is the timing capacitor in Farads and dV is V_{OSC} in volts peak-to-peak.

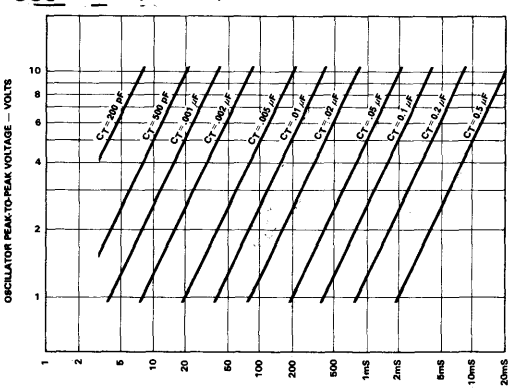


Figure 1. SG1731 Oscillator Period vs. VOSC and CT

As a design aid, the solutions to Equation 1 over the recommended range of T_{OSC} and V_{OSC} are given in graphic form in Figure 1. The lower limit on T_{OSC} is 2.85 μSec, corresponding to a maximum frequency of 350 kHz.

The maximum value of V_{OSC}, $(2V_{\Delta+}) - (2V_{\Delta-})$, is 10 volts peak-to-peak for linear waveforms.

Error Amplifier

The error amplifier of the SG1731 is a conventional internally-compensated operational amplifier with low output impedance. All of the usual feedback and frequency compensation techniques may be used to control the closed-loop gain characteristics. The control supply voltage $\pm V_S$ will determine the input common mode range and output voltage swing; both will extend to within 3 volts of the V_S supply.

Pulse Width Modulation

Pulse width modulation occurs by comparing the triangle waveform to a fixed upper ($+V_T$) and lower ($-V_T$) threshold voltage. A crossing above the upper threshold causes Output A to switch to the HIGH state, and a crossing below the lower threshold causes Output B to switch to the HIGH state.

Threshold crossings are generated by shifting the triangle waveform up and down with the error voltage (Pin 5). A positive error voltage will result in a pulse width modulated output at Driver A (Pin 13). Similarly, a negative error voltage produces a pulse train at Driver B (Pin 12). Figure 2 illustrates this process for the case where $V_{\Delta+}$ is greater than $+V_T$.

It is important to note that the triangle shifting circuit also attenuates the waveform seen at C_T by a factor of 2. This results in a waveform at the PWM comparators with a positive peak of $V_{\Delta+}$ and a negative peak of $V_{\Delta-}$, and must be taken into account when selecting the values for $+V_T$ and $-V_T$.

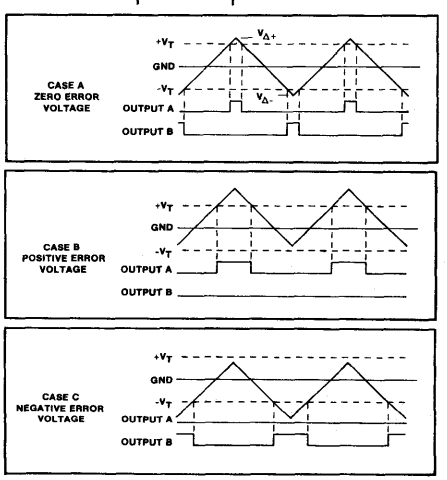


Figure 2. Pulse Width Modulation with no Deadband

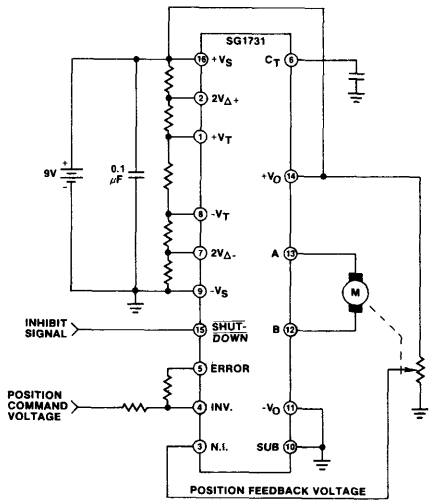


Figure 3. In this simple battery-powered position servo, the control supply and driver supply are both single-ended positive with respect to ground.

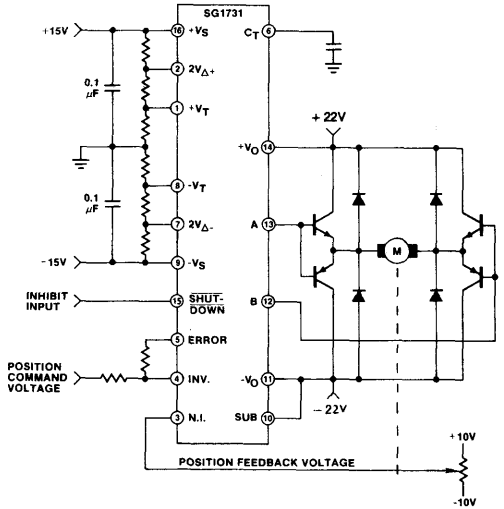


Figure 4. A high torque position servo is obtained by buffering the output drivers to obtain higher output current.

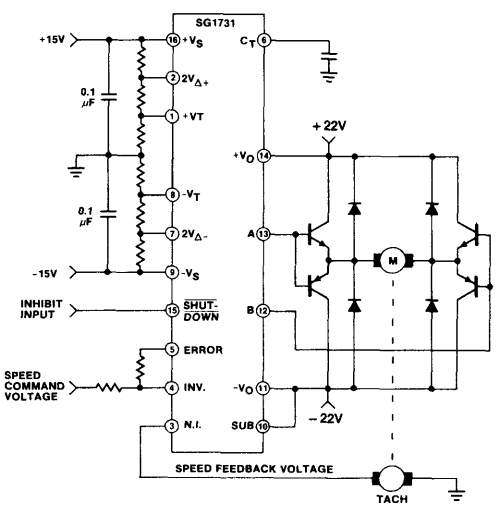


Figure 5. Bi-directional speed control results when the feedback voltage transducer is a tachometer.

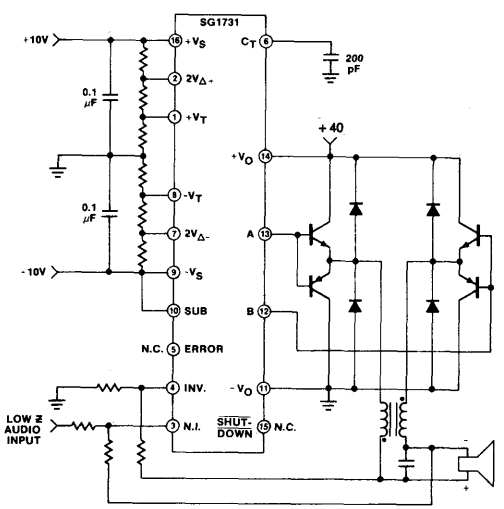


Figure 6. The two-quadrant transfer function of the SG1731 is ideal for pulse width modulated audio power amplifiers.

PROTECTION CIRCUITS

SG1542 / SG2542 / SG3542

VOLTAGE SENSING CIRCUIT

DESCRIPTION

This monolithic integrated circuit provides the control functions necessary to protect sensitive electronic circuitry from over-voltage transients or the effects of voltage regulator failure. It is designed for use with an external SCR "crowbar" for immediate shutdown of the power supply, but additionally provides logic level outputs for regulator turn-off and/or operator or system out-of-tolerance indication.

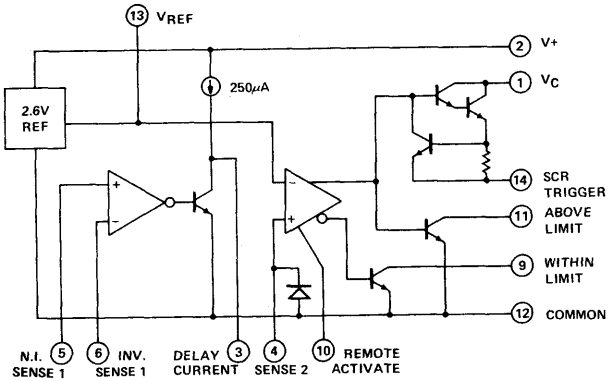
This device contains an accurate, stable 2.6 volt reference which allows the sensing threshold to be set predictably without the need for potentiometers. Uncommitted availability of both polarity inputs to the sensing comparator allows a wide flexibility of use including the ability to sense voltages less than the reference voltage. An external capacitor can be used to program an accurate time delay between fault occurrence and crowbar triggering, but this delay may be bypassed by inputing at the Sense 2 terminal or by using the remote activation capability.

For additional circuit functions, see SG1543 data sheet.

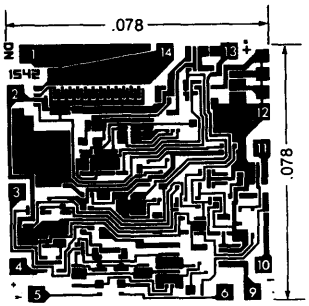
FEATURES

- **Operation from 4.5 to 40 volts**
- **Useful for either over- or under-voltage sensing**
- **Sensing threshold accurate to ±2%**
- **Built-in input hysteresis**
- **Zero to 35 volt sensing capability**
- **Programmable time delay**
- **SCR "Crowbar" drive of 200mA**
- **Remote activation capability**
- **2.6V 1% reference available**

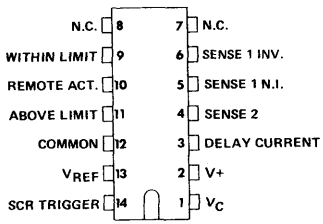
BLOCK DIAGRAM



CHIP LAYOUT



CONNECTION DIAGRAM



J, N PACKAGES (TO-116)

ABSOLUTE MAXIMUM RATINGS

Input Supply Voltage, V+	40V
Collector Supply Voltage, V_C	40V
Sense Voltage (1)	V+
Sense Voltage (2)	6.5V
Remote Activation Input Voltage	7.0V
SCR Trigger Current	300mA*
Limit Indicators Output Voltage	40V
Limit Indicators Output Sink Current	50mA

Power Dissipation (Package Limitation)	1000mW
Derate above 25° C	8.0 mW/° C
Operating Temperature Range	
SG1542	−55° C to +125° C
SG2542	−25° C to +85° C
SG3542	0° C to +70° C
Storage Temperature Range	−65° C to +150° C

*At higher input voltages, a dissipation limiting resistor, R_G, is required. See graph.

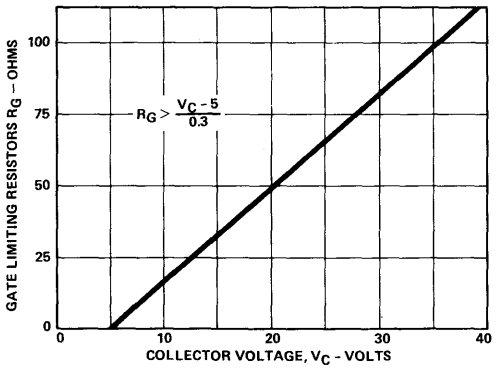
ELECTRICAL CHARACTERISTICS

(Unless otherwise stated, these specifications apply for V+ = 5 to 35V and T_J = −55° C to +125° C for the SG1542, −25° C to +85° C for the SG2542, and 0° C to +70° C for the SG3542.)

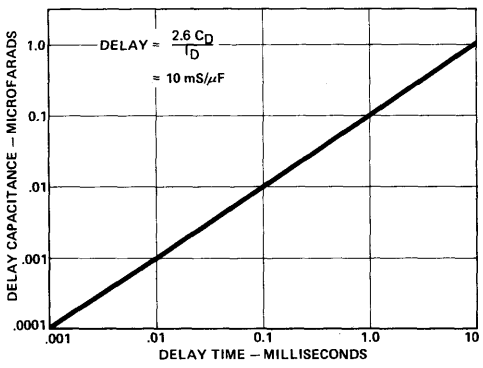
PARAMETER	CONDITIONS	SG1542/2542			SG3542			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Voltage Range	T_J = 25°C to T_{max}	4.5	—	40	4.5	—	40	V
Input Voltage Range	T_{min} to T_{max}	4.7	—	40	4.7	—	40	V
Supply Current	V+ = 40V, Outputs open	—	5	7	—	5	10	mA
Reference Voltage	T_J = 25°C	2.58	2.60	2.62	2.55	2.60	2.65	V
Reference Voltage	Over Temp. Range	2.55	—	2.65	2.50	—	2.70	V
Line Regulation	V+ = 5 to 40V	—	1	5	—	1	5	mV
Load Regulation	I_{REF} = 0 to 10mA	—	1	10	—	1	10	mV
Short Circuit Current	V_{REF} = 0	12	25	40	12	25	40	mA
Temperature Stability		—	.005	—	—	.005	—	%/°C
Sense 1 Offset Voltage	Sense 1 (+) rising	-10	0	+10	-20	0	+20	mV
Sense 1 Offset Voltage	Sense 1 (+) falling	-35	-25	-15	-50	-25	0	mV
Sense 1 Common Mode		0	—	(V+) −3	0	—	(V+) −3	V
Sense 1 Bias Current		—	-0.3	-1.0	—	-0.3	-1.0	μA
Sense 2 Threshold		2.50	2.60	2.70	2.50	2.60	2.70	V
Sense 2 Bias Current		—	1.0	10	—	1.0	10	μA
Delay Current		200	250	300	200	250	300	μA
Remote Activation Current		—	120	180	—	120	180	μA
Remote Act. Threshold		0.8	1.0	2.0	0.8	1.0	2.0	V
Peak Output Current	V_C = 5V, R_G = 0, V_O = 0	100	200	400	100	200	400	mA
Peak Output Voltage	I_O = 100mA	V_{IN} −2	V_{IN} −1.6	—	V_{IN} −2	V_{IN} −1.6	—	V
Output Off Voltage	V+ = V_C = 40V	—	0	0.1	—	0	0.1	V
Limit Indicators V_{SAT}	I_L = -10mA	—	0.2	0.5	—	0.2	0.5	V
Limit Indicators Leakage	V_{IND} = 40V	—	.01	1.0	—	.01	1.0	μA
Propagation Delay	T_O Ind., T_J = 25°C	—	500	—	—	500	—	nS
Propagation Delay	T_O Trigger, T_J = 25°C	—	500	—	—	500	—	nS
Output Current Rise Time	R_L = 50Ω, T_J = 25°C	—	400	—	—	400	—	mA/μS

TYPICAL CHARACTERISTICS

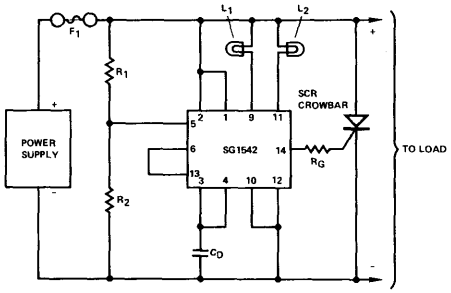
MINIMUM GATE CURRENT LIMITING RESISTANCE



ACTIVATION DELAY VS. CAPACITOR VALUE



BASIC OVER-VOLTAGE PROTECTION CIRCUIT CONFIGURATION



F_1 = Only necessary if power supply is not current limited

$V_{TRIP} = \left[\frac{2.6V\ (R_1 + R_2)}{R_2}\right]$, $R_2 \leq 100k\Omega$

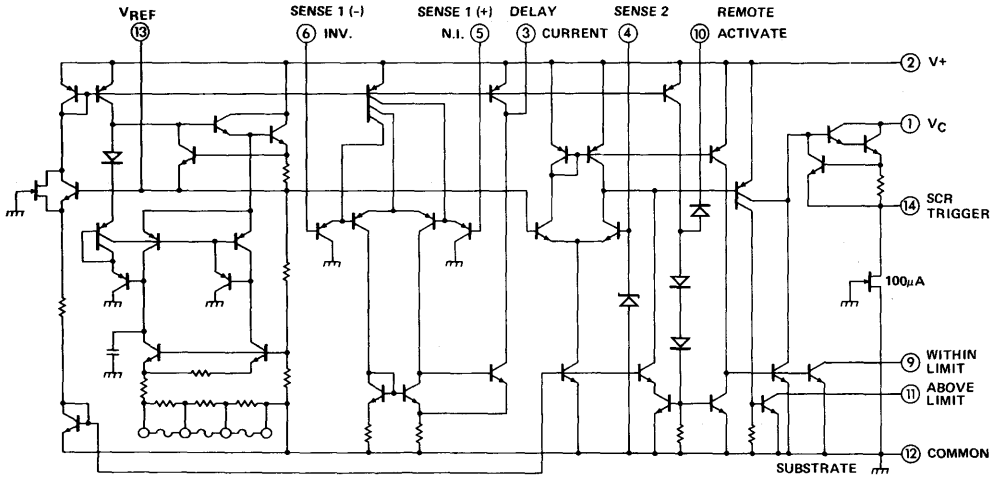
$t_D = 10^4\ C_D$

$R_G > \frac{V_C - 5}{0.3}$

L_1, L_2 = Indicator selected for max. current $\approx$ 10mA @ V_{TRIP}

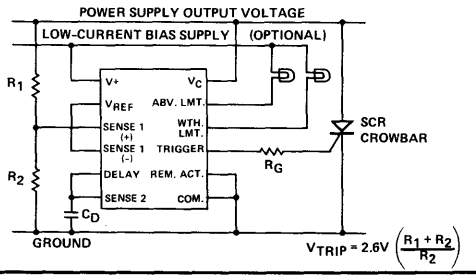
SCR = Selected for max. peak current capability

SG1542 SIMPLIFIED SCHEMATIC DIAGRAM

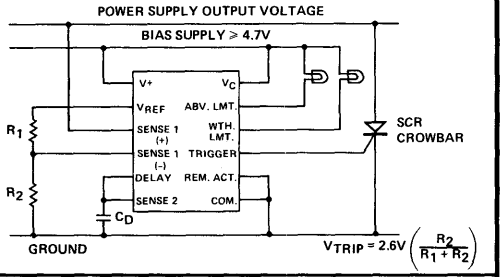


APPLICATIONS

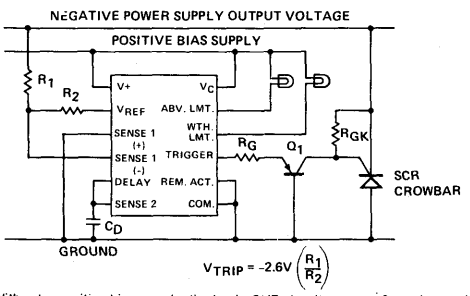
OVER-VOLTAGE SENSING FOR VOLTAGES ABOVE 2.6 VOLTS



OVER-VOLTAGE SENSING FOR VOLTAGES LESS THAN 2.6 VOLTS

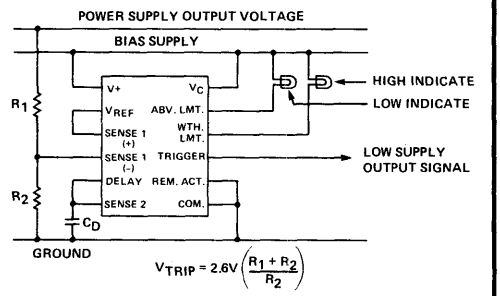


OVER-VOLTAGE SENSING FOR NEGATIVE OUTPUT VOLTAGES*

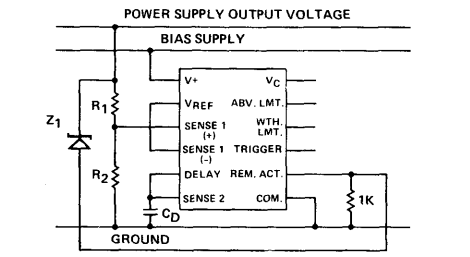


*Without a positive bias supply, the basic OVP circuit on page 3 can be used equally well with either positive or negative voltages.

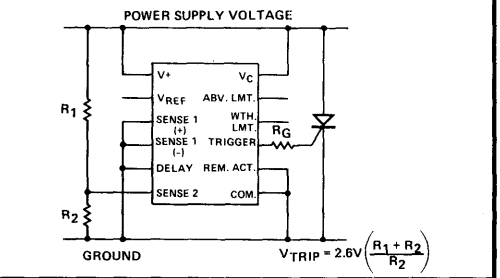
UNDER-VOLTAGE SENSING



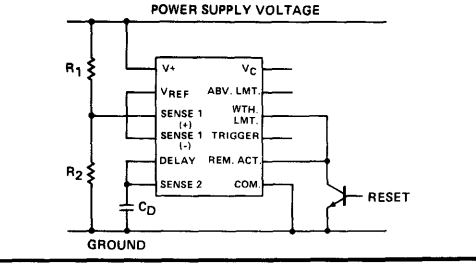
DELAYED THRESHOLD SENSE PLUS IMMEDIATE TRIP FOR HIGH OVER-VOLTAGE



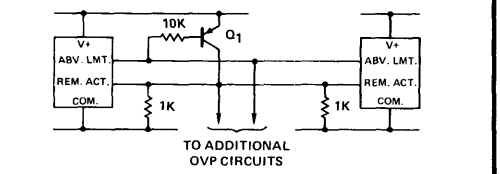
OVER-VOLTAGE SENSING WITH MINIMUM TIME DELAY



OVER-VOLTAGE LATCH WITH RESET



INTERCONNECTING MULTIPLE SG1542'S



Q1 must provide ≥ 2mA for each OVP circuit. With this arrangement, activation of any circuit will activate all. For a master-slave relationship, the WITHIN LIMIT terminal of the master may be directly connected to the REMOTE ACTIVATE terminals of all the slaves.

See Applications Notes for additional information.

SG1543 / 2543 / 3543

Power Supply Output Supervisory Circuit

DESCRIPTION

This monolithic integrated circuit contains all the functions necessary to monitor and control the output of a sophisticated power supply system. Over-voltage (O.V.) sensing with provision to trigger an external SCR "crowbar" shutdown; an under-voltage (U.V.) circuit which can be used to monitor either the output or to sample the input line voltage; and a third op amp/comparator usable for current sensing (C.L.) are all included in this IC, together with an independent, accurate reference generator.

Both over and under-voltage sensing circuits can be externally programmed for minimum time duration of fault before triggering. All functions contain open collector outputs which can be used independently or wire-or'ed together, and although the SCR trigger is directly connected only to the over-voltage sensing circuit, it may be optionally activated by any of the other outputs, or from an external signal. The O.V. circuit also includes an optional latch and external reset capability.

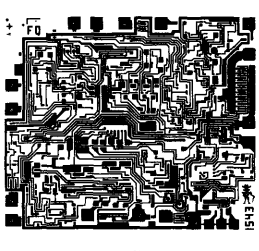
The current sense circuit may be used with external compensation as a linear amplifier or as a high-gain comparator. Although nominally set for zero input offset, a fixed threshold may be added with an external resistor. Instead of current limiting, this circuit may also be used as an additional voltage monitor.

The reference generator circuit is internally trimmed to eliminate the need for external potentiometers and the entire circuit may be powered directly from either the output being monitored or from a separate bias voltage.

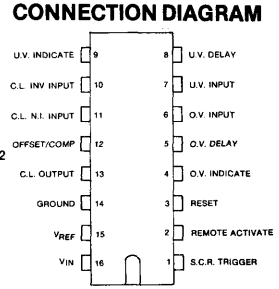
FEATURES

- **Over-voltage, under-voltage, and current sensing circuits all included**
- **Reference voltage trimmed to 1% accuracy**
- **SCR "Crowbar" drive of 300 mA**
- **Programmable time delays**
- **Open-collector outputs and remote activation capability**
- **Total standby current less than 10mA**

CHIP LAYOUT



CONNECTION DIAGRAM



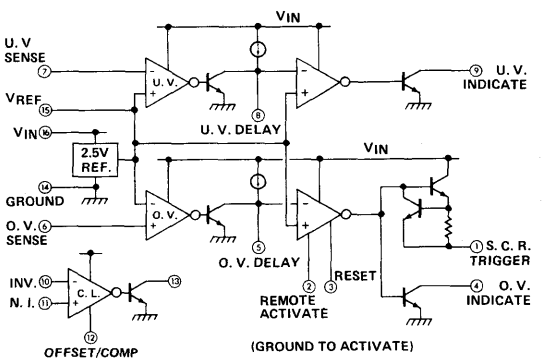
J-Package
TO-116 Cerdip

ABSOLUTE MAXIMUM RATINGS

Input Supply Voltage, V_{IN}	40V
Sense Inputs	V_{IN}
SCR Trigger Current	400 mA*
Indicator Output Voltage	40V
Indicator Output Sink Current	50mA
Power Dissipation (Package Limitation)	1000mW
Derate Above 25° C	8.0mW/° C
Operating Temperature Range	
SG1543	−55° C to +125° C
SG2543	−25° C to +85° C
SG3543	0° C to +70° C
Storage Temperature Range	−65° C to +150° C

* At higher input voltages, a dissipation limiting resistor, RG, is required.

BLOCK DIAGRAM



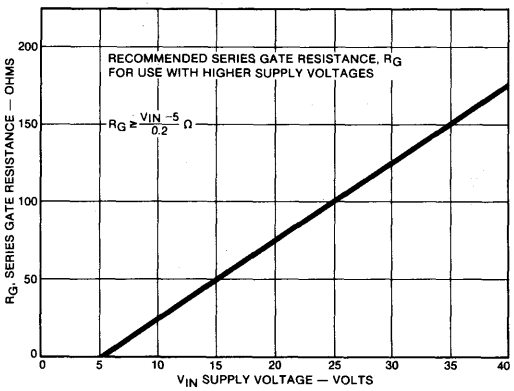
ELECTRICAL CHARACTERISTICS

(Unless otherwise stated, these specifications apply for T_J = −55° C to +125° C for the SG1543, −25° C to +85° C for the SG2543 and 0° C to +70° C for the SG3543; and for V_{IN} = 10 Volts.

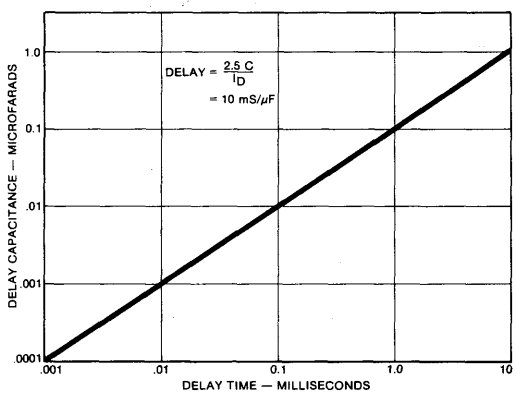
PARAMETER	CONDITIONS	SG1543/2543			SG3543			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Voltage Range	T_J = 25°C to T_{max}	4.5	–	40	4.5	–	40	V
Input Voltage Range	T_{min} to T_{max}	4.7	–	40	4.7	–	40	V
Supply Current	T_J = 25°C, V_{IN} = 40V	–	7	10	–	7	10	mA
REFERENCE SECTION (Pins 15, 16)								
Output Voltage	T_J = 25°C	2.48	2.50	2.52	2.45	2.50	2.55	V
Output Voltage	Over Temp. Range	2.45	–	2.55	2.40	–	2.60	V
Line Regulation	V_{IN} = 5 to 30V	–	1	5	–	1	5	mV
Load Regulation	I_{REF} = 0 to 10 mA	–	1	10	–	1	10	mV
Short Circuit Current	V_{REF} = 0	12	25	40	12	25	40	mA
Temperature Stability		–	50	–	–	50	–	ppm/°C
SCR TRIGGER SECTION (Pins 1, 2, 3)								
Peak Output Current	V_{IN} = 5V, R_G = 0, V_O = 0	100	200	400	100	200	400	mA
Peak Output Voltage	V_{IN} = 15V, I_O = 100mA	12	13	–	12	13	–	V
Output Off Voltage	V_{IN} = 40V	–	0	0.1	–	0	0.1	V
Remote Activate Current	Pin 2 = Gnd	–	.4	.8	–	.4	.8	mA
Remote Activate Voltage	Pin 2 open	–	2	6	–	2	6	V
Reset Current	Pin 3 = Gnd, Pin 2 = Gnd	–	.4	.8	–	.4	.8	mA
Reset Voltage	Pin 3 open, Pin 2 = Gnd	–	2	6	–	2	6	V
Output Current Rise Time	R_L = 50Ω	–	400	–	–	400	–	mA/μS
Prop. Delay from Pin 2	T_J = 25°C, $V_{(Pin\ 2)}$ = 0.4V	–	300	–	–	300	–	nS
Prop. Delay from Pin 6	C_D = 0, $V_{(Pin\ 6)}$ = 2.7V,	–	500	–	–	500	–	nS
COMPARATOR SECTIONS (Pins 6, 7, 5, 8, 4, 9)								
Input Threshold (Input voltage rising on Pin 6 and falling on Pin 7)	T_J = 25°C	2.45	2.50	2.55	2.40	2.50	2.60	V
	Over Temp. Range	2.40	–	2.60	2.35	–	2.65	V
Input Hysteresis		–	25	–	–	25	–	mV
Input Bias Current	Sense input = 0V	–	0.3	1.0	–	0.3	1.0	μA
Delay Saturation		–	0.2	0.5	–	0.2	0.5	V
Delay High Level		–	6	8	–	6	8	V
Delay Charging Current	V_D = 0V	200	250	300	200	250	300	μA
Indicate Saturation	I_L = -10mA	–	0.2	0.5	–	0.2	0.5	V
Indicate Leakage	V_{IND} = 40V	–	.01	1.0	–	.01	1.0	μA
Propagation Delay	$V_{(Pin\ 6)}$ = 2.7V, $V_{(Pin\ 7)}$ = 2.3V, T_J = 25°C; C_D = 0	–	400	–	–	400	–	nS
	$V_{(Pin\ 6)}$ = 2.7V, $V_{(Pin\ 7)}$ = 2.3V, T_J = 25°C; C_D = 1μf	–	10	–	–	10	–	mS
CURRENT LIMIT SECTION (Pins 10, 11, 12, 13)								
Input Voltage Range		0	–	$(V_{IN}-3V)$	0	–	$(V_{IN}-3V)$	V
Input Bias Current	Pin 12 open, V_{CM} = 0V	–	0.3	1.0	–	0.3	1.0	μA
Input Offset Voltage	Pin 12 open, V_{CM} = 0V	–	0	10	–	0	15	mV
Input Offset Voltage	10kΩ from Pin 12 to Gnd	80	100	120	70	100	130	mV
CMRR	$0 \leq V_{CM} \leq 12V$, V_{IN} = 15V	60	70	–	60	70	–	dB
AVOL	Pin 12 open, V_{CM} = 0V	72	80	–	72	80	–	dB
Output Saturation	I_L = -10mA	–	0.2	0.5	–	0.2	0.5	V
Output Leakage	V_{IND} = 40V	–	.01	1.0	–	.01	1.0	μA
Small Signal Bandwidth	A_V = 0dB, T_J = 25°C	–	5	–	–	5	–	MHz
Propagation Delay	$V_{overdrive}$ = 100mV, T_J = 25°C	–	200	–	–	200	–	nS

TYPICAL CHARACTERISTICS

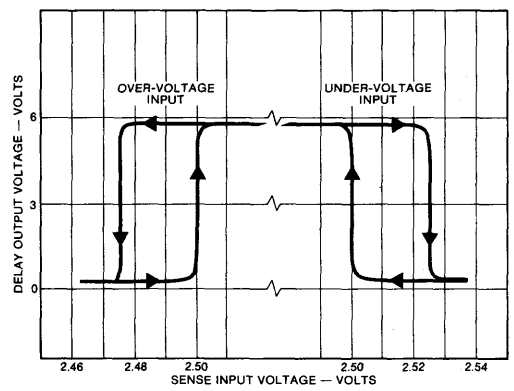
SCR TRIGGER POWER LIMITING



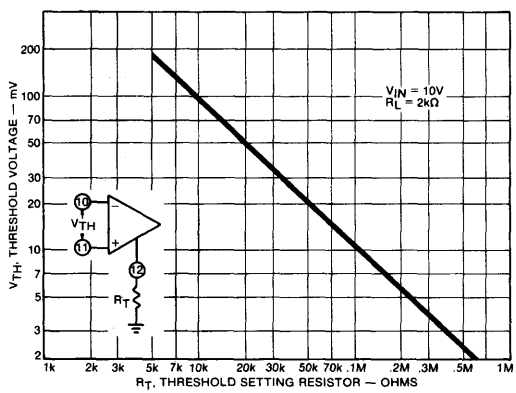
ACTIVATION DELAY VS. CAPACITOR VALUE



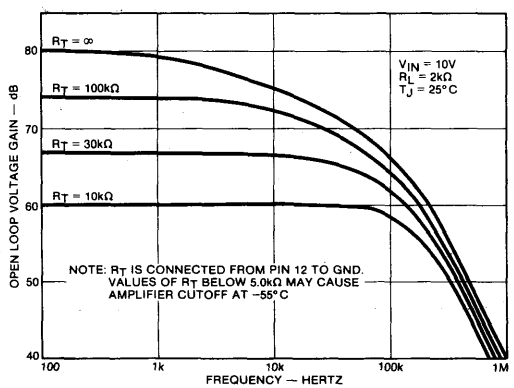
COMPARATOR INPUT HYSTERESIS



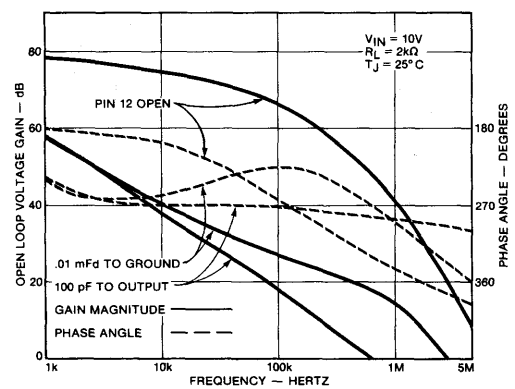
CURRENT LIMIT INPUT THRESHOLD



CURRENT LIMIT AMPLIFIER GAIN

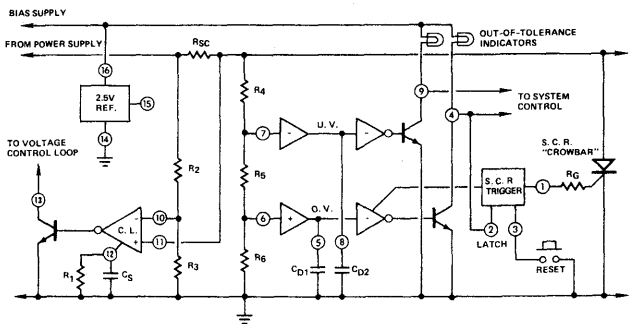


CURRENT LIMIT AMPLIFIER FREQUENCY RESPONSE



APPLICATIONS

TYPICAL APPLICATION



The values for the external components are determined as follows:

Current limit input threshold, $Vth \approx \frac{1000}{R1}$

Cs is determined by the current loop dynamics

Peak current to load, $Ip \cong \frac{Vth}{Rsc} + \frac{Vo}{Rsc}\left(\frac{R2}{R2 + R3}\right)$

Short circuit current, $Isc = \frac{Vth}{Rsc}$

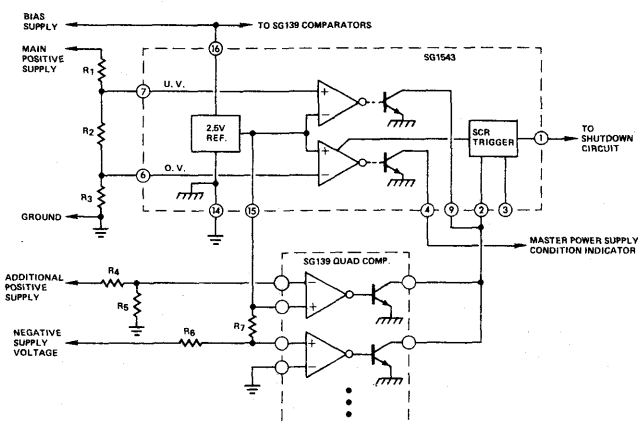
Low output voltage limit, $Vo\ (Low) = \frac{2.5\ (R4 + R5 + R6)}{R5 + R6}$

High output voltage limit, $Vo\ (High) = \frac{2.5\ (R4 + R5 + R6)}{R6}$

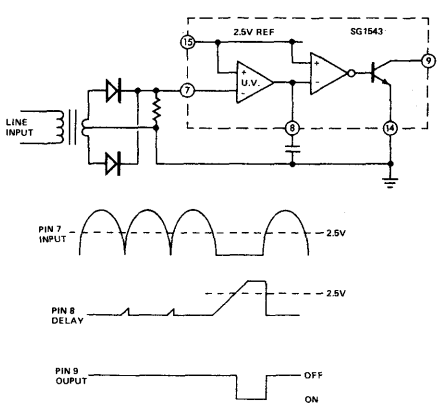
Voltage sensing delay, td = 10,000 Cd

SCR trigger power limiting resistor, $Rg > \frac{Vin - 5}{0.2}$

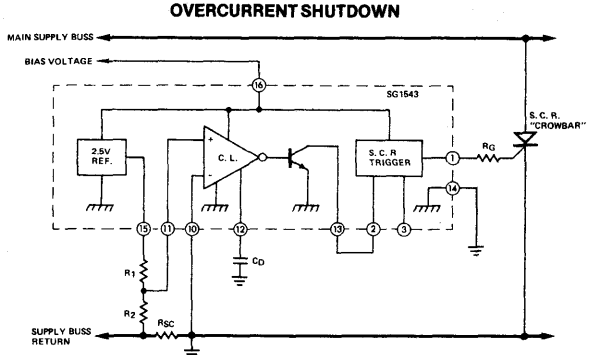
SENSING MULTIPLE SUPPLY VOLTAGES



INPUT LINE MONITOR



OVERCURRENT SHUTDOWN



Data subject to change without notice.

LOW-VOLTAGE SUPERVISORY CIRCUIT

DESCRIPTION

This device was designed to provide all the operational features of the SG1543/2543/3543 devices but with the added advantage of uncommitted inputs to the voltage sensing comparators. This allows monitoring of voltage levels less than 2.5 volts by dividing down the internal reference supply.

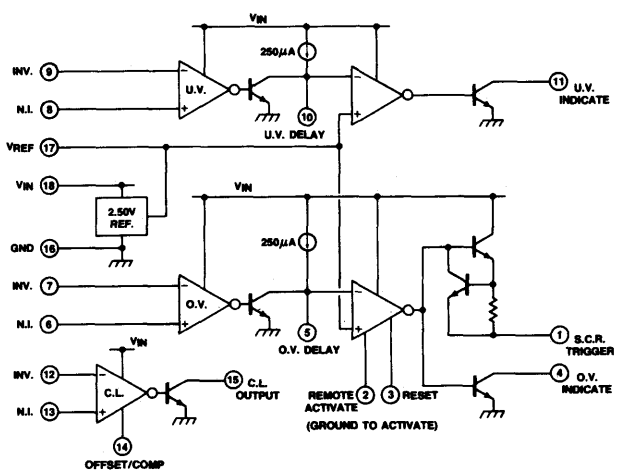
In all other respects, the SG1544 series is identical to the SG1543 series. These monolithic devices contain all the functions necessary to monitor and control the output of a sophisticated power supply system. Overvoltage sensing with provision to trigger an external SCR "crowbar" shutdown; an undervoltage circuit which can be used to monitor either the output or sample the input line voltage; and a third op amp/comparator usable for current sensing are all included in this IC, together with an independent, accurate reference generator.

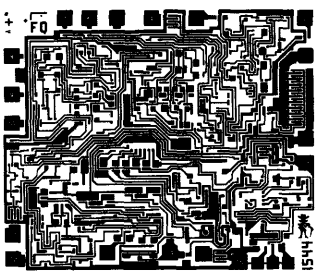
The voltage-sensing input comparators are identical and can be used with threshold levels from zero volts to (V_{IN} −3V). Each has approximately 25 mv of hystersis which is offset so the switching differential threshold is zero on the non-inverting input for rising levels and zero on the inverting input for falling signals. All other operating characteristics are as described in the SG1543 data sheet and application note.

FEATURES

- **Uncommitted comparator inputs for wide input flexibility**
- **Common-Mode range from zero to near supply voltage**
- **Reference voltage trimmed to 1% accuracy**
- **All other features of SG1543 series**

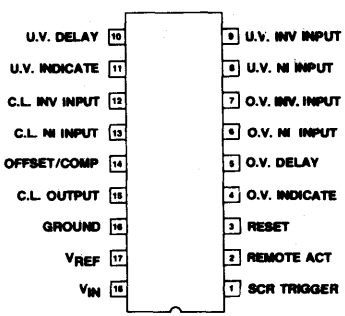
BLOCK DIAGRAM





CONNECTION DIAGRAM

TOP VIEW



J-PACKAGE 18-PIN TO-116 CERDIP

ELECTRICAL CHARACTERISTICS

Unless otherwise stated, these specifications apply for T_J = −55°C to +125°C for the SG1544, −25°C to +85°C for the SG2544 and 0°C to + 70°C for the SG3544; and for V_{IN} = 5 to 35 Volts. Electrical tests are performed with V_{IN} = 10 Volts and 2kΩ pull-up resistors on all indicator outputs. All electrical ratings and specifications are tested with the inverting over-voltage input and the non-inverting under-voltage input externally connected to the 2.5 volt reference.

PARAMETER	CONDITIONS	SG1544/2544 MIN	SG1544/2544 TYP	SG1544/2544 MAX	SG3544 MIN	SG3544 TYP	SG3544 MAX	UNITS
Input Voltage Range	T_J = 25°C to T_{max}	4.5	–	40	4.5	–	40	V
Input Voltage Range	T_{min} to T_{max}	4.7	–	40	4.7	–	40	V
Supply Current	V_{IN} = 40V, Outputs open	–	7	10	–	7	10	mA
REFERENCE SECTION (Pins 17, 18)								
Output Voltage	T_J = 25°C	2.48	2.50	2.52	2.45	2.50	2.55	V
Output Voltage	Over Temp. Range	2.45	–	2.55	2.40	–	2.60	V
Line Regulation	V_{IN} = 5 to 30V	–	1	5	–	1	5	mV
Load Regulation	I_{REF} = 0 to 10 mA	–	1	10	–	1	10	mV
Short Circuit Current	V_{REF} = 0	12	25	40	12	25	40	mA
Temperature Stability		–	50	–	–	50	–	ppm/°C
SCR TRIGGER SECTION (Pins 1, 2, 3)								
Peak Output Current	V_{IN} = 5V, R_G = 0, V_O = 0	100	200	400	100	200	400	mA
Peak Output Voltage	V_{IN} = 15V, I_O = 100mA	12	13	–	12	13	–	V
Output Off Voltage	V_{IN} = 40V	–	0	0.1	–	0	0.1	V
Remote Activate Current	Pin 2 = Gnd	–	.4	.8	–	.4	.8	mA
Remote Activate Voltage	Pin 2 open	–	2	6	–	2	6	V
Reset Current	Pin 3 = Gnd, Pin 2 = Gnd	–	.4	.8	–	.4	.8	mA
Reset Voltage	Pin 3 open, Pin 2 = Gnd	–	2	6	–	2	6	V
Output Current Rise Time	R_L = 50Ω	–	400	–	–	400	–	mA/μS
Prop. Delay from Pin 2	T_J = 25°C, $V_{(Pin\ 2)}$ = 0.4V	–	300	–	–	300	–	nS
Prop. Delay from Pin 6	C_D = 0, $V_{(Pin\ 6)}$ = 2.7V	–	500	–	–	500	–	nS
COMPARATOR SECTIONS (Pins 6, 7, 5, 4; 8, 9, 10, 11)								
Input Threshold (Input voltage rising on Pin 6 and falling on Pin 9)	T_J = 25°C	2.45	2.50	2.55	2.40	2.50	2.60	V
	Over Temp. Range	2.40	–	2.60	2.35	–	2.65	V
Input Hysteresis		–	25	–	–	25	–	mV
Input Bias Current	Sense input = 0V	–	0.3	1.0	–	0.3	1.0	μA
Delay Saturation		–	0.2	0.5	–	0.2	0.5	V
Delay High Level		–	6	8	–	6	8	V
Delay Charging Current	V_D = 0V	200	250	300	200	250	300	μA
Indicate Saturation	I_L = −10mA	–	0.2	0.5	–	0.2	0.5	V
Indicate Leakage	V_{IND} = 40V	–	.01	1.0	–	.01	1.0	μA
Propagation Delay	$V_{(Pin\ 6)}$ = 2.7V, $V_{(Pin\ 9)}$ = 2.3V, T_J = 25°C, C_D = 0	–	400	–	–	400	–	nS
	C_D = 1μf	–	10	–	–	10	–	mS
CURRENT LIMIT SECTION (Pins 12, 13, 14, 15)								
Input Voltage Range		0	–	(V_{IN}−3V)	0	–	(V_{IN}−3V)	V
Input Bias Current	Pin 14 open, V_{CM} = 0V	–	0.3	1.0	–	0.3	1.0	μA
Input Offset Voltage	Pin 14 open, V_{CM} = 0V	–	0	10	–	0	10	mV
Input Offset Voltage	10Ω from Pin 14 to Gnd	80	100	120	80	100	120	mV
CMRR	0< V_{CM} <12V, V_{IN} = 15V	60	70	–	60	70	–	dB
AVOL	Pin 14 open, V_{CM} = 0V	72	80	–	72	80	–	dB
Output Saturation	I_L = −10mA	–	0.2	0.5	–	0.2	0.5	V
Output Leakage	V_{IND} = 40V	–	.01	1.0	–	.01	1.0	μA
Small Signal Bandwidth	A_V = 0dB, T_J = 25°C	–	5	–	–	5	–	MHz
Propagation Delay	$V_{overdrive}$ = 100mV, T_J = 25°C	–	200	–	–	200	–	nS

See Applications Notes for additional information.

ADVANCED DATA

SG1548/SG2548/SG3548

Performance data described herein represent design goals. Final device specifications are subject to change.

QUAD POWER FAULT MONITOR

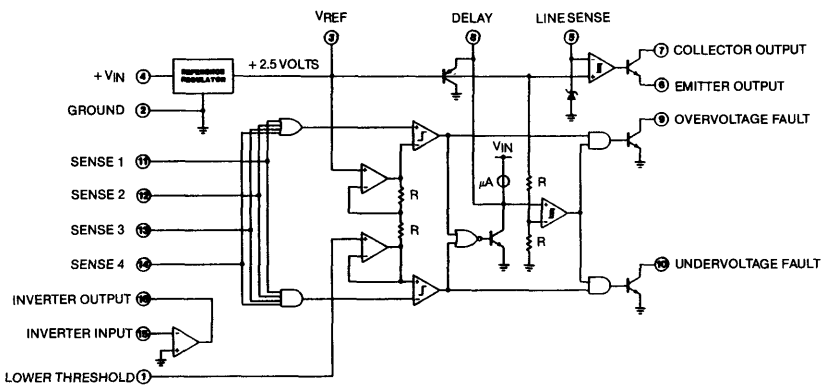
DESCRIPTION

The SG1548 is an integrated circuit capable of monitoring up to four positive DC supply voltages simultaneously for overvoltage fault conditions. An on-chip inverting op amp also allows monitoring one negative DC voltage. The fault tolerance window is accurately programmable from ±2% to ±40% using a simple divider network on the ±2.5 volt reference. A single external capacitor sets the fault indication delay, eliminating false outputs due to switching noise, logic transition current spikes, and short-term AC line interruptions. An additional comparator referenced to ±2.5 volts allows the AC line to be monitored for undervoltage conditions or for generation of a line clock. The comparator can also be used for programmable undervoltage lockout in a switching power supply. Uncomitted collector and emitter outputs permit both inverting and non-inverting operation. External availability of the precision ±2.5 volt reference and open-collector logic outputs permit expansion to monitor additional voltages using available open-collector quad comparators.

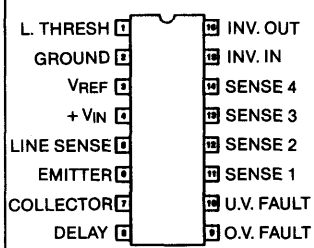
FEATURES

- Monitors four DC voltages and the AC line
- Precision ±2.5 volt ±1% low-drift reference
- Fault tolerance adjustable from ±2% to ±40%
- Separate overvoltage, undervoltage and AC line outputs
- Fault delay programmable with a single capacitor
- Comparator hysteresis to prevent oscillations
- On-chip inverting op amp for negative voltage
- Open-collector output logic for expandability
- Operation from +4.5 to +40 volt supplies
- Standard 16 pin dual-in-line package

BLOCK DIAGRAM



CONNECTION DIAGRAM (TOP VIEW)



J or N PACKAGE
TO-116 STYLE

ORDERING INFORMATION

Part Number	Temperature Range	Package
SG1548J	−55°C to +125°C	16 Pin Ceramic DIP
SG2548J	−25°C to +85°C	16 Pin Ceramic DIP
SG3548J	0°C to +70°C	16 Pin Ceramic DIP
SG3548N	0°C to +70°C	16 Pin Plastic DIP

SG1549 / SG2549 / SG3549

CURRENT SENSE LATCH

DESCRIPTION

This monolithic integrated circuit is an analog latch device with digital reset. It was specifically designed to provide pulse-by-pulse current limiting for switch-mode power supply systems, but many other applications are also feasible. Its function is to provide a latching switch action upon sensing an input threshold voltage, with reset accomplished by an external clock signal. This device can be interfaced directly with many kinds of pulse width modulating control IC's, including the SG1524, SG1525A and SG1527A.

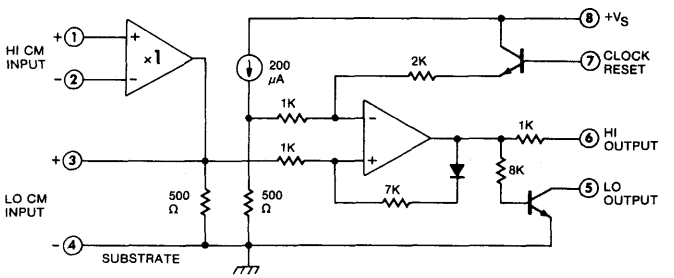
The input threshold for the latch circuit is 100mV, which can be referenced either to ground or to a wide-ranging positive voltage. There are high- and low-going output signals available, and both the supply voltage and clock signal can be taken directly from an associated PWM control chip.

With delays in the range of 200 nanoseconds, this latch circuit is ideal for fast-reaction sensing to provide overall current limiting, short circuit protection, or transformer saturation control.

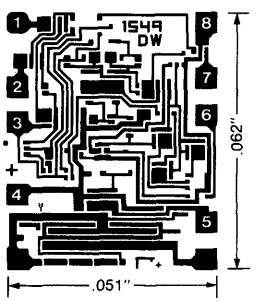
FEATURES

- **Current sensing with 100mV threshold**
- **Common-mode input at ground or to 40V**
- **Complementary outputs**
- **Automatic reset from PWM clock**
- **180nS delay**
- **Interface direct to SG1524, SG1525A, SG1527A**

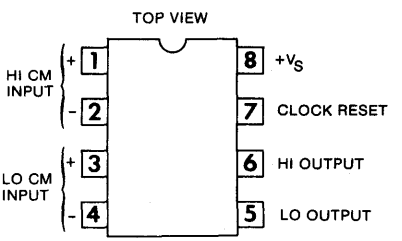
BLOCK DIAGRAM



CHIP LAYOUT



CONNECTION DIAGRAM



Y OR M PACKAGES (MINIDIP)

ABSOLUTE MAXIMUM RATINGS

Input Supply Voltage, V_S	25V
HI CM Input Voltage	40V
LO Output "off" voltage	40V
LO Output "on" current	25mA
Power Dissipation	600mW
Derate above 25°C	5.0 mW/°C

Operating Temperature Range	
SG1549 Y	−55°C to +125°C
SG2549 Y or M	−25°C to +85°C
SG3549 Y or M	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

ELECTRICAL CHARACTERISTICS

(Unless otherwise stated, these specifications apply over the operating temperature range, with V_S = +5.0 volts, and with the circuit unlatched, or reset.)

PARAMETER	TEST CONDITIONS	SG1549/2549			SG3549			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
CM Input	(Note 1)							
Threshold Voltage	Pin 1 & 2 shorted	90	100	110	80	100	120	mV
Input Impedance	V(Pin 3) = 50mV	400	500	600	400	500	600	Ω
HI CM Input	(Note 1)							
Threshold Voltage	V_{CM} = 2V, Pin 3 open	90	100	110	80	100	120	mV
Threshold Voltage	V_{CM} = 40V, Pin 3 open	90	100	110	80	100	120	mV
Input Current	V(Pin 1) = V(Pin 2) = 40V	—	200	300	—	200	300	μA
Clock Reset								
Min. Trigger Voltage		—	2.0	2.5	—	2.0	2.5	V
Input Current	V(Pin 7) = 4V	—	20	40	—	20	40	μA
HI Output								
Off Voltage		—	0	0.1	—	0	0.1	V
On Voltage	I_L = 1mA	2.8	3.2	—	2.8	3.2	—	V
LO Output								
Off Leakage	V(Pin 5) = 40V	—	.01	1.0	—	.01	1.0	μA
On Voltage	I_L = -10mA	—	.3	0.5	—	.3	0.5	V
Supply Current	V(Pin 8) = 5V	—	2	3	—	2	5	mA
	V(Pin 8) = 20V	—	10	15	—	10	15	mA

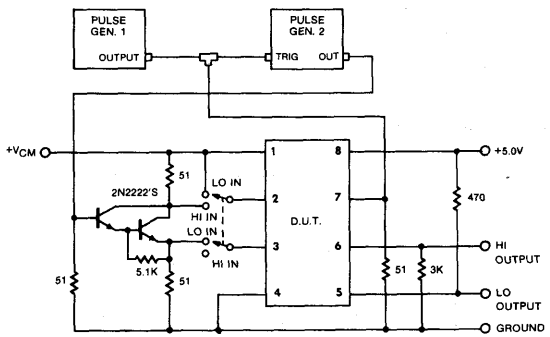
Note 1: Input threshold voltages and supply current are directly proportional to supply voltage, V_S.

TYPICAL SWITCHING CHARACTERISTICS

VS = 5V, TA = 25°C

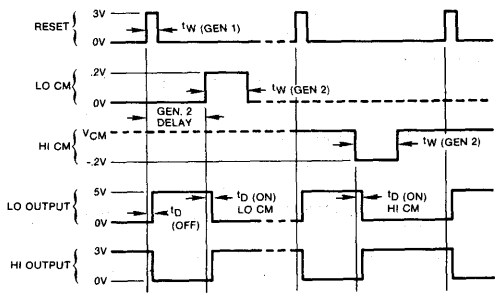
PARAMETER	SYMBOL	CONDITIONS	TYPICAL	UNITS
Reset Minimum Pulse Width	t_{w1}	Amplitude = 3.0V	150	nSec
Delay from Reset to LO Output	t_D (off)	R_L = 470Ω to V_S	300	nSec
LO Input Minimum Pulse Width	t_{w2}	Amplitude = 200mV	50	nSec
Delay from LO Input to LO Output	t_D (on) LO CM	Amplitude = 200mV R_L = 470Ω to V_S	180	nSec
Delay from HI Input to LO Output	t_D (on) HI CM	Amplitude = 200mV V_{CM} = 5V	300	nSec
Delay from HI Output to LO Output		LO CM Input = 200mV	30	nSec

DYNAMIC TEST CIRCUIT



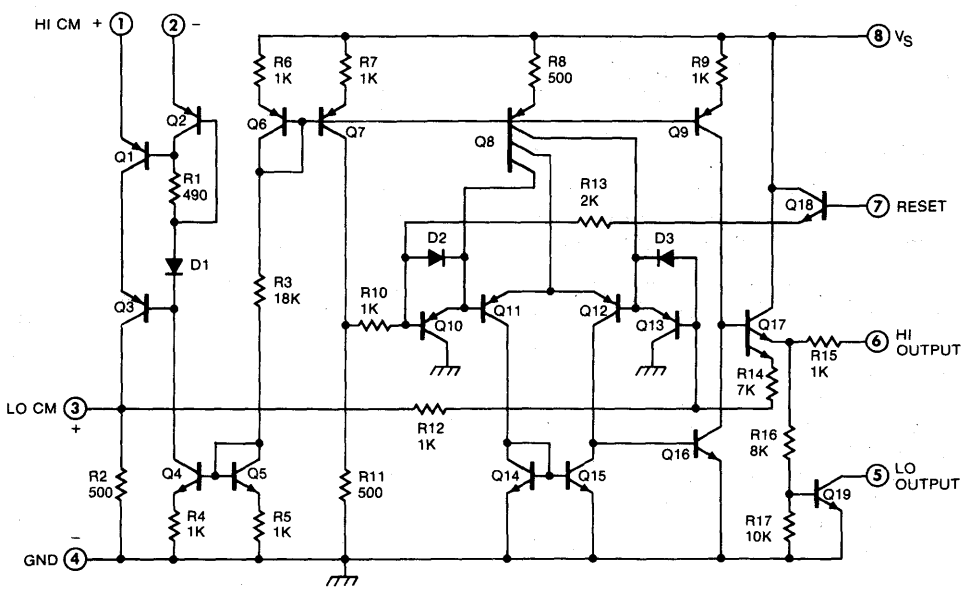
Note: Pulse Gen. 2 must have triggering, delay and amplitude controls.

SWITCHING WAVEFORMS



Note: HI OUTPUT Precedes LO OUTPUT by approximately 30 nSec.

SCHEMATIC



APPLICATIONS

HIGH LINE SENSING — The SG1549 will provide current sensing in the positive supply line in the typical SG1524 single-ended switching regulator application shown in Figure 1. The HI CM sense circuitry can be used with input voltages between 2 and 40 volts.

A value for R_{SC} is determined by dividing the 100mV input threshold by the peak current desired. High-frequency noise, or switching transients, can usually be eliminated by a small capacitor between pins 3 and 4.

Current control may be accomplished by either the HI OUTPUT pin connected to the SG1524's Shutdown pin, or the LO OUTPUT pin connected directly to the Compensation Terminal. In either case, activation of the current sense latch will tend to discharge the compensation capacitor, C_C, which may cause slow recovery from pulse limiting. If this feature is desired, the LO OUTPUT pin may be used to discharge a soft-start network instead of coupling directly to the SG1524. If it is not desired, the use of a small value of C_C, and perhaps a diode across R_C, will enhance recovery.

Another method of introducing the current shutdown signal is shown in Figure 2 where the SG1524 is used to activate a constant drive current to the high-current switch, in this case an SM600. The 2N2222 forms a constant current generator when driven from the SG1524's 5.0 volt reference through a 1K resistor. This transistor is then switched off by the LO OUTPUT transistor in the SG1549, achieving the fastest response to the output of the regulator.

LOW LINE SENSING — In many types of feed-forward or push-pull converters, current protection may be provided by sensing in an emitter resistor referenced to ground on the primary side of an output transformer. The fast-reacting SG1549 can easily sense secondary overload as reflected back to the primary and, additionally, provide protection from unbalanced transformer saturation.

When using the LO CM inputs, the HI CM inputs should be shorted together. While the LO CM inputs may be connected directly across a sense resistor, R_{SC}, a small low-pass filter as shown in Figure 3 is often required to eliminate high frequency transients. It must be remembered that the 500 ohm input impedance at the LO CM terminals will cause the use of R1 to increase the effective threshold; however, this also offers the possibility of an easily adjustable threshold by incorporating a potentiometer at the input.

Coupling the output signal from the SG1549 to the control chip may be done in several ways including the use of either the Compensation or Shutdown pins on the SG1524 as described earlier.

Another convenient way to tie the output of the SG1549 into the PWM control in higher power applications is by using the SG1627 Dual Interface Driver and connecting the LO OUTPUT terminal of the SG1549 directly to the two Non-Inverting inputs of the SG1627 as shown in Figure 4.

And finally, keep in mind that the LO OUTPUT terminal of the SG1549 will easily drive most high-speed optical couplers should some type of isolation between current sense and shutdown control be required.

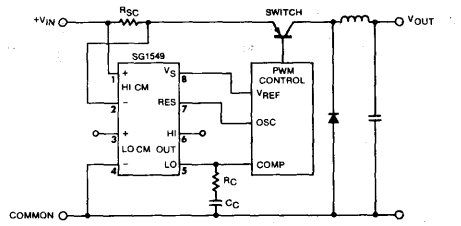


Figure 1 — High Line sensing with the SG1549 in conjunction with an SG1524 PWM control IC.

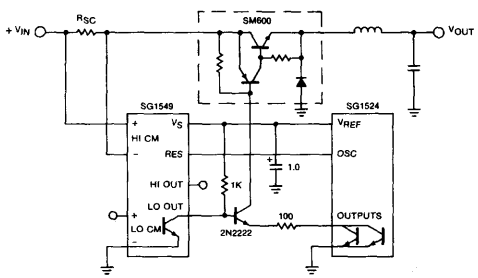


Figure 2 — Current control for a buck regulator with constant drive current.

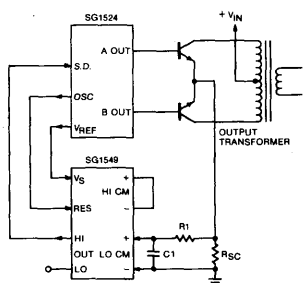


Figure 3 — A push-pull converter with low-line emitter current sensing.

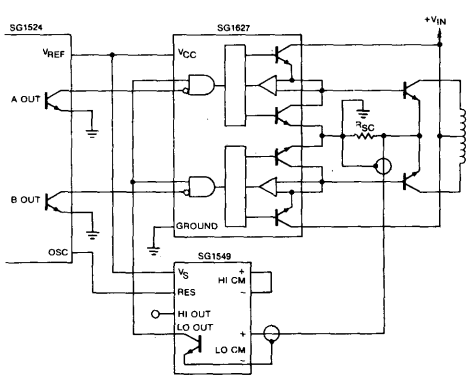


Figure 4 — Power Boost and current control with the SG1627.

ADVANCED DATA
SG3509

Performance data described herein represent design goals.
Final device specifications are subject to change.

AIR FAULT DETECTOR

DESCRIPTION

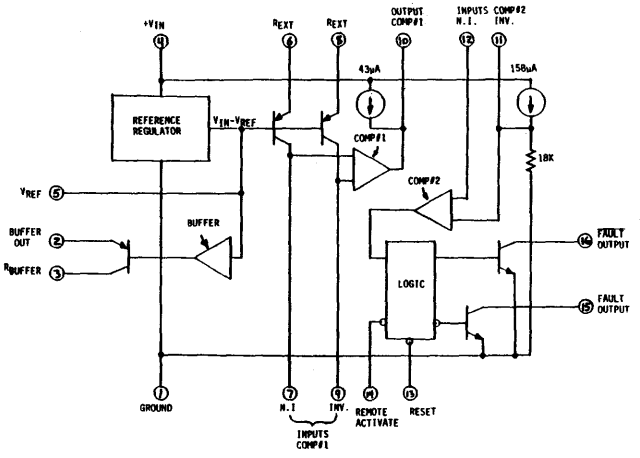
This monolithic integrated circuit provides the control functions necessary to protect equipment with forced air cooled system from loss of air flow. It is designed to provide a positive indication of the presence of air flow independent of air temperature. Outputs FAULT and $\overline{\text{FAULT}}$ are used to activate an alarm or shut-down equipment when air flow drops below a preset level for a programmed time period.

This device contains a regulated, stable 2.2 volt reference with $-2mV/°C$ temperature coefficient which provides a bias for the heater current source and the matching programmable current sources. Availability of both polarity inputs to the comparator #1 allows a wide flexibility of use. An external capacitor can be used to program an accurate time delay between occurence and fault indication.

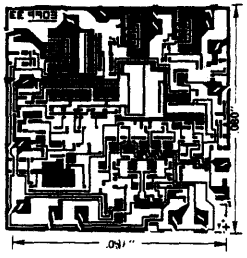
FEATURES

- **Operation from 4.5 to 40 volts**
- **2.2 volt reference with respect to V_{IN}**
- **Matching programmable current sources**
- **Programmable heater current source up to 100mA**
- **Zero to 35 volts sensing capability**
- **Programmable time delay**
- **Remote activation capability**
- **Latching/Non-latching capability**
- **Fault and $\overline{\text{Fault}}$ output available**
- **Open-collector outputs with 50mA sink capability**

BLOCK DIAGRAM

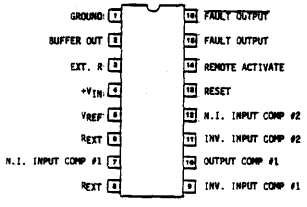


CHIP LAYOUT



CONNECTION DIAGRAM

TOP VIEW



TO-116 STYLE

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage (+ V_{IN})	+ 40V
Sink Load Current (continuous)	50mA
Power Dissipation at T_A = + 25°C (Note 2)	600mW
Operating Junction Temperature	− 125°C
Storage Temperature Range	− 55°C to 150°C
Lead Temperature (Soldering, 10 seconds)	+ 300°C

Note 1. Values beyond which damage may occur.
Note 2. Derate at 6.67mW/°C for ambient temperatures above + 35°C.

RECOMMENDED OPERATING CONDITIONS (Note 3)

Input Voltage (+ V_{IN})	+ 4.5 to + 40V
Common-Mode Voltage Range Comp #1(V_{CM})	0 to V_{IN} − 1.5V
Collector Voltage FAULT/$\overline{\text{FAULT}}$ Outputs	0 to + 40V
Sink Load Current FAULT/$\overline{\text{FAULT}}$ Outputs	0 to 50mA
Programmable Current Sources Resistors (R_{EXT})	150KΩ to 7.5KΩ
Reference Sink Current	
with V_{IN} = 4.5V to 6V	0 to 1mA
with V_{IN} > 6V	0 to 10mA
Buffer Out Sink Current	0 to 100mA

Note 3. Range over which the device is functional and parameter limits are guaranteed.

3

ELECTRICAL CHARACTERISTICS

Unless Otherwise stated, these specifications apply for T_A = 25°C

PARAMETER			REQUIREMENTS		
NAME	**SYMBOL**	**TEST CONDITION (3)**	**MIN**	**MAX**	**UNIT**
Reference Section Output Voltage (Note 6)	$V_{REF}1$	V_{IN} = 4.5V	2.09	2.31	V
Line Regulation	LINE REG	V_{IN} = 4.5V to 40V, I_L = 0		10	mV
Load Regulation	LOAD REG	I_{REF} = 0 to 1mA, V_{IN} = 4.5V		10	mV
Short-Circuit Current	I_{OS}	V_{IN} = 12V	5	25	mA
Comparator 1, Input Offset Voltage	V_{OS}	T_A = 25° to 70°C		± 10	mV
Input Bias Current	I_B			− 1	μA
Output Offset Current	I_{IO}	$I_{IN}(+) - I_{IN}(-)$		± 100	nA
Input Common-Mode Voltage Range	V_{CM}		0	V_{IN} − 2	V
Voltage Gain	V_G	$R_L \geq$ 15K Ohms	4		V/mV
Output Source Current	(SOURCE) I_O	$V_{PIN}10$ = 0	34	52	μA
Comparator 2, + Input Bias Current	I_B+	$V_{PIN}12$ = V_{REF}		2	μA
− Input Reference Voltage	$V_{REF}2$	I_L = 0	2.0	3.80	V
Input Resistance to Ground	R_{IN}		12.6	23.4	Kohms
Remote Activate Current	I_{RA}	+ V_{IN} = + 12V, Pin 14 = 0V		0.9	mA
Remote Activate Voltage	V_{RA}	+ V_{IN} = 12V, Pin 14 open	2	7	V
Reset Activate Current	I_{ReA}	+ V_{IN} = + 12V, p 14 = 0V, V_{pin} 13 = 0V		0.9	mA
Reset Activate Voltage	V_{ReA}	Pin 13 open, Pin 14 Gnd		1.5	V
Fault Low Output	V_{SAT}	I_{SINK} = 50mA		2.0	V
Fault Low Output	V_{SAT}	I_{SINK} = 16mA		0.5	V
Programmable Current Sources Output Current (Notes 4 & 5)	I_{OUT}	R_{EXT} = 20K = .1%	10	200	μA
Current Match	I_{MATCH}	R_{EXT} = 20K ± .1%		± 1	%
Buffer Output, Pin 2 Voltage	$V_{PIN\ 2}$	Input Current = 100mA 1.9		2.3	V

Notes: (3) T_A = 25°C unless otherwise specified.
(4) Pin 6, 20K to V_{IN} measure Ic pin to 7 Gnd.
(5) Pin 8 same 20K to V_{IN} measure Ic pin 9 to Gnd.
(6) V_{REF} 1 is designed for a − 2mV°C ± 1mV output voltage temperature coefficient.

SG3523 / 3523A / 3423 / 3423A

Over-Voltage Sensing Circuit

DESCRIPTION

This monolithic integrated circuit provides the control functions necessary to protect sensitive electronic circuitry from over-voltage transients or the effects of voltage regulator failure. It is designed for use with an external SCR "crowbar" for immediate shutdown of the power supply, but additionally provides logic level outputs for regulator turn-off and/or operator or system out-of-tolerance indication.

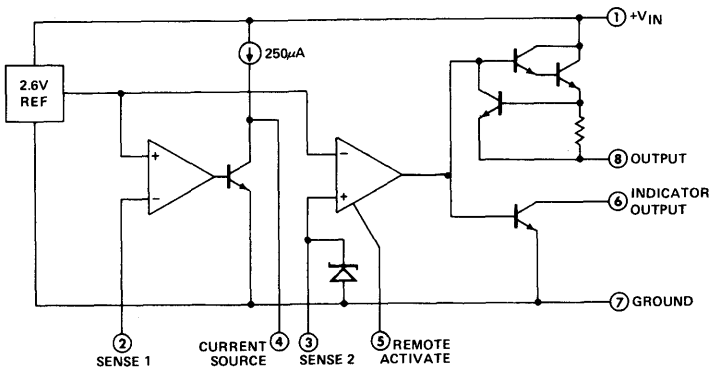
This device contains an accurate, stable 2.6 volt reference which allows the sensing threshold to be set predictably without the need for potentiometers. An external capacitor can be used to program an accurate time delay between fault occurence and crowbar triggering, but this delay may be bypassed by inputing at the Sense 2 terminal or by using the remote activation capability.

For additional circuit functions, see SG1542 and SG1543 data sheets.

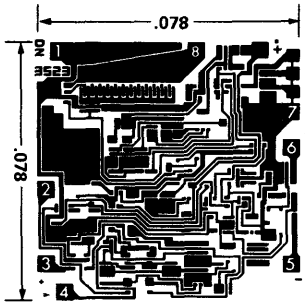
FEATURES

- **Operation from 4.5 to 40 volts**
- **Highly accurate sensing threshold**
- **Built-in input hysteresis**
- **Programmable time delay**
- **SCR "Crowbar" drive of 200mA**
- **Remote activation capability**

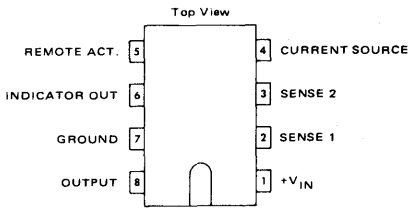
BLOCK DIAGRAM



CHIP LAYOUT



CONNECTION DIAGRAM



Y, M-PACKAGES (MINIDIP)

ABSOLUTE MAXIMUM RATINGS

Input Supply Voltage, V_{IN}	40V
Sense Voltage (1)	V_{IN}
Sense Voltage (2)	6.5V
Remote Activation Input Voltage	7.0V
SCR Trigger Current	500mA
Indicator Output Voltage	40V
Indicator Output Sink Current	50mA

Power Dissipation (Package Limitation)	
Ceramic minidip (Y-pkg.)	800mW
Derate above 25°C	8.0mW/°C
Plastic minidip (M-pkg.)	400mW
Derate above 25°C	4.0 mW/°C
Operating Temperature Range	
SG3523/3523A	−55°C to +125°C
SG3423/3423A	0°C to +70°C

3

ELECTRICAL CHARACTERISTICS

(Unless otherwise specified, these specifications apply for V_{IN} = 5 to 35V and T_J = −55°C to +125°C for the SG3523/3523A and 0°C to +70°C for the SG3423/3423A.)

PARAMETER	CONDITIONS	SG3523A			SG3423A			SG3423/SG3523			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Supply Voltage Range		4.5	–	40	4.5	–	40	4.5	–	40	V
Supply Current		–	5	7	–	5	7	–	5	10	mA
Sense Threshold	T_J = 25°C	2.55	2.60	2.65	2.50	2.60	2.70	2.45	2.60	2.75	V
Sense Threshold	Over Temp. Range	2.50	–	2.70	2.45	–	2.75	2.35	–	2.85	V
Input Hysteresis	Sense 1 only	–	25	–	–	25	–	–	25	–	mV
Input Bias Current	Sense 1	–	-0.3	-1.0	–	-0.3	-1.0	–	–	–	μA
	Sense 2	–	+5	+10	–	+5	+10	–	–	–	μA
Current Source		200	250	300	200	250	300	100	250	300	μA
Remote Activation Input Current	$V_{Pin\ 5}$ = 2.0	–	5	40	–	5	40	–	5	40	μA
	$V_{Pin\ 5}$ = 0.8V	–	-120	-180	–	-120	-180	–	-120	-180	μA
Output Voltage	I_O = 100mA	V_{IN} −2.2	V_{IN} −1.8	–	V_{IN} −2.2	V_{IN} −1.8	–	V_{IN} −2.2	V_{IN} −1.8	–	V
Peak Output Current	V_{IN} = 5V, V_O = 0V	100	200	400	100	200	400	–	–	–	mA
Output Off Voltage	V_{IN} = 40V	–	0	0.1	–	0	0.1	–	–	–	V
Indicator Saturation Voltage	I_L = -1.6mA	–	0.1	–	–	0.1	–	–	0.1	0.4	V
	I_L = -10mA	–	0.2	0.5	–	0.2	0.5	–	0.4	–	V
Indicator Leakage	$V_{Pin\ 6}$ = 40V	–	.01	1.0	–	.01	1.0	–	–	–	μA
Propagation Delay to Output	T_J = 25°C, Sense 1	–	1.0	–	–	1.0	–	–	1.0	–	μS
	T_J = 25°C, Sense 2	–	0.5	–	–	0.5	–	–	0.5	–	μS
Output Current Rise Time	T_J = 25°C	–	400	–	–	400	–	–	400	–	mA/μS

ADVANCED DATA
SG3551

Performance data described herein represent design goals.
Final device specifications are subject to change.

TRIPLE CURRENT SENSE LATCH

DESCRIPTION

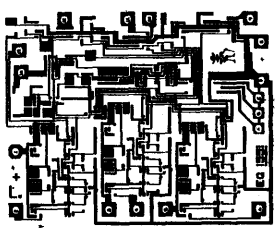
This monolithic integrated circuit is a triple current sense comparator with latch and digital reset. It was specifically designed for printer coil saturation control. Each comparator input has a fixed 360 mV threshold to allow direct current sensing across a sampling resistor. When coil current exceeds a preset level, the comparator changes state and latches the drive control off. A reset command unlatches the driver and initiates another current ramp to the solenoid.

An on-chip bandgap regulator allows this device to maintain threshold accuracy over a supply voltage range of +4.5 to +25 volts. The common-mode range of the differential current sense inputs is not limited by the latch supply voltage, and may be as high as +40 volts. The SG3551 is available in a 14 pin plastic dual-in-line package, and is rated for operation over an ambient temperature range of 0 to +85°C.

FEATURES

- **Three Current Sense Latches**
- **±5% Accuracy on Current Sense Threshold**
- **+4.5 to +25 Volt Supply Voltage Range**
- **Common Mode Range up to 40 Volts**
- **On-chip Bandgap Reference**
- **40 Volt, 25 mA Open-Collector Outputs**

CHIP LAYOUT

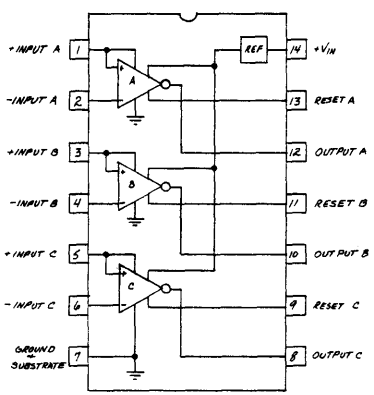


DIE SIZE : 73 X 93 MILS

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Input Supply	25	V
IN +	40	V
IN -	40	V
Output Off Voltage	40	V
Output On Current	25	mA
Reset Input Voltage	7	V
Power Dissipation	600	mW
Temperature Range Operating	0 to +85	°C
Storage	-65 to +150	°C

CONNECTION DIAGRAM



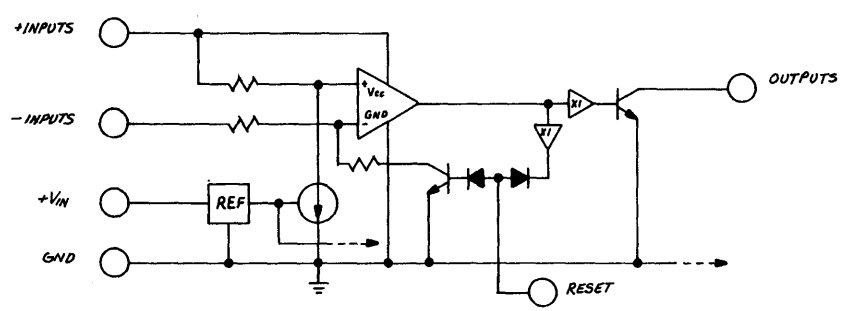
TOP VIEW

ELECTRICAL CHARACTERISTICS

(Unless Otherwise stated, these specifications apply over the operating temperature range of 0-85°C with V_S = 5V ± 10%)

PARAMETER (+, – INPUTS)	CONDITIONS	MIN	MAX	UNITS
Threshold Voltage	V_{CM} = 3.5 to 40V V_S = 4.5 to 25V	340	380	mV
Positive Input Current	$+V_{IN} = -V_{IN}$ = 40V Reset = 0.4V		1.5	mA
Negative Input Current	$+V_{MC} = +40V\Delta V_{IN}$ = 360mV Reset = 2.4V		1.5	µA
RESET				
High-Level $\overline{\text{Reset}}$ Voltage		2		V
Low-Level $\overline{\text{Reset}}$ Voltage			0.8	V
High-Level Input Current	V_S = 25V, Reset = 2.4V		20	µA
Low-Level Input Current	V_S = 25V, Reset = 0.4V		–400	µA
Reset Minimum Pulse Width	Amplitude = 3.0V		500	nS
OUTPUT VOLTAGE				
Off-State Leakage	V_O = 40V		1.0	µA
On-State Voltage (latched)	I_O = 10mA, $+V_{IN} = -V_{IN}$ Reset= 2.4V		0.5	V
Supply Current (unlatched)	V_S = 25V, Reset = 0.4V		10	mA
PROPAGATION DELAYS				
From Reset to Output	R_L = 470Ω to V_S (See figure 1)		1.5	µS
From Input to Output	R_L = 470Ω to V_S (See figure 2)		1.5	µ

BLOCK DIAGRAM



4

OPERATIONAL AMPLIFIERS

General Purpose, Compensated Op Amps

General Purpose, Uncompensated Op Amps

Quad Op Amps

High Voltage Op Amps

High Power Op Amp

Micropower Op Amp

SG101/201 SG101A/201A/301A

Uncompensated Operational Amplifiers

The SG101/201 are general purpose operational amplifiers. Features include excellent input bias/current and drift characteristics plus short circuit protection and pin compatibility with many industry-standard operational amplifiers.

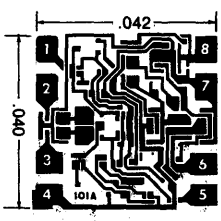
The SG101A/201A/301A offer improved performance over the SG101/201 operational amplifiers and also provide short circuit protection and pin compatibility with industry standard types.

- **Frequency compensated with a single capacitor — no resistor required**
- **Low current drain: 1.8mA at ±20V**
- **Continuous short circuit protection**
- **Operation as a comparator with differential inputs as high as ±30V**
- **No latch up when common mode range is exceeded**
- **3mV offset voltage over temperature**
- **100nA input current over temperature**
- **20nA offset current over temperature**
- **Guaranteed drift characteristics**
- **Offsets guaranteed over full common mode range**

PARAMETERS*	101	201	101A	201A	301A	UNITS
Supply Voltage	±5 to ±20	±5 to ±20	±5 to ±20		±5 to ±15	V
Operating Temperature Range	−55 to +125	0 to +70	−55 to +125	−25 to +85	0 to +70	°C
Package Types	T, Y, J, F	T,Y,J,F,N,M	T, Y, J, F	T, Y, J, F, N, M		—
Input Offset Voltage	5.0	7.5	2.0 (3.0)		7.5 (10)	mV
Input Offset Current	200 (500)	500 (750)	10 (20)		50 (70)	nA
Input Bias Current	0.5 (1.5)	1.5 (2.0)	0.075 (0.1)		0.25 (0.30)	μA
Temp Coeff Input Offset Voltage	(3.0 typ)	(6.0 typ)	15		30	μV/°C
Temp Coeff INput Offset Current	—	—	0.2		0.6	nA/°C
Large Signal Voltage Gain[1]	50 (25)	20 (15)	50 (25)		25 (15)	V/mV
Common Mode Rejection	(70)	(65)	(80)		(80)	dB
Power Supply Rejection	(316)	(316)	(100)		(100)	μV/V
Input Common Mode Voltage Range[2]	(±12)	(±12)	(+15, −12)		(+15, −12)	V
Differential Input Voltage	±30	±30	±30		±30	V
Slew Rate $A_V = 1$,	0.2	0.2	0.2		0.2	V/μS
$A_V = 10$	3 (typ)	3 (typ)	3 (typ)		3 (typ)	
Unity Gain Bandwidth	0.5 (typ)	0.5 (typ)	0.5 (typ)		0.5 (typ)	MHz
Supply Current	3.0	3.0	3.0		3.0	mA
V_{out} $R_L = 2k\Omega$	±10	±10	±10		±10	V
$R_L = 10k\Omega$	±12	±12	±12		±12	V
Noise						
$R_S = 1k\Omega$ f = 10Hz to 10kHz	4	4	4		4	μV(rms)
$R_S = 500k\Omega$ f = 10Hz to 10kHz	25	25	25		25	(typ)

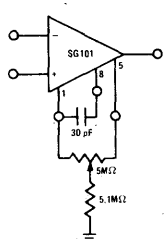
*Parameters apply over supply voltage range and are min./max. limits either at $T_A = 25°C$ (or over operating temperature range if enclosed in parentheses), unless otherwise indicated.

[1] $R_L = 2k\Omega$ [2] $V_S = \pm 15V$

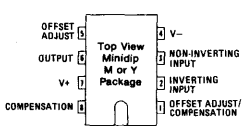


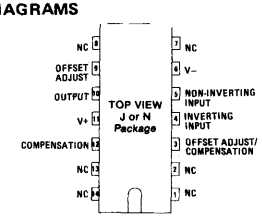
SG101/201, SG101A/201A/301A Chip
(See T-package diagram for pad functions)

Compensation and Optional Balancing Circuit



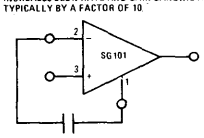
CONNECTION DIAGRAMS

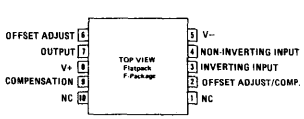


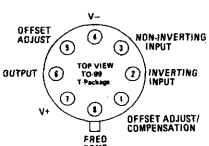


Feedforward Compensation

INCREASES SLEW RATE AND GAIN-BANDWIDTH TYPICALLY BY A FACTOR OF 10







SG107/207/307
SG741/741C

General-Purpose Compensated Operational Amplifiers

The SG107/207/307 offer excellent input bias currents and drift characteristics as well as short circuit protection and pin compatibility with the 741 class of amplifiers.

- 3mV max offset voltage over temperature
- 100 nA max input bias current over temperature
- 20nA max offset current over temperature
- Offsets guaranteed over full common mode range
- Guaranteed drift characteristics

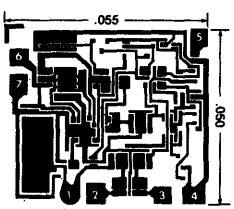
SG741/741C are pin compatible with the most widely accepted operational amplifiers and provide excellent performance for a wide range of applications.

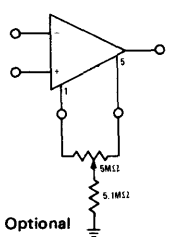
- Complete short circuit protection
- Offset voltage null capability
- High common mode voltage range
- High differential input voltage range

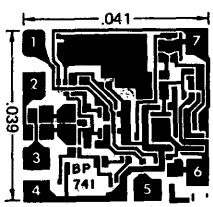
PARAMETERS*	107	207	307	741	741C	Units
Supply Voltage	±5 to ±20		±5 to ±20	±15	±15	V
Operating Temperature Range	−55 to +125	−25 to +85	0 to +70	−55 to +125	0 to +70	°C
Package Types	T, J, F, Y	T, J, F, Y, M, N		T, J, F, Y	T,J,Y,F,M,N	–
Input Offset Voltage	2.0 (3.0)		7.5 (10)	5.0 (6.0)	6.0 (7.5)	mV
Input Offset Current	10 (20)		50 (70)	200 (500)	200 (300)	nA
Input Bias Current	0.075 (0.1)		0.25 (0.3)	0.5 (1.5)	0.5 (0.8)	μA
Temp. Coeff. Input Offset Voltage	(15)[2]		(30)[2]	(3.0 typ)	(6.0 typ)	μV/°C
Temp. Coeff. Input Offset Current	(0.2)		(0.6)	(0.5 typ)	(0.5 typ)	nA/°C
Large Signal Voltage Gain	50 (25)		25 (15)	50 (25)	20 (15)	V/mV
Common Mode Rejection	(80)		(80)	(70)	70	dB
Power Supply Rejection	(100)		(100)	(150)	150	μV/V
Input Common Mode Range	+15, −12		+15, −12	±12	±12	V
Differential Input Voltage	±30		±30	±30	±30	V
Unity Gain Bandwidth	0.5 (typ)		0.5 (typ)	0.8 (typ)	0.8 (typ)	MHz
Slew Rate	0.2		0.2	0.3	0.3	V/μS
Supply Current	3.0		3.0	2.8	2.8	mA
Output Voltage Swing						
R_L = 2kΩ	±10		±10	±10	±10	V
R_L = 10kΩ	±12		±12	±12		V
Noise (typ)						
R_s = 1kΩ f = 10Hz to 10kHz	4		4	3	3	μV (rms) (typ)
R_s = 500kΩ f = 10Hz to 10kHz	25		25	25	25	

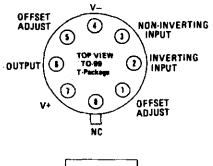
*Parameters apply over supply voltage range and are min./max. limits either at T_A = 25°C (or over operating temperature range if enclosed in parentheses), unless otherwise indicated.

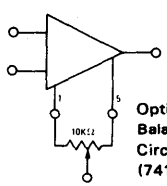
[1] V_S = ±15V [2] T_A = +25°C ≤ +125°C [3] Minimum recommended closed loop gain of 10.

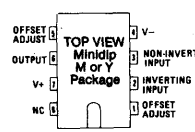


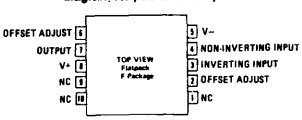


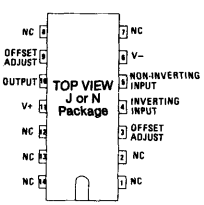












Silicon General

LINEAR INTEGRATED CIRCUITS

SG124/224/324

Quad Operational Amplifier

The SG124 series integrated circuit contains four true-differential, independent operational amplifiers. Each amplifier has been designed to operate from either a single supply voltage or plus and minus voltages and features internal frequency compensation, high gain, and very low supply current requirements. An additional significant advantage of these amplifiers is that when using a single supply, the input and output can be operated down to ground potential. Thus, they can be powered by a standard +5V DC logic supply and still be compatible with all forms of logic inputs and outputs.

- **Four internally compensated op amps in a single package**
- **Inputs and outputs can go to ground with a single supply voltage**
- **Input bias current is both low and constant with temperature**
- **Wide supply voltage compatibility with low current drain**
- **Available in 14-pin plastic or cerdip package**

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V^+	$32V_{DC}$ or $\pm16V_{DC}$
Differential Input Voltage	$32V_{DC}$
Input Voltage	$-0.3V_{DC}$ to $+32V_{DC}$
Power Dissipation (Note 1)	
N Package (plastic)	600mW
Derate above 25°C	6.0mW/°C
J Package (cerdip)	1000mW
Derate above 25°C	6.7mW/°C
Output Short-Circuit to Gnd (Note 2) $V^+ \leq 15V_{DC}$ and T_A = 25°C	Continuous
Operating Temperature Range	
SG124	−55°C to +125°C
SG224	−25°C to +85°C
SG324	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C

Electrical Characteristics (V^+ = +5V DC and T_A = 25°C unless otherwise noted)

Parameter	Conditions	SG124 Min.	SG124 Typ.	SG124 Max.	SG224/SG324 Min.	SG224/SG324 Typ.	SG224/SG324 Max.	Units
Input Offset Voltage	R_S = 0Ω	—	2	5	—	2	7	mV_{DC}
Input Bias Current (Note 3)	$[I_{IN}(+) + I_{IN}(-)]/2$	—	45	300	—	45	500	nA_{DC}
Input Offset Current	$I_{IN}(+) - I_{IN}(-)$	—	±3	±30	—	±5	±50	nA_{DC}
Input Common-Mode Voltage Range (Note 4)		0	—	V^+-1.5	0	—	V^+-1.5	V_{DC}
Supply Current	R_L = ∞ On All Op Amps	—	0.8	2	—	0.8	2	mA_{DC}
Large Signal Voltage Gain	$R_L \geq 2k\Omega$	—	100	—	—	100	—	V/mV
Output Voltage Swing	R_L = 2 kΩ	0	—	V^+-1.5	0	—	V^+-1.5	V_{DC}
Common Mode Rejection Ratio	DC	—	85	—	—	85	—	dB
Power Supply Rejection Ratio	DC	—	100	—	—	100	—	dB
Amplifier-to-Amplifier Coupling	f = 1 kHz to 20 kHz (Input Referred)	—	−120	—	—	−120	—	dB
Output Current Source	V_{IN}^+ = +1V_{DC}, V_{IN}^- = 0 V_{DC}	20	40	—	20	40	—	mA_{DC}
Output Current Sink	V_{IN}^- = +1 V_{DC}, V_{IN}^+ = 0 V_{DC}	10	20	—	10	20	—	mA_{DC}

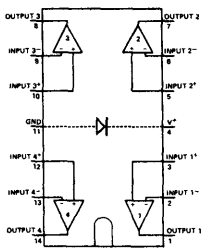
Note 1: For operating at high temperatures, the SG324 must be derated based on a +125°C maximum junction temperature and a thermal resistance of 175°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient. The SG224 and SG124 can be derated based on a +150°C maximum junction temperature.

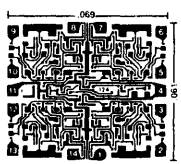
Note 2: Short circuits from the output to V^+ can cause excessive heating and eventual destruction. The maximum output current is approximately 40 mA independent of the magnitude of V^+. At values of supply voltage in excess of +15V_{DC}, continuous short-circuits can exceed the power dissipation ratings and cause eventual destruction.

Note 3: The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, *independent of the state of the output so no loading* change exists on the input lines.

Note 4: The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V^+-1.5V, but either or both inputs can go to +30V_{DC} without damage.

CONNECTION DIAGRAM





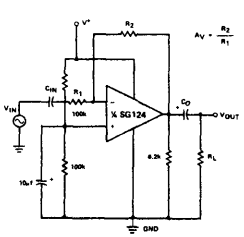
CHIP BONDING DIAGRAM

APPLICATIONS INFORMATION

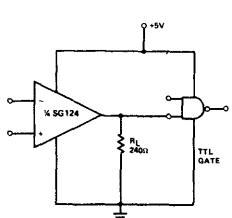
To reduce the power supply current drain, the amplifiers have a class A *output stage for small signal levels which converts to class B in a large* signal mode. This allows the amplifiers to both source and sink large output currents. Therefore both NPN and PNP external current boost transistors can be used to extend the power capability of the basic amplifiers. The output voltage needs to raise approximately 1 diode drop above ground to bias the on-chip vertical PNP transistor for output current sinking applications.

For AC applications, where the load is capacitively coupled to the output of the amplifier, a resistor should be used, from the output of the amplifier to ground to increase the class A bias current and prevent crossover distortion. Where the load is directly coupled, as in DC applications, there is no crossover distortion.

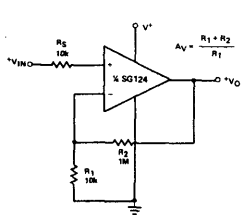
Capacitive loads which are applied directly to the output of the amplifier reduce the loop stability margin. Values of 50 pF can be accommodated using the worst-case non-inverting unity gain connection. Large closed loop gains or resistive isolation should be used if larger load capacitance must be driven by the amplifier.



SINGLE SUPPLY INVERTING AC AMPLIFIER WITH INPUT BIASED TO ONE-HALF SUPPLY



TTL INTERFACE



SINGLE SUPPLY NON-INVERTING DC AMPLIFIER (0V INPUT = 0V OUTPUT)

3.5 AMP POWER OP AMP

DESCRIPTION

The SG1173 is a monolithic operational amplifier with a high current output stage capable of sinking or sourcing up to 3.5 amps. It operates with supply voltages up to ±24V. Internal current limit, thermal shutdown, and on-chip compensation make the SG1173 easy to use both for new designs and retrofit applications. The input specifications of the amplifier are competitive with industry standard devices that offer much lower output currents.

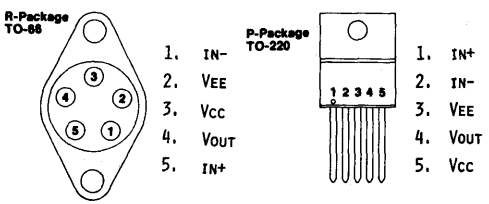
FEATURES

- **3.5 Amps output current**
- **Current limit and thermal shutdown protection**
- **Internal compensation**
- **Available in TO-220 and TO-66 packages**

APPLICATIONS

- **Motor drivers**
- **Servo systems**
- **Power amplifers**

CONNECTION DIAGRAMS (Top Views)

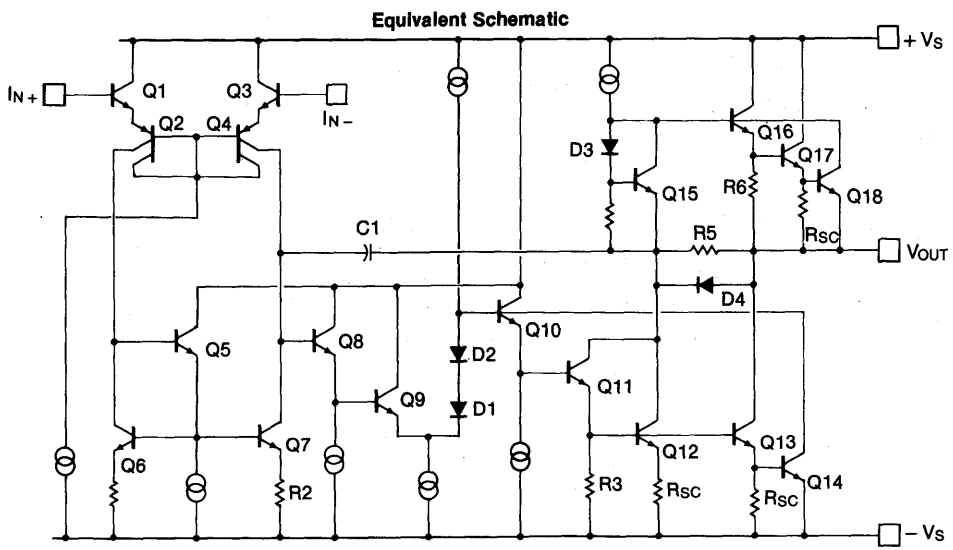


NOTE: CASE & TAB INTERNALLY CONNECTED TO VEE

PACKAGE INFORMATION

R-Package:TO-66	P-Package: TO-220
Θ_{JC} = 6°C/W max	Θ_{JC} = 5°C/W max
Θ_{JA} = 50°C/W max	Θ_{JA} = 65°C/W max
Order SG1173R SG3173R	Order SG1173P SG3173P

Equivalent Schematic



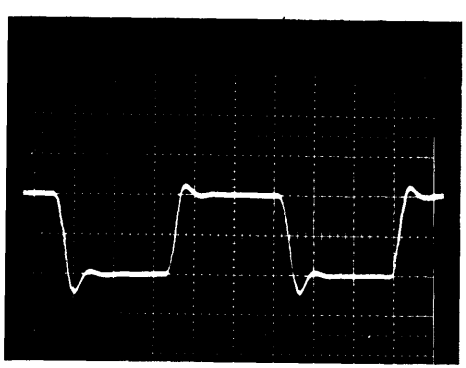
ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±25V
Output Current ..... Internally Limited
Differential Input Voltage ..... ±50V
Common Mode Voltage ..... ±25
Operating Junction Temp ..... 150°C

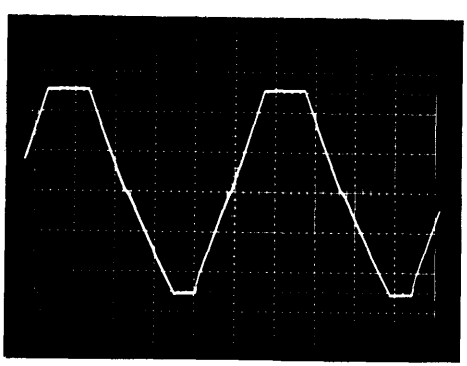
ELECTRICAL CHARACTERISTICS Vs = ±24V

SYMBOL	PARAMETER	CONDITIONS	1173			3173			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input Offset Voltage	25°C		2.0	4.0		2.0	6.0	mV
		$T_{low} - T_{high}$			6.0			8.0	mV
I_{IB}	Input Bias Current	25°C		250	500		250	700	nA
		$T_{low} - T_{high}$			750		1000		nA
I_{IO}	Input Offset Current	25°C		50	150		50	200	nA
		$T_{low} - T_{high}$			250			300	nA
V_{OUT}	Output Voltage Swing	R_L = 10Ω 25°C	±18	±20		±18	±20		Volts
		$T_{low} - T_{high}$	±17.5			±17.5			Volts
I_{OS}	Output Short Circuit Current	25°C	±3.5			±3.5			Amps
CMRR	Common Mode Rejection Ratio	ΔV_{CM} = ±12V 25°C	76	90		70	90		dB
		$T_{low} - T_{high}$	70						dB
PSRR	Power Supply Rejection Ratio	ΔV_S = 12V 25°C	80	90		76	90		dB
		$T_{low} - T_{high}$	74						dB
A_{VOL}	Open Loop Voltage Gain	$R_{L=10\Omega}$ $V_{OUT=10V}$ 25°C	40K	100k		25K	100k		V/V
		$T_{low} - T_{high}$	25K						V/V
I_S	Supply Current	25°C			20			20	mA
		$T_{low} - T_{high}$			30				mA

Notes: T_{low} = −55°C for SG1173R, 0°C for SG1173P and SG3173
T_{high} = 125°C for SG1173R, 70°C for SG1173P and SG3173



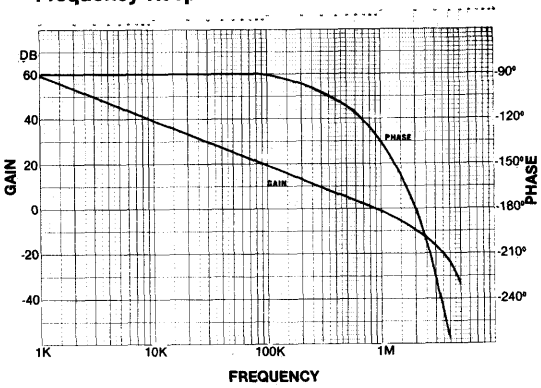
Small Signal Transient Response
50mV/vertical division
1μsec/horizontal division



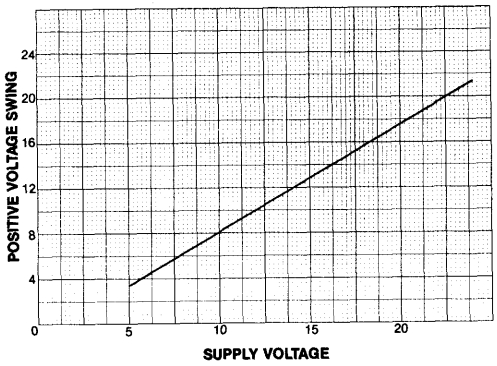
Large Signal Transient Response
5 V/vertical division
20μ sec/horizontal division

TYPICAL PERFORMANCE CHARACTERISTICS

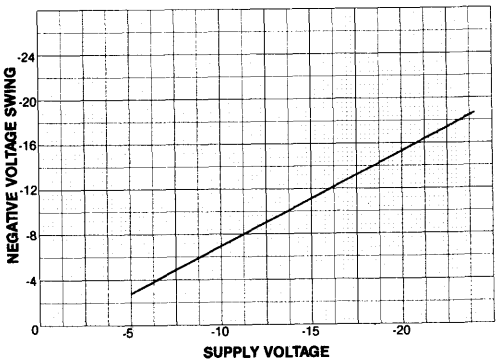
Frequency Response



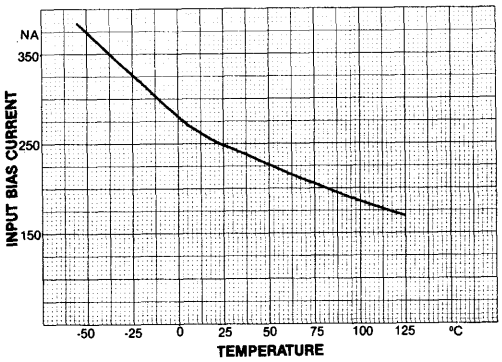
Positive Voltage Swing



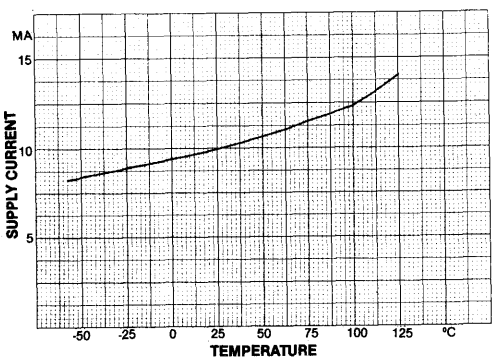
Negative Voltage Swing



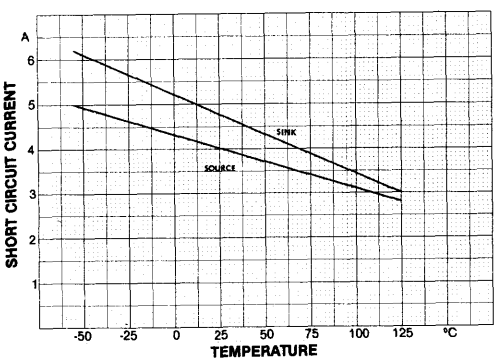
Input Bias Current



Supply Current



Short Circuit Current



APPLICATIONS

Proper usage of the SG1173 requires the same design and layout considerations used with other op amps. Power supplies should be adequately bypassed and clamped with Zener diodes if transients are a problem. Leads to high impedance nodes should be kept as short as possible to minimize undesirable input-output coupling or RF pick-up. In addition to these, the high current capability of the SG1173 presents some new challenges that a designer must be aware of. Special care should be taken to avoid spurious feedback due to ground loops or voltage drops in high current paths. Kelvin connections should be used when applicable. When driving inductive loads, protection diodes must be used to clamp the output voltage to the power supplies. This protects the amplifier from high voltage transients caused by the stored energy in the inductor. Some loads may require external load compensation. Examples of this are shown in Figure 1 and 2. Safe operating area (SOA) is another area where extreme care must be used. Simultaneous conditions of high current and high voltage on the part may cause the junction temperature to exceed the maximum rating. In any application, the worst case power dissipations should be calculated and adequate heat sinking must be provided.

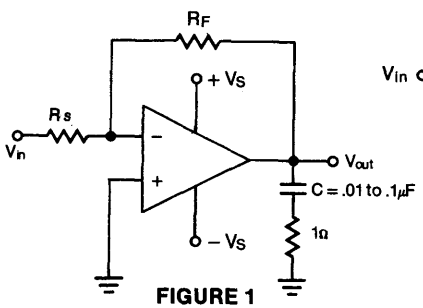


FIGURE 1
Inverting amplifier with RC load compensation

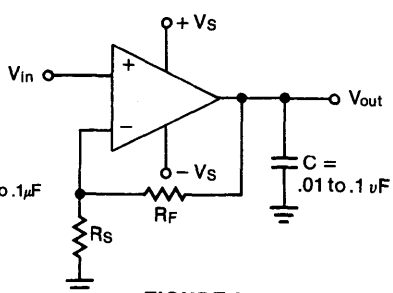


FIGURE 2
Non-inverting amplifier with capacitive load compensation

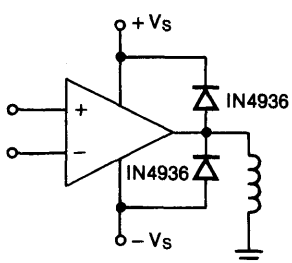


FIGURE 3
Protection diodes used with inductive load

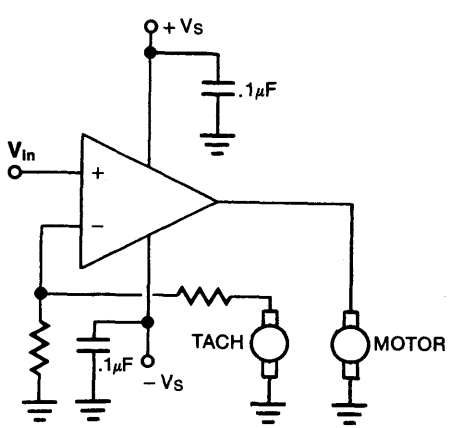


FIGURE 4
Motor speed control with tachometer feedback.

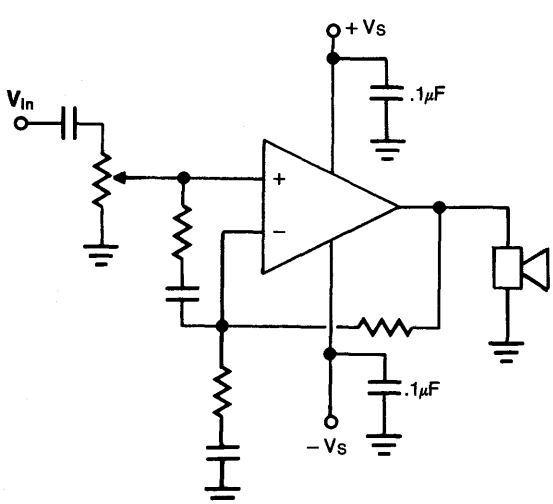


FIGURE 5
Audio Amplifier

SG1253/SG2253/SG3253

Low Power Operational Amplifiers — Triple

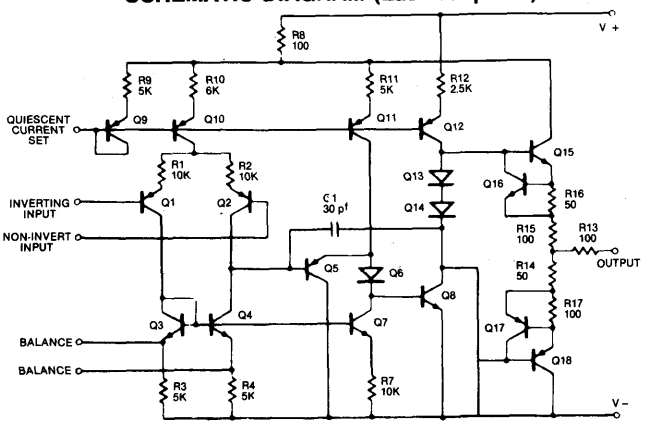
DESCRIPTION

SG1253/2253/3253 operational amplifiers are triple operational amplifiers which have been designed to offer exceptional performance under conditions of extremely low internal power consumption. Quiescent current is determined by a single external resistor which permits operation over a wide range of currents and voltages.

FEATURES

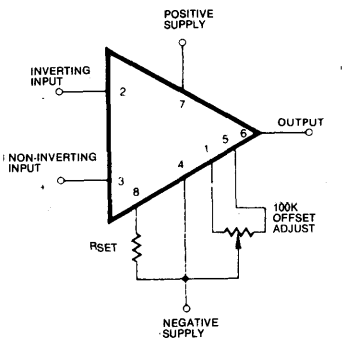
- **Adjustable power consumption to less than 20 microwatts**
- **Supply voltages from ± 0.75 to ± 18 volts**
- **Less than 15 nA bias currents**
- **Complete short-circuit protection**
- **Internally compensated**

SCHEMATIC DIAGRAM (Each Amplifier)



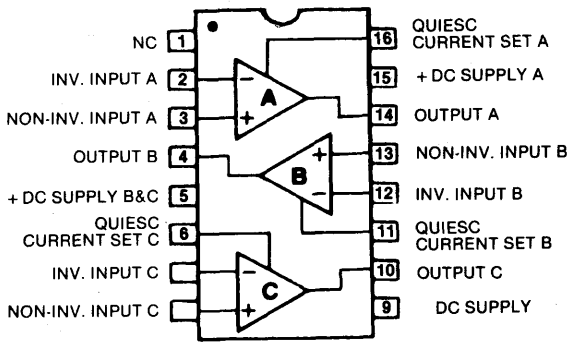
NOTE: Balance adjust not available in triple op amp.

CONNECTION DIAGRAM



NOTE: R_{SET} is required to establish the internal operating currents. Its value may be determined on the table given on page 2.

TRIPLE



TOP VIEW
SG1253/2253/3253

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Differential Input Voltage (Note 1)	±15V
Common Mode Input Voltage (Note 2)	±15V
Output Short Circuit Duration	Indefinite (Note 3)
Power Dissipation (Pkg. Limitation)	
J-Package	1000mW
Derate above 25°C	8.0mW/°C
Storage Temperature Range	
J-Package	−65°C to +150°C
M-Package	−55°C to +125°C

Note 1. This rating applies to maximum voltage differential between input terminals. The maximum input voltage on either input terminal is limited to supply voltage up to a limit of ± 15V.

Note 2. This rating limited to ± supply voltage to a maximum of ± 15V.

Note 3. With the output shorted to ground or either supply. Rating applies to +125°C case temperature or +75°C ambient temperature.

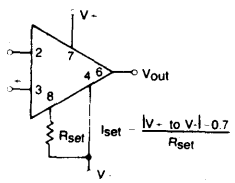
SETTING QUIESCENT CURRENT

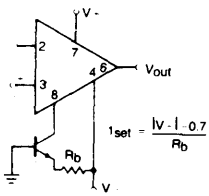
RESISTOR BIASING

Vs	QUIESCENT CURRENT 10μA	30μA	100μA	300μA
±1.5	1.5MΩ	470KΩ	150KΩ	– –
±3	3.3MΩ	1.1MΩ	330KΩ	100KΩ
±6	7.5MΩ	2.7MΩ	750KΩ	220KΩ
±9	13MΩ	4MΩ	1.3MΩ	350KΩ
±12	18MΩ	5.6MΩ	1.5MΩ	510KΩ
±15	22MΩ	7.5MΩ	2.2MΩ	620KΩ

CURRENT SOURCE BIASING

IQ	10μA	30μA	100μA	300μA
Iset	1.3μA	4μA	15μA	50μA





ELECTRICAL CHARACTERISTICS

PARAMETERS/CONDITIONS		1253[1]	2253[1]	3253[1]	UNITS
Operating Temperature Range		−55 to +125	0 to +70	0 to +70	°C
Supply Voltage		±18			
Differential Input Voltage[3]		±15			
Common Mode Range[3]		±15			
Input Offset Voltage	RS ≤ 100KΩ RS ≤ 10KΩ	– 3(4)	– 3(4)	– 6.0(7.5)	mV
Input Bias Current	VS = ±3V VS = ±15V	18(20) 12(15)	18(20) 12(15)	40(50) 25(30)	nA
Input Offset Current		5(8)	5(8)	10(15)	nA
Input Resistance		3	3	3	M
Large Signal Voltage Gain	RL = 10K VS = ±3V RL = 10K VS = ±15V	40(25 400(50)	40(25) 100(50)	40(25) 75(50)	V/mV
Output Voltage Swing	VS = ±3V, RL = 10KΩ VS = ±15V, RL = 10KΩ		±1.5(±1.0) ±11(±10)		V
CMRR RS ≤ 10KΩ		(70)	(70)	(70)	dB
PSRR RS ≤ 10KΩ	VS = 3V VS = ±15V	(200) (150)	(200) (150)	(200) (150)	μV/V
Power Consumption	VS = ±3V VS = ±15V, RL = 0	(240) (1200)	(240) (1200)	(240) (1200)	μW
Average TC of Offset Voltage	RS = 10K (±15V for 1250)	4(typ)	4(typ)	6(typ)	μV/°C
Average TC of Offset Current	RS = 20K (±15V for 1250)	2(typ)	2(typ)	1(typ)	pA/°C
Equiv. Input Noise Voltage	f=10Hz (±15V for 1250)	35(typ)	35(typ)	35(typ)	nV/√Hz
Equiv. Input Noise Current	f=10Hz (±15V for 1250)	0.5(typ)	0.5(typ)	0.5(typ)	pA/√Hz
Slew Rate	RL = 10K, CL = 100pF	0.2(typ)	0.2(typ)	0.2(typ)	V/μS
Small Signal Unity Gain-Bandwidth	Rf = 0 Vin = 20mV, RL = 20KΩ	–	–	–	kHz

Parameters for the SG1253 are min/max limits either at T_A = 25°C (or over operating temperature range if enclosed in parentheses), for supply voltage of +3V to +15V and for a quiescent current of 30 A established by an R_{set} of 1.1.

Silicon General

LINEAR INTEGRATED CIRCUITS

SG1536/1436/1436C

General-Purpose Compensated Operational Amplifiers

SG1536/1436/1436C are intended specifically for use in high voltage applications where high common mode input ranges, high output voltage swings and low input currents are required. These devices are internally compensated and are pin compatible with industry-standard operational amplifiers.

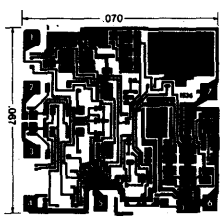
- Usable with up to ±40V supplies
- Provides up to ±30V output voltage swing
- Common mode voltages to ±24V
- Input current 35nA max over temperature

PARAMETERS*	1536[1]	1436[1]	1436C[1]	UNITS
Supply Voltage	±40	±34	±30	V
Operating Temperature Range	−55 to +125	0 to +75	0 to +75	°C
Package Types	T.Y.			–
Input Offset Voltage	5.0 (7.0)	10	12	mV
Input Offset Current	3.0 (7.0)	10 (14)	25	nA
Input Bias Current	20 (35)	40 (55)	90	nA
Large Signal Voltage Gain	100 (50)	70 (50)	50	V/mV
Common Mode Rejection	80	70	50	dB
Power Supply Rejection	100	200	50	μV/V
Input Common Mode Range[2]	±24	±22	±18	V
Differential Input Voltage (V)	±(V⁺ + |V⁻| − 3V)			V
Unity Gain Bandwidth	1.0 (typ)	1.0 (typ)	1.0 (typ)	MHz
Slew Rate[4]	2.0 (typ)	2.0 (typ)	2.0 (typ)	V/μS
Supply Current	4.0	5.0	5.0	mA
Output Voltage Swing R_L = 2kΩ	±22[1]	±20[1]	±20[1]	V
R_L = 10kΩ	±30[5]	–	–	V
Noise (typ) A_V = 100, R_S = 10kΩ, f = 1.0 KHz, BW = 1.0Hz	50	50	50	nV/(Hz)½ (typ)

*Parameters apply over supply voltage range and are min./max. limits either at T_A = 25°C (or over operating temperature range if enclosed in parentheses), unless otherwise indicated.

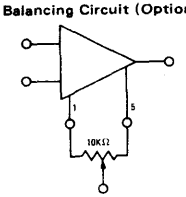
[1] V_S = ±28V [2] V_S = ±15V [3] Inputs are shunted with back-to-back diodes for over voltage protection

[4] R_L = 5 kΩ [5] R_L = 5.0kΩ, V_S = ±36V.

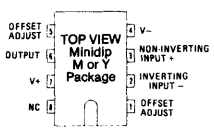


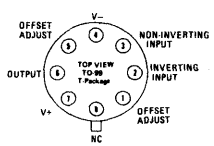
SG1536/1436/1436C Chip (See T-package diagram for pad functions)

Balancing Circuit (Optional)



CONNECTION DIAGRAMS





INTERFACE CIRCUITS

Sense Amplifiers

Core Drivers

Dual Peripheral Drivers

Dual Sense Amplifier/Data Registers

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC+}		4.75	5	5.25	V
Supply voltage, V_{CC-}		−4.75	−5	−5.25	V
Reference voltage, V_{ref}		±1.5	±2.1	±4.5	V
High-level output voltage, V_{OH}	Detector and buffer			V_{CC}	V
High-level output current, I_{OH}	Register			−400	μA
Low-level output current, I_{OL}	Register			16	mA
	Buffer			25	
	Detector			3.2	
Width of reset pulse, $t_{w(R)}$		115			ns

Supply voltages (see Note 1)
- V_{CC+} . . . . . 7 V
- V_{CC-} . . . . . −7 V

Reference voltage, V_{ref} . . . . . ±5 V
Differential input voltage, V_{ID} . . . . . ±5 V
Voltage from any input to ground . . . . . 5.25 V
Continuous total dissipation at (or below) 70°C free-air temperature (see Note 3) . . . . 450 mW
Operating free-air temperature range: SG 55236 . . . . . −55°C to 125°C
SG 75236 . . . . . 0°C to 70°C
Storage Temperature range . . . . . −65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds . . . . . 300°C

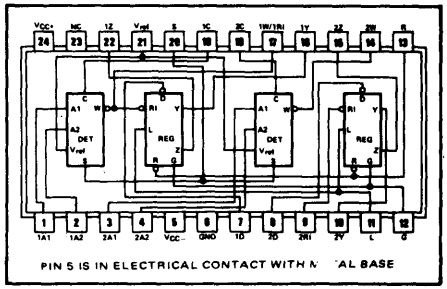
NOTE: 1. Voltage values, except differential input voltage, are with respect to the network ground terminal.

electrical characteristics over recommended operating free-air temperature range, $V_{ref} = \pm 2.1$V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_T	Differential-input threshold voltage (see Note 3)		V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 25°C	SG55236	5	7	9	mV
				SG75236	4	7	10	
			V_{CC+} = 5 V ± 5%, V_{CC-} = −5 V ± 5%	SG55236	4.5	7	9.5	
			V_{CC+} = 5 V, V_{CC-} = −5 V	SG75236	4	7	10	
V_{ICF}	Common-mode input firing voltage		f = 0.1 MHz to 20 MHz			±1.5		V
I_{IB}	Differential-input bias current		V_{CC+} = 5 V, V_{CC-} = −5 V, V_{ID} = 0			20		μA
I_{IO}	Differential-input offset current		V_{CC+} = 5 V, V_{CC-} = −5 V, V_{ID} = 0			0.5		μA
V_{IH}	High-level input voltage (strobe and logic inputs)				2			V
V_{IL}	Low-level input voltage (strobe and logic inputs)						0.8	V
V_{OH}	High-level output voltage	Register	V_{CC+} = 4.75 V, V_{CC-} = −4.75 V, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −400 μA		2.4			V
		Detector	V_{CC+} = 4.75 V, V_{CC-} = −4.75 V, V_{IH} = 2 V, V_{IL} = 0.8 V					
I_{OH}	High-level output current	Buffer	V_{CC+} = 4.75 V, V_{CC-} = −4.75 V, V_{IH} = 2 V, V_{IL} = 0.8 V, V_{OH} = 4.75 V				250	μA
V_{OL}	Low-level output voltage	Register	V_{CC} = 4.75 V, V_{CC-} = −4.75 V, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA				0.4	V
		Buffer	V_{CC} = 4.75 V, V_{CC-} = −4.75 V, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 25 mA				0.5	V
		Detector	V_{CC} = 4.75 V, V_{CC-} = −4.75 V, V_{IH} = 2 V, V_{IL} = 0.8 V				0.4	V
I_I	Input current at maximum input voltage (logic inputs)		V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{IH} = 5.25 V				1	mA
I_{IH}	High-level input current	Data in or channel select	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{IH} = 2.4 V				40	μA
		Register input 2RI					−750	
		Strobe, reset, or buffer input					80	
		Data load					160	
I_{IL}	Low-level input current	Strobe, reset, or buffer input	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{IL} = 0.4 V				−3.2	mA
		Register input 2RI					−3	
		Channel select					−1.6	
		Data load					−6.4	
		Data in					−2	
I_{OS}	Short-circuit output current‡	Register	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_O = 0		−20		−60	mA
I_{ref}	Reference-input current		V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{ref} = −2.1 V, T_A = 25°C				0.5	mA
I_{CC+}	Supply current from V_{CC+}		V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, T_A = 25°C				55	mA
I_{CC-}	Supply current from V_{CC-}		V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, T_A = 25°C				18	mA

HIGH-SPEED SENSE AMPLIFIERS WITH BUILT-IN DATA REGISTER AND BUFFER FOR APPLICATION IN COINCIDENT-CURRENT CORE MEMORIES

- ± 2-mV Threshold Sensitivity with Threshold Voltage Independent of Temperature and Supply-Voltage Variations
- Adjustable Differential-Input Threshold Voltage
- Reference Amplifier Inherently Stable with No External Frequency Compensation Required
- Built-In Data Register with Provisions for External Data Inputs
- Built-In Data Buffer Drives 450-pF Load in 15 ns
- Low Power Consumption
- Internal Reference Voltage Attenuator Makes Reference Amplifier Less Sensitive to Noise
- Two Independent Channels with TTL Compatible Logic Inputs and Outputs



NC—No internal connection

FUNCTION TABLE

INPUTS							OUTPUTS	
A	C	S	W/R1†	L	D	R	G	Y	Z
H	H	H	L	X	X	X	H	H	L
H	H	H	L	X	X	X	L	H	H
↓	H	H	↑	L	X	H	H	H	L
↓	H	H	↑	L	X	H	L	H	H
H	↓	H	↑	L	X	H	H	H	L
H	↓	H	↑	L	X	H	L	H	H
H	H	↓	↑	L	X	H	H	H	L
H	H	↓	↑	L	X	H	L	H	H
L	X	X	H	H	H	X	X	L	H
L	X	X	H	H	L	X	H	H	L
L	X	X	H	H	L	X	L	H	H
L	X	X	H	L	X	L	X	L	H
L	X	X	H	L	X	↑	X	L	H
X	L	X	H	H	H	X	X	L	X
X	L	X	H	H	L	X	H	H	L
X	L	X	H	H	L	X	L	H	H
X	L	X	H	L	X	L	X	L	H
X	L	X	H	L	X	↑	X	L	H
X	X	L	H	H	H	X	X	L	X
X	X	L	H	H	L	X	H	H	L
X	X	L	H	H	L	X	L	H	H
X	X	L	H	L	X	L	X	L	H
X	X	L	H	L	X	↑	X	L	H

The normal sequence of operation is shown in the timing diagram.

FUNCTION TABLE FOR DUAL-CHANNEL DETECTOR OPERATION (2W connected to 1W/1R1)

INPUTS					OUTPUT
1A	1C	2A	2C	S	1W·2W
H	H	X	X	H	L
X	X	H	H	H	L
↓	H	L	X	H	↑
↓	H	X	L	H	↑
L	X	↓	H	H	↑
X	L	↓	H	H	↑
Any Other Combination					H

H = high level (steady state), L = low level (steady state)
X = irrelevant (any input, including transitions)
↓ = transition from high level to low level, ↑ = transition from low level to high level
†The W/R1 column shows the output from the detector resulting from the inputs A, C, and S. In positive logic, W = $\overline{ACS}$. For dual operation with 2W connected to 2R1, this column represents an intermediate node and can be ignored.

For independent operation of register 2, this column is an input and the A, C, and S columns should be ignored.

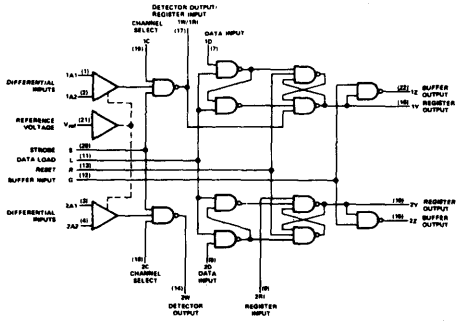
For dual-channel operation with 2W connected to 1W/1R1, this column is the result of W = $\overline{S(1A \cdot 1C + 2A \cdot 2C)}$ as shown in the table above.

definition of logic levels

INPUT	H	L
A‡	$V_{ID} > V_{T\ max}$	$V_{ID} < V_{T\ min}$
LOGIC	$V_I > V_{IH\ min}$	$V_I < V_{IL\ max}$

‡A is a differential voltage (V_{ID}) between A1 and A2. For these circuits, V_{ID} is consider positive regardless of which terminal is positive with respect to the other.

functional block diagram



Memory Drivers

PERFORMANCE

- 600-mA Output Capability
- Fast Switching Times
- Output Short-Circuit Protection
- Dual Sink and Dual Source Outputs
- Minimum Time Skew between Address and Output Current Rise
- 24-Volt Output Capability

EASE OF DESIGN

- Source Base Drive Externally Adjustable
- TTL or DTL Compatibility
- Input Clamping Diodes
- Transformer Coupling Eliminated
- Reliability Increased
- Drive-Line Lengths Reduced
- Use of External Components Minimized

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		SG55325	SG75325	UNIT
Supply voltage V_{CC1} (see Note 1)		7	7	V
Supply voltage V_{CC2} (see Note 1)		25	25	V
Input voltage (any address or strobe input)		5.5	5.5	V
Continuous total dissipation at (or below) 100°C case temperature		1	1	W
Operating free-air temperature range		−55 to 125	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	°C
Lead temperature 1/16 inch from case for 60 seconds	J package	300	300	°C
Lead temperature 1/16 inch from case for 10 seconds	N package	260	260	°C

NOTE: 1. Voltage values are with respect to network ground terminal.

electrical characteristics over rated operating free-air temperature range (unless otherwise noted)

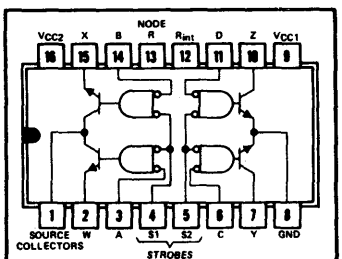
PARAMETER			TEST CONDITIONS		SG55325 MIN	SG55325 TYP†	SG55325 MAX	SG75325 MIN	SG75325 TYP†	SG75325 MAX	UNIT
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.8			0.8	V
V_I	Input clamp voltage		V_{CC1} = 4.5 V, I_I = −10 mA,	V_{CC2} = 24 V, T_A = 25°C		−1.3	−1.7		−1.3	−1.7	V
$I_{(off)}$	Source-collectors terminal off-state current		V_{CC1} = 4.5 V, V_{CC2} = 24 V	Full range			500			200	μA
				T_A = 25°C		3	150		3	200	
V_{OH}	High-level sink output voltage		V_{CC1} = 4.5 V, I_O = 0	V_{CC2} = 24 V,	19	23		19	23		V
$V_{(sat)}$	Saturation voltage	Source outputs	V_{CC1} = 4.5 V, V_{CC2} = 15 V, R_L = 24 Ω, $I_{(source)}$ ≈ −600 mA,	Full range			0.9			0.9	V
				T_A = 25°C		0.43	0.7		0.43	0.75	
		Sink outputs	V_{CC1} = 4.5 V, V_{CC2} = 15 V, R_L = 24 Ω, $I_{(sink)}$ ≈ 600 mA,	Full range			0.9			0.9	
				T_A = 25°C		0.43	0.7		0.43	0.75	
I_I	Input current at maximum input voltage	address inputs	V_{CC1} = 5.5 V, V_I = 5.5 V	V_{CC2} = 24 V,			1			1	mA
		strobe inputs					2			2	
I_{IH}	High-level input current	address inputs	V_{CC1} = 5.5 V, V_I = 2.4 V	V_{CC2} = 24 V,		3	40		3	40	μA
		strobe inputs				6	80		6	80	
I_{IL}	Low-level input current	address inputs	V_{CC1} = 5.5 V, V_I = 0.4 V	V_{CC2} = 24 V,		−1	−1.6		−1	−1.6	mA
		strobe inputs				−2	−3.2		−2	−3.2	
$I_{CC(off)}$	Supply current, all sources and sinks off	from V_{CC1}	V_{CC1} = 5.5 V, T_A = 25°C	V_{CC2} = 24 V,		14	22		14	22	mA
		from V_{CC2}				7.5	20		7.5	20	
I_{CC1}	Supply current from V_{CC1}, either sink on		V_{CC1} = 5.5 V, $I_{(sink)}$ = 50 mA,	V_{CC2} = 24 V, T_A = 25°C		55	70		55	70	mA
I_{CC2}	Supply current from V_{CC2}, either source on		V_{CC1} = 5.5 V, $I_{(source)}$ = −50 mA,	V_{CC2} = 24 V, T_A = 25°C,		32	50		32	50	mA

switching characteristics, V_{CC1} = 5 V, T_A = 25°C

PARAMETER¶	TO (OUTPUT)	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Source collectors	9	V_{CC2} = 15 V, R_L = 24 Ω,		25	50	ns
t_{PHL}			C_L = 25 pF		25	50	
t_{TLH}	Source outputs	10	V_{CC2} = 20 V, R_L = 1 kΩ,		55		ns
t_{THL}			C_L = 25 pF		7		
t_{PLH}	Sink outputs	9	V_{CC2} = 15 V, R_L = 24 Ω,		20	45	ns
t_{PHL}			C_L = 25 pF		20	45	
t_{TLH}	Sink outputs	9	V_{CC2} = 15 V, R_L = 24 Ω,		7	15	ns
t_{THL}			C_L = 25 pF		9	20	
t_s	Sink outputs	9	V_{CC2} = 15 V, R_L = 24 Ω, C_L = 25 pF		15	30	ns

¶ t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output
t_{TLH} = transition time, low-to-high-level output
t_{THL} = transition time, high-to-low-level output
t_s = storage time

J, OR N DUAL-IN-LINE
OR F FLAT PACKAGE (TOP VIEW)



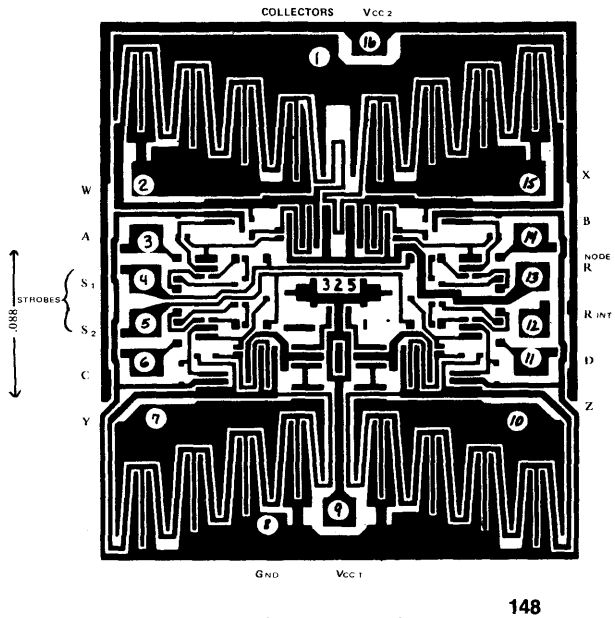
PIN 8 OF THE F FLAT PACKAGES IS IN ELECTRICAL CONTACT WITH THE METAL BASE

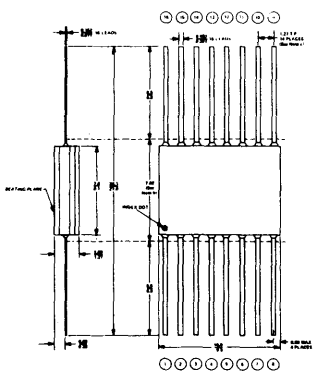
positive logic: See truth table

TRUTH TABLE

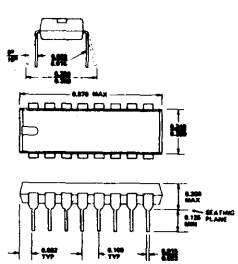
ADDRESS INPUTS				STROBE INPUTS		OUTPUTS			
SOURCE		SINK		SOURCE	SINK	SOURCE		SINK	
A	B	C	D	S1	S2	W	X	Y	Z
L	H	X	X	L	H	ON	OFF	OFF	OFF
H	L	X	X	L	H	OFF	ON	OFF	OFF
X	X	L	H	H	L	OFF	OFF	ON	OFF
X	X	H	L	H	L	OFF	OFF	OFF	ON
X	X	X	X	H	H	OFF	OFF	OFF	OFF
H	H	H	H	X	X	OFF	OFF	OFF	OFF

H = high level, L = low level, X = irrelevant
NOTE: Not more than one output is to be on at any one time.





F-FLAT PACKAGE
16 PIN CERAMIC



N-PACKAGE
16-PIN PLASTIC

Memory Drivers

FEATURES

- Quad Positive or Sink Memory Drivers
- 600 mA Output Current Sink Capability
- 24V Output Capability
- Clamp Voltage Variable to 24V
- SG55327, SG75327 PERFORMANCE
- Quad Memory Switches
- 600 mA Output Current Capability
- VCC2 Drive Voltage Variable to 24V
- Output Capable of Swinging Between VCC2 and Ground
- High-Repetition-Rate Driver Compatible with High-Speed Magnetic Memories
- Inputs Compatible with TTL Decoders
- Minimum Time Skew between Strobe and Output-Current Rise
- Pulse-Transformer Coupling Eliminated
- Drive-Line Lengths Reduced

ABSOLUTE MAXIMUM RATINGS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

	SG55326	SG75326	SG55327	SG75327	UNIT
Supply voltage, V_{CC} or V_{CC1} (see Note 1)	7	7	7	7	V
Supply voltage, V_{CC2}			25	25	V
Input voltage, any address or strobe	5.5	5.5	5.5	5.5	V
Output collector voltage	25	25	25	25	V
Output clamp voltage	25	25			V
Output collector current	750	750	750	750	mA
Continuous total dissipation at (or below) 100°C case temperature (see Note 2)	1	1	1	1	W
Operating free-air temperature range	−55 to 125	0 to 70	−55 to 125	0 to 70	°C
Storage temperature range	−65 to 150	−65 to 150	−65 to 150	−65 to 150	°C
Lead temperature 1/16 inch from case for 60 seconds: J, Y or M package	300	300	300	300	°C
Lead temperature 1/16 inch from case for 10 seconds: N package	260	260	260	260	°C

recommended operating conditions

	SG55326			SG75326			SG55327			SG75327			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC} or V_{CC1}	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
Supply voltage, V_{CC2}							4.5		24	4.5		24	V
Output collector voltage			24			24			24			24	V
Output-clamp voltage, $V_{(clamp)}$	4.5		24	4.5		24							V
Output collector current			600			600			600			600	mA
Operating free-air temperature, T_A	−55		125	0		70	−55		125	0		70	°C

NOTE: 1. Voltage values are with respect to network ground terminal(s).

SG55326, SG75326 electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SG55326			SG75326			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.8			0.8	V
V_I	Input clamp voltage		V_{CC} = 4.5 V, T_A = 25°C	I_I = −10 mA,		−1	−1.7		−1	−1.7	V
V_{OH}	High-level output voltage		V_{CC} = 4.5 V,	I_O = 0	19	23		19	23		V
$V_{(sat)}$	Saturation voltage		V_{CC} = 4.5 V, $I_{(sink)}$ = 600 mA§, See Note 3	Full range			0.9			0.9	V
				T_A = 25°C		0.43	0.7		0.43	0.75	
$V_{F(clamp)}$	Output-clamp-diode forward voltage		$V_{(clamp)}$ = 0, T_A = 25°C	$I_{(clamp)}$ = −10 mA,			1.5			1.5	V
$I_{(clamp)}$	Output-clamp current, one output on		$I_{(sink)}$ = 50 mA,	T_A = 25°C		5	7		5	7	mA
I_I	Input current at maximum input voltage	Address	V_I = 5.5 V				1			1	mA
		Strobe					4			4	
I_{IH}	High-level input current	Address	V_I = 2.4 V				40			40	μA
		Strobe					160			160	
I_{IL}	Low-level input current	Address	V_I = 0.4 V			−1	−1.6		−1	−1.6	mA
		Strobe				−4	−6.4		−4	−6.4	
$I_{CC(off)}$	Supply current, all outputs off		All inputs at 5 V,	T_A = 25°C		18	25		18	25	mA
$I_{CC(on)}$	Supply current, one output on		$I_{(sink)}$ = 50 mA,	T_A = 25°C		58	75		58	75	mA

SG55326, SG75326 switching characteristics, V_{CC} = 5V, T_A = 25°C

PARAMETER¶	TO (OUTPUT)	TEST CONDITIONS§	MIN	TYP	MAX	UNIT
t_{PLH}	W, X, Y, or Z	V_S = $V_{(clamp)}$ = 15 V, R_L = 24 Ω, C_L = 25 pF, See Figure 5		30	50	ns
t_{PHL}				25	50	
t_{TLH}	W, X, Y, or Z			7	15	ns
t_{THL}				10	20	
t_s	W, X, Y, or Z			24	35	ns
V_{OH}	W, X, Y, or Z	V_S = $V_{(clamp)}$ = 24 V, R_L = 47 Ω, C_L = 25 pF, $I_{(sink)}$ = 500 mA, See Figure 5	V_S−25			mV

SG55327, SG75327 electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

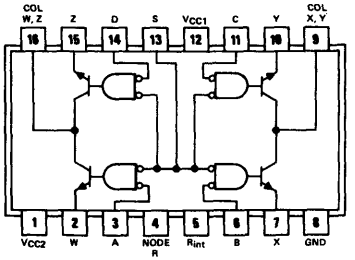
PARAMETER			TEST CONDITIONS†		SG55327			SG75327			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.8			0.8	V
V_I	Input clamp voltage		V_{CC} = 4.5 V, T_A = 25°C	I_I = −10 mA		−1	−1.7		−1	−1.7	V
$I_{(off)}$	Collectors terminal off-state current		V_{CC1} = 4.5 V, $V_{(col)}$ = 24 V	Full range			500			200	μA
				T_A = 25°C			150			200	
$V_{(sat)}$	Saturation voltage		V_{CC1} = 4.5 V, V_O = 0, $I_{(source)}$ = −600 mA§, See Notes 3 and 4	Full range			0.9			0.9	V
				T_A = 25°C		0.43	0.7		0.43	0.75	
I_I	Input current at maximum input voltage	Address	V_I = 5.5 V				1			1	mA
		Strobe					4			4	
I_{IH}	High-level input current	Address	V_I = 2.4 V				40			40	μA
		Strobe					160			160	
I_{IL}	Low-level input current	Address	V_I = 0.4 V			−1	−1.6		−1	−1.6	mA
		Strobe				−4	−6.4		−4	−6.4	
$I_{CC(off)}$	Supply current, all outputs off	From V_{CC1}	All inputs at 5 V,	T_A = 25°C		7	10		7	10	mA
		From V_{CC2}				13	20		13	20	
$I_{CC(on)}$	Supply current, one output on	From V_{CC1}	$V_{(col)}$ = 6 V, T_A = 25°C,	$I_{(source)}$ = −50 mA, See Note 3		8	12		8	12	mA
		From V_{CC2}				36	55		36	55	

SG55327, SG75327 switching characteristics, V_{CC1} = 5V, T_A = 25°C

PARAMETER¶	TO (OUTPUT)	TEST CONDITIONS§	MIN	TYP	MAX	UNIT
t_{PLH}	Collectors	V_S = V_{CC2} = 15 V, R_L = 24 Ω, C_L = 25 pF, See Figure 5 and Note 4		35	55	ns
t_{PHL}	W, Z or X, Y			30	55	
t_{TLH}	W, X, Y, or Z	$V_{(col)}$ = V_{CC2} = 20 V, R_L = 100 Ω, C_L = 25 pF, See Figure 6 and Note 4		30		ns
t_{THL}				10		
V_{OH}	Collectors W, Z or X, Y	V_S = V_{CC2} = 24 V, R_L = 47 Ω, C_L = 25 pF, $I_{(sink)}$ ≈ 500 mA, See Figure 5 and Note 4	V_S−25			mV

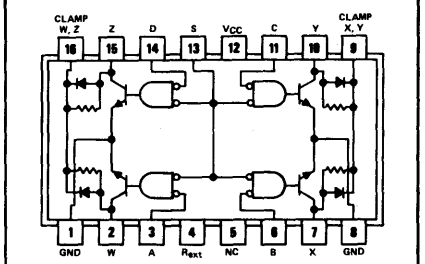
CONNECTION DIAGRAMS

SG55327, SG75327
J OR N DUAL-IN-LINE OR
F FLAT PACKAGE (TOP VIEW)



PIN 8 OF J AND N PACKAGES IS IN ELECTRICAL CONTACT WITH THE METAL BASE

SG55326, SG75326
J OR N DUAL-IN-LINE OR
F FLAT PACKAGE (TOP VIEW)

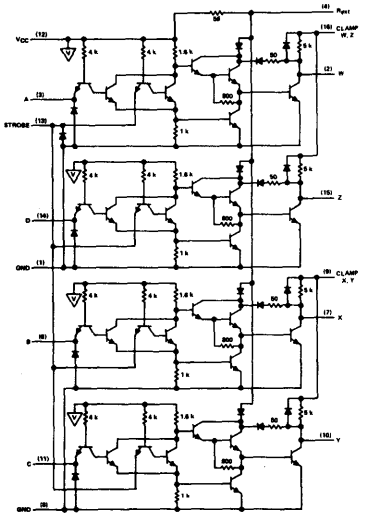


PINS 1 AND 8 OF J AND N PACKAGES ARE IN ELECTRICAL CONTACT WITH THE METAL BASE

5

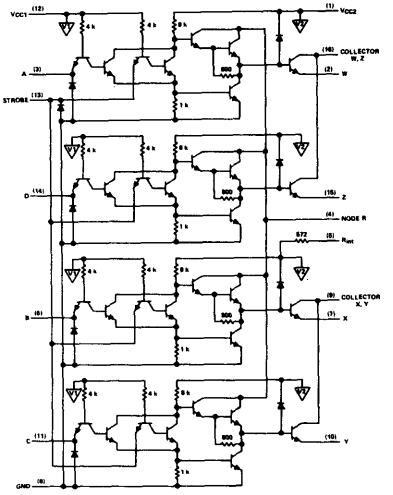
SCHEMATICS

SG55326, SG75326



▽ ▽ ▽ . . . V_{CC}, V_{CC1}, or V_{CC2} bus, respectively.

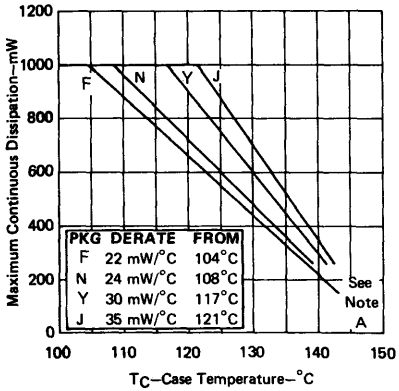
SG55327, SG75327



Resistor values shown are nominal and in ohms.

THERMAL INFORMATION

CASE TEMPERATURE
DISSIPATION DERATING CURVE



NOTE A: Rated operating free-air temperature ranges must be observed regardless of heat-sinking.

FIGURE 1

FREE-AIR TEMPERATURE
DISSIPATION DERATING CURVE

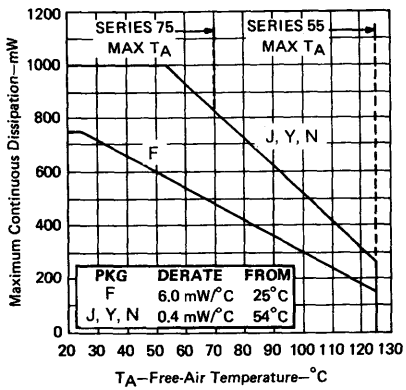
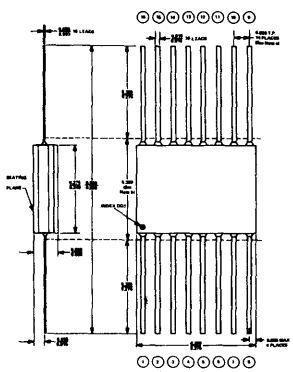
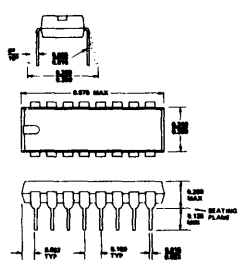


FIGURE 2

PACKAGES



F-FLAT PACKAGE
16-PIN CERAMIC



N-PACKAGE
16-PIN PLASTIC

J-PACKAGE
16-PIN CERDIP

Dual Peripheral Drivers

The SG55450B and SG55460 Series are general purpose dual peripheral drivers whose output stage includes a completely uncommitted, high-voltage, high current NPN transistor. Inputs to the standard TTL gates are diode clamped and fully DTL/TTL compatible. The output transistors of the SG55450B and SG75450B are capable of sinking 300 mA and will withstand 30 volts when off. The SG55460 and SG75460 devices have the same current rating but with higher voltage capability of 40 volts and only slight reduction in switching speeds.

The SG55450B and SG55460 are characterized for operation over the full military temperature range of -55°C to +125°C while the SG75450B and SG75460 are designed for 0°C to +70°C operation.

- **Current capacity of 300 mA per driver**
- **High output voltage capability**
- **High-speed switching characteristics**
- **Both military and commercial temperature ranges**

ABSOLUTE MAXIMUM RATINGS (Note 1)	SG55450B SG75450B	SG55460 SG75460
Supply Voltage, V_{CC}	7V	7V
Input Voltage	5.5V	5.5V
V_{CC} to Substrate Voltage	35V	40V
Collector to Substrate Voltage	35V	40V
Collector to Base Voltage	35V	40V
Collector to Emitter Voltage (Note 2)	30V	40V
Emitter to Base Voltage	5V	5V
Collector Current (Note 3)	300mA	300mA
Power Dissipation		
N Package (plastic)	600mW	600mW
Derate above 25°C	6.0mW/°C	6.0mW/°C
J Package (cerdip)	1000mW	1000mW
Derate above 25°C	6.7mW/°C	6.7mW/°C
Operating, Free Air Temperature Range		
SG55450B, SG55460	−55°C to +125°C	
SG754508, SG75460	0°C to +70°C	
Storage Temperature Range	−65°C to +150°C	

NOTES:
1. Voltage values shown are with respect to ground terminal unless otherwise specified.
2. With base-to-emitter resistance less than 500Ω.
3. Both sides of circuit may conduct rated current simultaneously provided power dissipation rating is not exceeded.

ELECTRICAL CHARACTERISTICS

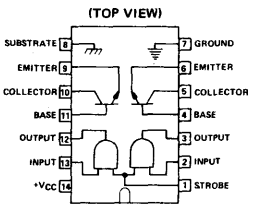
(over operating temperature range and with V_{CC} = 5V ± 5%, unless otherwise specified)

TTL GATES

Parameter	Test Conditions	Min.	Typ.	Max.	Units
High-level input voltage, V_{IH}	V_{OL} < 0.4V, I_{OL} = 16mA	2	—	—	V
Low-level input voltage, V_{IL}	V_{OH} > 2.4V, I_{OH} = −.4mA	—	—	0.8	V
High-level output voltage, V_{OH}	V_{IL} = 0.8V, I_{OH} = −.4mA	2.4	3.3	—	V
Low-level output voltage, V_{OL}	V_{IH} = 2.0V, I_{OL} = 16 mA	—	.25	0.4	V
Input clamp voltage, V_I	I_I = −12mA	—	−1.2	−1.5	V
High-level input current, I_{IH}	V_I = 2.4V	—	—	40	μA
High-level strobe current, I_{SH}	V_I = 2.4V	—	—	80	μA
Low-level input current, I_{IL}	V_I = 0.4V	—	—	−1.6	mA
Low-level strobe current, I_{SL}	V_I = 0.4V	—	—	−3.2	mA
Input current at max. V, I_I	V_I = 5.5V	—	—	1.0	mA
Strobe current at max. V, I_S	V_S = 5.5V	—	—	2.0	mA
Output short circuit current, I_{OS}		−18	−35	−55	mA
Supply current, high out, I_{CCH}	V_I = 0	—	2	4	mA
Supply current, low out, I_{CCL}	V_I = 5V	—	6	11	mA

OUTPUT TRANSISTORS (High current measurements made with pulse techniques)

Parameter	Test Conditions	55450B	75450B	55460	75460	Units
Collector-base breakdown BV_{CBO}	I_C = 100μA, I_E = 0	35	35	40	40	V min.
Collector-emitter breakdown BV_{CER}	I_C = 100μA, R_{BE} = 500Ω	30	30	40	40	V min.
Emitter-base breakdown BV_{EBO}	I_E = 100μA, I_C = 0	5	5	5	5	V min.
Base-emitter voltage V_{BE}	I_B = 10mA, I_C = 100 mA	1.2	1.0	1.2	1.0	V max.
	I_B = 30mA, I_C = 300mA	1.4	1.2	1.4	1.2	V max.
Collector-emitter saturation $V_{CE\ (SAT)}$	I_B = 10mA, I_C = 100mA	.5	.4	.5	.4	V max.
	I_B = 30mA, I_C = 300mA	.8	.7	.8	.7	V max.
Current transfer ratio h_{FE}	V_{CE} = 3V, I_C = 100mA, T_A = 25°C	25	25	25	25	min.
	V_{CE} = 3V, I_C = 300mA, T_A = 25°C	30	30	30	30	min.
	V_{CE} = 3V, I_C = 100mA, T_A = min.	10	20	10	20	min.
	V_{CE} = 3V, I_C = 300 mA, T_A = min.	15	25	15	25	min.

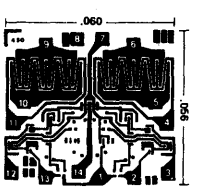


CONNECTION DIAGRAM

Note: The substrate (pin 8) must always be at the most negative voltage for proper device operation.

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_A = 25°C)

Parameter	Test Conditions	55450B, 75450B Typ.	55450B, 75450B Max.	55460, 75460 Typ.	55460, 75460 Max.	Units
TTL GATES						
Propagation delay time Low-to-high-level output, t_{PLH}	C_L = 15 pF	12	22	22	—	nS
Propagation delay time High-to-low-level output, t_{PHL}	R_1 = 400Ω	8	15	8	—	nS
OUTPUT TRANSISTORS						
Delay time, t_d	I_C = 200mA	8	15	10	—	nS
Rise time, t_r	$I_{b(1)}$ = 20mA	12	20	16	—	nS
	$I_{b(2)}$ = −40mA					
Storage time, t_s	$V_{BE(OH)}$ = −1V	7	15	23	—	nS
Fall time, t_f	C_L = 15 pF, R_L = 50Ω	6	15	14	—	nS
GATES & TRANSISTORS COMBINED						
Propagation delay time Low-to-high-level out, t_{PLH}	I_C = 200mA	20	30	45	65	nS
High-to-low-level out, t_{PHL}	C_L = 15 pF	20	30	35	50	nS
Transition time Low-to-high-level out, t_{TLH}	R_L = 50Ω	7	12	10	20	nS
High-to-low-level out, t_{THL}		9	15	10	20	nS



CHIP BONDING DIAGRAM

DISK DRIVE INTERFACE

DESCRIPTION:

The SG82727 is a monolithic integrated circuit designed to interface the standard disk drive bus to the actuator stepping motor, read/write circuitry and a microprocessor. A full featured 5¼ inch disk drive can be implemented with only three devices: the SG82727, an integrated read/write circuit and a microprocessor.

The SG82727 is designed for direct interface to the 8048 or 8049 microcontroller. The device can also be addressed by 8051, 6500/1, 6805 and similar microcontrollers with some external circuitry.

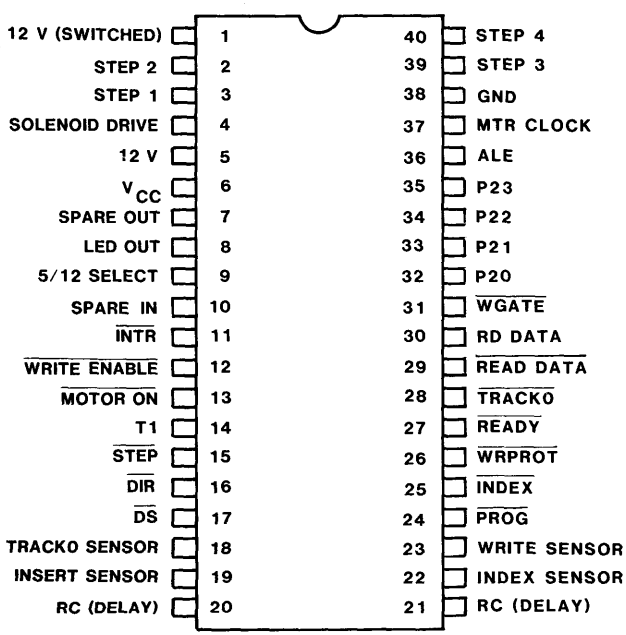
No external components are required between the host cable and the SG82727 (a single resistor packet may be required to pull up inputs in one drive per system). Internally clamped stepping motor outputs can sink and source 275 mA and the door latch solenoid driver can source 250 mA. The SG82727 supports direct interface to optical sensors. All other inputs are TTL compatible.

FEATURES:

- Direct drive of stepping motor (bipolar, 275 mA)
- Direct drive of door lock solenoid (250 mA)
- Direct Drive of LED activate indicator
- Direct interface to host disk drive bus
- Power saving feature for door lock
- 300 Hz output for spindle motor control
- Direct interface to microprocessor
- Two internal one-shots to shape index pulse
- TTL compatible logic input and outputs
- Packaged in a 40 pin DIP

5

CONNECTION DIAGRAM
(Top View)



FUNCTION

1. 12 Volt Input, Switched — Power to the stepping motor drivers. May be switched to 5 volts through an external transistor to save power. The output signal to select 5 or 12 volts is supplied at pin 9 (5/12 select).
2. Step Output 2 — Pins 2, 3, 39 and 40 are 275 mA push-pull drivers which can directly control the actuator arm stepping motor. These outputs have internal clamping diodes.
3. Step Output 1 — See pin 2.
4. Door Solenoid Driver Output — The output can source 250 mA. It is intended to drive a door lock solenoid.
5. 12 Volt Input — Power for the door lock solenoid driver.
6. 5 Volt Input (V_{CC}) — Power to the SG82727 logic circuits.
7. Spare Output — This TTL compatible output is user definable. It is gated with DS' (Drive Select) and controlled by the microprocessor.
8. Activated LED Output Driver — Directly drives the activated LED.
9. 5/12 Select Output — This output can be used to control a power save feature. It should be connected, through a resistor, to the base of the external transistor which supplies power to pin 1.
10. Spare Input — This TTL compatible input is user definable. The signal is inverted when read by the microprocessor.
11. INTR' Output — TTL compatible interrupt signal to the microprocessor. An INTR' is generated for each STEP' input. The signal may be masked by the microprocessor.
12. WRITE ENABLE' Input — Write enable input from the host system.
13. MOTOR ON' Input — Motor on input from the host system.
14. T1 Output — This TTL compatible output is toggled every other STEP' input.
15. STEP' Input — Step input from the host system.
16. DIR' Input — Direction input from the host system.
17. DS' Input — Drive select input from the host system.
18. Track 0 Sensor Input — Direct interface for optical sensor. This input has a minimum of 200 mV input hysterisis and 22K input resistance.
19. Insert Sensor Input — Direct interface for optical sensor. This input has a minimum of 200 mV input hysteristis and 22K input resistance.
20. RC Control — An external resistor and capacitor adjust the time out of an internal one-shot to control the index to data delay.
21. RC Control — An external resistor and capacitor adjust the time out of an internal one-shot to control the width of the index pulse.
22. Index Sensor Input — Direct interface for optical sensor. This input has a minimum of 200 mV input hysterisis and 22K input resistance.
23. Write Protect Sensor Input — Direct interface for optical sensor. This input has a minimum of 200 mV input hysterisis and 22K input resistance.
24. PROG Input — The negative transition of this TTL compatible input strobes commands to the SG82727 from the microprocessor; data are passed between the microprocessor and the SG82727 on the positive transition. This signal is directly compatible with the PROG output of an 8048 or 8049.
25. INDEX' — This TTL compatible output provides the index pulse to the read/write circuit. It is gated with DS' (drive select).
26. WRPROT' Output — Write protect output to the host system. Gated by DS' (drive select).
27. READY' Output — Ready output to the host system. Gated by DS' (drive select).
28. TRACK0' Output — Track 0 output to the host system. Gated by DS' (drive select).
29. READ DATA' Output — Read data output to the host system. Gated by DS' (drive select).

30 RD DATA Input — A TTL compatible input from the read/write circuit. This signal is the data from the disk. The SG82727 gates the data with DS' (drive select) and makes it available to the host system on pin 29.

31 WGATE' Output — This is a TTL compatible output to the read/write circuit. It is gated by WRITE ENABLE' (pin 12), DS' (drive select) and the input from the write protect sensor. It can be enabled by the microprocessor.

32 P20 — P20, P21, P22 and P23 form a 4 bit TTL compatible interface to the microprocessor. They are directly compatible with the lower 4 bits of port 2 of an 8048 or 8049.

33 P21 — See pin 32.

34 P22 — See pin 32.

35 P23 — See pin 32.

36 ALE Clock Input — A TTL compatible input used in conjunction with MTR clock output to generate a 300 Hz signal to control the speed of the spindle motor. The ALE clock of an 8048 or 8049 running at a 4.608 MHz clock rate may be input to this pin. The SG82727 will function without this input if spindle motor timing is generated from some other source.

37 MTR Clock Output — TTL compatible output. See pin 36.

38 Ground — Drive and device common.

39 Step Output 3 — See pin 2.

40 Step Output 4 — See pin 2.

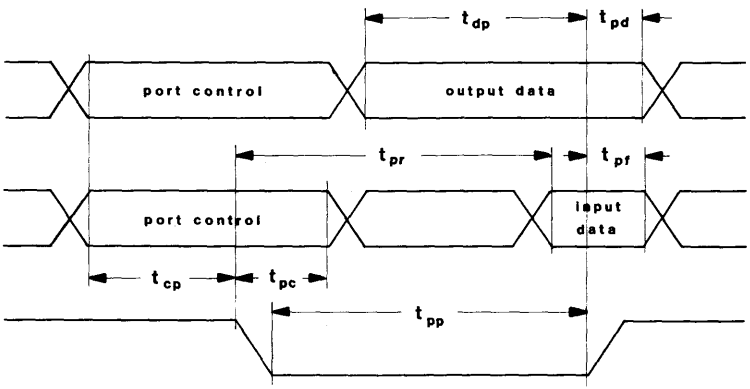
COMMAND	8048 PORT	DIRECTION	FUNCTION BITS 0	1	2	3
1	5	Read	Track Sensor	Write Prot. Sensor	Index Sensor F/F	Spare In.
2	6	Read	DIR	MOTOR ON	WENABLE	DS
3	7	Read	Insert Sensor	—	—	—
4	4	Write	STEPPING MOTOR BIT PATTERN			
5	5	Write	Preset INT	Clock INT	Act LED	12/5 Select
6	6	Write	Reset Index Sensor F/F	READY	TRACK 0	Enable WGATE
7	7	Write	5/12 Enable	Door Lock Solenoid	Spare Output	—

NOTE: 8048 instructions MOVD P,A and MOVD A,P select the SG82727. ORLD and ANLD instructions are ignored. P defines the 8048 port. A is the accumulator. Other microprocessors should send the appropiate command to the SG82727 as the PROG input is strobed.

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
Output High Voltage (WGATE', MTR Clock, INTR', T1	V_{OH}	$I_{OH} = -400\mu A$	3.5			Volts
Output Low Voltage	V_{OL}	$I_{OL} = 4$ mA			.4	Volts
High Level Output Current (INDEX', WR PROT', READY' TRACKO', READ DATA', SPARE ACLED, 5/12 Select)	I_{OH}	$V_{OH} = 5V$			250	μA
Low Level Output Current	I_{OL}		48			mA
Low Level Output Voltage	V_{OL}	$I_{OL} = 48$ mA			.4	Volts
Output High Voltage (P20 — P23)	V_{OH}	$I_{OH} = 400\ \mu A$	2.4			Volts
Output Low Voltage	V_{OL}	$I_{OL} = 1.6$ mA			.45	Volts
Positive Going Threshold (DIR', STEP', DS', WENABLE', MOTOR ON', SPARE)	V_T+		1.2	1.6	1.9	Volts
Negative Going Threshold	V_T-		0.5	0.8	1.0	Volts
Input High Current	I_{IN}	$V_I = 2.7V$			20	μA
Input Low Current	I_{IL}	$V_I = .4V$			−400	μA
Input High Voltage (ALE, PROG)	V_{IH}		2			Volts
Input Low Voltage	V_{IL}				0.8	Volts
High Level Input Current	I_{IH}	$V_I = 2.7V$			20	μA
Low Level Input Current	I_{IL}	$V_I = .4V$			−400	μA
Input High Voltage	V_{IH}		2			Volts
Input Low Voltage	V_{IL}				0.8	Volts
Input High Current	I_{IH}				−500	μA
Input Low Current	I_{IL}				400	μA
Comparator Positive Threshold (TRACKO SENSOR, WRITE PROT SENSOR, INDEX SENSOR, INSERT SENSOR)	V_T+		1.6		2.2	Volts
Comparator Negative Threshold	V_T-		1.1		1.7	Volts
Hystersis ($V_T+ - V_T-$)	V_{HYS}		200		600	mV
Input Resistance	R_{IN}		17.6		26.4	KΩ
Input Current	I_{IN}	$V_{IN} = 1.5V$		4		μA
Output Low Voltage (Step 1 — Step 4)	$V_{SATSINK}$	I = 275 mA			0.7	
Output High Voltage	$V_{SATSOURCE}$	I = 275 mA			$V_{12V}-1.8$	
Positive Clamp Voltage	V_D+	I = 275 mA			$V_{12V}+1.2$	
Negative Clamp Voltage	V_D-	I = 275 mA	−1.2			Volts
Output High Voltage 5 Volt Mode (Solenoid Driver)	V_{SAT5V}	I = 100 mA			$V_{5V}-2.6$	
Output High Voltage	V_{SAT12V}	I = 250 mA			$V_{12V}-3.6$	
Negative Clamp 12V Mode	V_D-	I = 250 mA	−1.2			Volts

AC CHARACTERISTICS

t_{PP}	PROG' Pulse Width	2.03 μS	Min.
t_{CP}	Port Control Setup to PROG'	355 nS	Min.
t_{PC}	Port Control Hold to PROG'	669 nS	Min.
t_{DP}	Output Data Setup	1.15 μS	Min.
t_{PD}	Output Data Hold	276 nS	Min.
t_{PF}	Input Data Hold from PROG'	326 nS	Min.
t_{PR}	PROG' to P2 Input Valid	1.84 μS	Max.



SG82727 Timing Diagram

APPLICATIONS

8048 or 8049 Interface

The SG82727 may be directly connected with an 8048 or 8049 microprocessor. The P21 to P24 pins should be connected to bits 1 through 4 of port 2. The PROG' pin on the SG82727 should be connected to the same pin on the 8048 or 8049. At a clock rate above 4.608 MHz the SG82727 must be controlled from a standard I/O port with an appropriate software driver.

8051 Interface

The SG82727 can be controlled from any I/O port on the 8051. The following software driver subroutine assumes that the lower 4 bits of port 2 are connected to P21 through P24 and that bit 4 of port 2 is connected to the PROG' input of the SG82727. To call this driver the A register must contain the command and the R0 register the data for a write command. After execution the A register will have the data on both a read and a write.

```
DRIVER ORL  A,10H
       MOV  P2,A          ;OUTPUT COMMAND
       CLR  P2,4          ;SET PROG' LOW
       JB   ACC.2,WRITE   ;IF BIT 2=1
                          ;WRITE,ELSE READ
READ   ORL  P2,0FH        ;SET P2 FOR INPUT
       MOV  A,P2          ;READ DATA
       SETB P2,4          ;SET PROG' HIGH
            RET
WRITE  MOV  A,R0          ;PLACE DATA IN ACC
       ANL  A,0FH         ;KEEP PROG'LOW
       MOV  P2,A          ;WRITE DATA
       SETB P2,4          ;SET PROG' HIGH
       RET
```

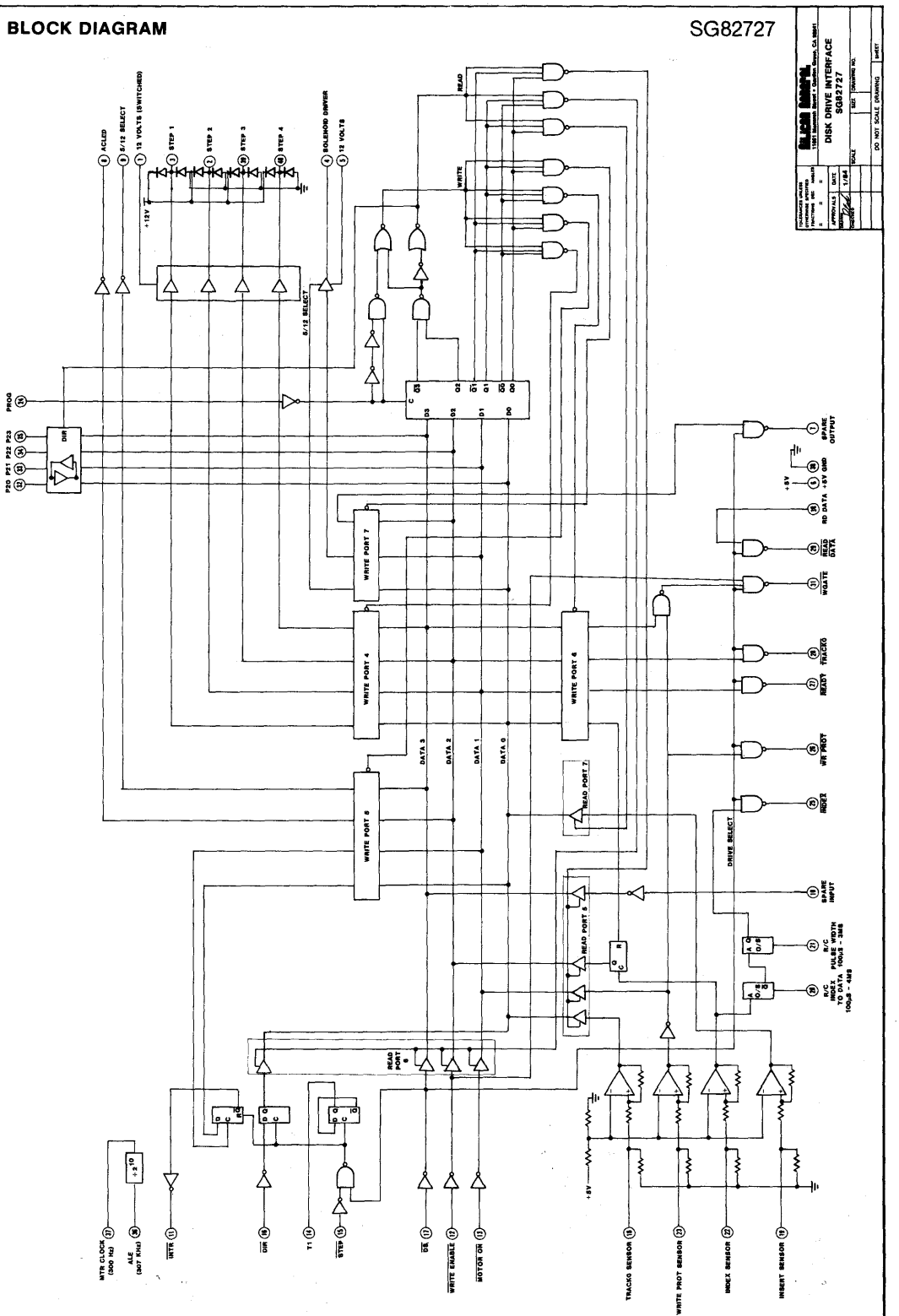
6500/1 Interface

The SG82727 can be controlled from any I/O port on the 6500/1. The following software driver subroutine assumes that the lower 4 bits of any port are connected to P21 through P24 and that bit 7 of that port is connected to the PROG' input of the SG82727. To call this driver the A register must contain the command and the X register the data for a write command. After execution the A register will have the data on both a read and a write.

```
DRIVER ORA  #$80
       STA  PORT          ;WRITE COMMAND TO
                          PORT
       AND  #$0F          ;STROBE PROG' AND
                          ;WRITE COMMAND
       STA  PORT
       CMP  #$04          ;IF BIT 4 READ, ELSE
                          ;WRITE
       BMI  READ          ;GO READ
WRITE  TXA                ;GET DATA IN A
       STA  PORT          ;WRITE DATA TO
                          ;PORT
OUT    ORA  #$80          ;SET PROG' HIGH
       STA  PORT
       AND  #$0F          ;CLEAN UP DATA
       RTS
READ   LDA  #$0F          ;SET BITS 0-3 FOR
                          ;INPUT
       STA  PORT
       LDA  PORT          ;GET DATA
       BPL  OUT           ;NOTE: BIT 7 IS A 0
```

BLOCK DIAGRAM

SG82727



POWER DRIVERS

High Current Output Drivers
Switch Drivers
Half Bridge Drivers
Dual H Bridge
Power Drivers
Quad Darlington Drivers
Motor Control Circuits
Quad Drivers

ADVANCED DATA
SG293D

Performance data described herein represent design goals.
Final device specifications are subject to change.

QUAD BI-POLAR DRIVER

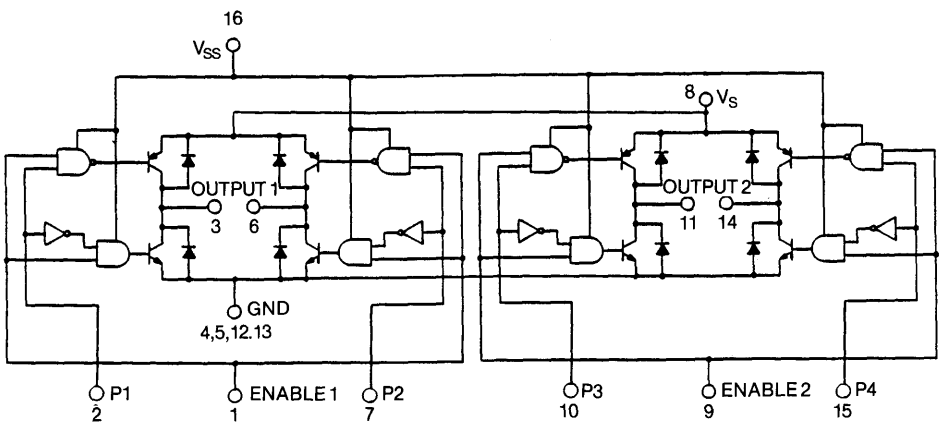
DESCRIPTION

The SG293D is a four channel high current high voltage bi-polar driver. It is designed to provide a dual H bridge interface between most standard logic families and fractional horsepower motor coils. The circuit has built in thermal protection and clamp diodes for inductive load suppression.

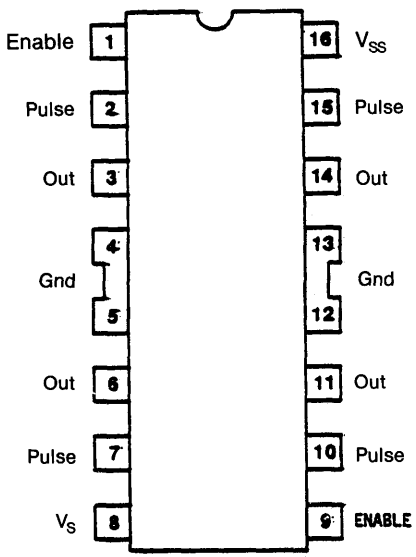
FEATURES

- **2 Full H bridges with clamp diodes**
- **Current source and sink to 1.5 amps peak**
- **40 Volts operation**
- **Thermal protection**
- **Chip enable**
- **16 Pin dip package**

LOGIC DIAGRAM



CONNECTION DIAGRAM



TRUTH TABLE

ENABLE	V_P	OUTPUT
0	0	Off
0	0	Off
1	0	0 (sink)
1	1	1 (source)

ABSOLUTE MAXIMUM RATINGS

V_S = 40 Volts V_{SS} = 40 Volts
I_{OUT} = 1.5 Amps V_{IN} = 15 Volts

ELECTRICAL CHARACTERISTICS (each channel)

V_S = 24 Volts, V_{SS} = 5 Volts

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_{SS} Supply Current	I_{SS}				15	mA
V_S Supply Current	I_S	I_O = 0			6	mA
"0" Input Current	I_{IN} (0)	Inputs = Gnd			100	μA
"1" Input Current	I_{IN} (1)	Inputs = 5.0V			10	μA
"0" Input Voltage	V_I (0)				0.8	Volt
"1" Input Voltage	V_I (1)		2.0			Volt
V_{CE} (Sat) Source	V_{OUT} (H)	I_{SOURCE} = 1.0 Amp			1.8	Volt
V_{CE} (Sat) Sink	V_{OUT} (L)	I_{SINK} = 1.0 Amp			1.8	Volt
Diode Forward Voltage	V_F	I_F = 1.0 Amp			1.8	Volt

ADVANCED DATA
SG298D

Performance data described herein represent design goals.
Final device specifications are subject to change.

QUAD BI-POLAR DRIVER

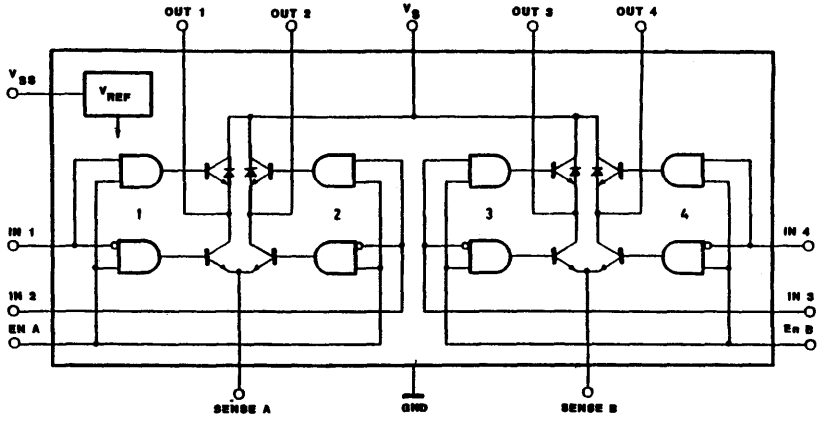
DESCRIPTION

The SG298D is a four channel high current high voltage bi-polar driver. It is designed to provide a dual H bridge interface between most standard logic families and fractional horsepower motor coils. The circuit has built in thermal protection and clamp diodes for inductive load suppression.

FEATURES

- **2 Full H bridges with clamp diodes**
- **Current source and sink to 2.5 amps peak**
- **46 Volts operation**
- **Thermal protection**
- **Chip enable**
- **15 sip package**

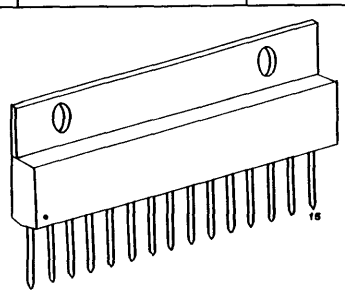
LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS (for each channel V_S = 42 V, V_{SS} = 5 V, T_J = 25°C)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_S	Supply Voltage	Operative condition		V_{IN} + 2.5		46	V
V_{SS}	Logic Supply Voltage			4.5		7	V
I_S	Quiescent Supply Current	V_{inh} = H	V_I = L		3	5	mA
		I_L = 0	V_I = H		15	20	
		V_{inh} = L				1	
I_{SS}	Quiescent Current from V_{SS}	V_{inh} = H	V_I = L		5	8	mA
		I_L = 0	V_I = H		1.5	2	
		V_{inh} = L			1	1.5	
V_I L	Input Low Voltage			− 0.3		1.5	V
V_I H	Input High Voltage			2.3		V_{SS}	
I_I L	Low Voltage Input Current	V_I = L				− 10	μA
I_I H	High Voltage Input Current	V_I = H			30	100	
V_{inh} L	Inhibit Low Voltage			− 0.3		1.5	V
V_{inh} H	Inhibit High Voltage			2.3		7	
I_{inh} L	Low Voltage Inhibit Current	V_{inh} = L				− 10	μA
I_{inh} H	High Voltage Inhibit Current	V_{inh} H = ≤ V_{SS} − .06V			30	100	
$V_{CE\ sat\ (H)}$	Source Saturation Voltage	I_L = 1A			1.2	1.6	V
		I_L = 2A			1.8	2.6	
$V_{CE\ sat\ (L)}$	Sink Saturation Voltage	I_L = 1A			1.2	1.6	V
		I_L = 2A			1.7	2.4	
$V_{CE\ sat}$	Total Drop	I_L = 1A				3.2	V
		I_L = 2A				4.8	
V_{SENS}	Sensing Voltage			− 1		2	V
T_1 (V_I)	Source Current Turn Off Delay	0.5 V_I to 0.9 I_L			1.7		μS
T_2 (V_I)	Source Current Fall Time	0.9 I_L to 0.1 I_L			0.2		μS
T_3 (V_I)	Source Current Turn On Delay	0.5 V_I to 0.1 I_L			2.5		μS

PACKAGE



DUAL HIGH-CURRENT OUTPUT DRIVER

DESCRIPTION

The SG1627 series devices are monolithic, high-speed driver integrated circuits designed to interface digital control logic with high current loads. Each device contains two independent drivers which will either source or sink up to 500 mA of current. The sink transistor is designed as a saturating switch while the source transistor can be used either as a switch or as a constant current generator with external resistor programming.

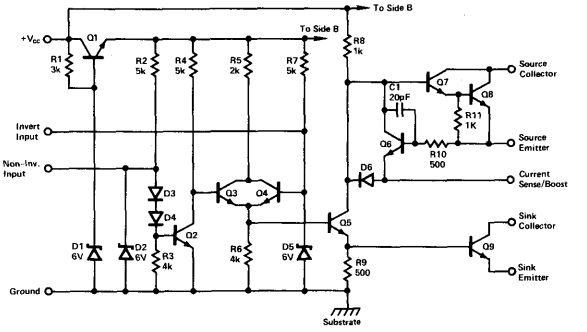
Each half of this device contains both inverting and non-inverting inputs which have two volt thresholds for high noise immunity. Either input can be used alone to switch the output, or one input can be strobed with the other. These units have been designed to directly interface with the SG1524 Regulating Pulse Width Modulator Circuit.

These devices are supplied in ceramic 16-pin D.I.L. packages. The SG1627 is specified for operation over a −55°C to +125°C temperature range while the SG2627 and SG3627 are intended for industrial applications of 0°C to +100°C.

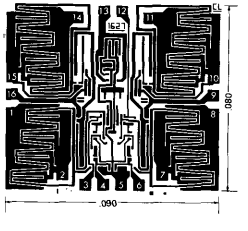
FEATURES

- **Two independent driver circuits**
- **Outputs will source or sink currents to 500 mA**
- **100 nSec response time**
- **Full compatibility with SG1524 PWM circuit**
- **Constant current drive capability**
- **Two volt threshold for high noise immunity**
- **Source and sink can be separated for complementary outputs**

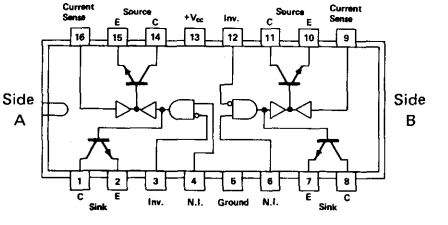
SCHEMATIC (one half of total device shown)



CHIP LAYOUT



CONNECTION DIAGRAM (TO—116 OUTLINE) (TOP VIEW)



ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} SG1627, 2627	30V
3627	20V
Output Collector Voltage SG1627, 2627	30V
SG3627	20V
Source or Sink Current, DC	500 mA
Peak Current (<2% duty cycle)	1A
Input Voltage	5.5V
Input Current	10 mA
Avg. Total Power Dissipation (Note 1)	1000 mW
Derate Above 50°C	10 mW/°C

Operating Junction Temperature Range	
SG1627	−55°C to +125°C
SG2627 & 3627	0°C to +100°C
Storage Temperature Range	−65° to +150°C

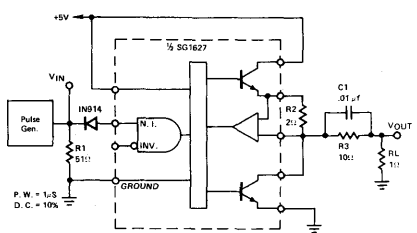
Note 1: Total power dissipation is the sum of the control logic power plus the power of each source and sink output transistor, factored duty cycle.

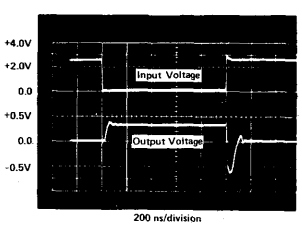
ELECTRICAL CHARACTERISTICS

Unless otherwise stated, these specifications apply for $T_J = -55°C$ for the SG1627 and 0°C to +100°C for the SG2627 and 3627. $V_{CC} = 5V$.

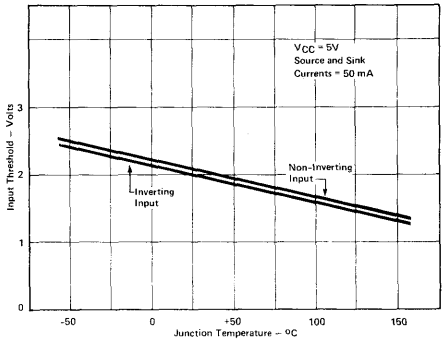
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
High-Level Input Voltage		2.8	–	5.5	Volts
Low-Level Input Voltage		0	–	1.4	Volts
Input Threshold		–	2.0	–	Volts
Low-Level Input Current	$V_I = 0$	–	-1.0	-2.0	mA
Source Off, Leakage Current	Collector V = V_{max}	–	0.3	1.0	mA
Source On, Collector Sat.	I_{source} = 50 mA	–	1.1	1.7	Volts
(Source Emitter Grounded,	I_{source} = 300 mA	–	1.2	1.9	Volts
$R_{SC} = 0$)	I_{source} = 500 mA	–	1.3		Volts
Source On, Emitter Voltage	I_{source} = -50 mA	(V_{CC}−3V)	–	–	Volts
Sink Off, Leakage Current	Collector V = V_{max}	–	1.0	100	μA
Sink On, Collector Sat.	I_{sink} = 50 mA	–	0.2	0.4	Volts
	I_{sink} = 300 mA, V_{CC} = 20V		0.5	0.7	Volts
	I_{sink} = 500 mA, I_{boost} = 25 mA		0.5		Volts
Current Limit Sense Voltage	$R_{SC} = 10\Omega$, $T_A = 25°C$	600	700	900	mV
Sense Voltage Temp. Coef.	$R_{SC} = 10\Omega$	–	1.8	–	mV/°C
Supply Current	V_{CC} = 5V		15	22	mA
(Both sink transistors on)	V_{CC} = 20V		50	73	mA
	V_{CC} = 30V (ex. 3627)		80	115	mA
Output Response, Turn On	Fig. 4, $R_L = 24\Omega$, $T_A = 25°C$	–	50	–	nS
Output Response, Turn Off	Fig. 4, $R_L = 24\Omega$, $T_A = 25°C$	–	100	–	nS
Thermal Resistance θ_{JA}		–	80	110	°C/W
Thermal Resistance θ_{JC}		–	45	60	°C/W

TOTEM POLE OUTPUT SWITCH CIRCUIT

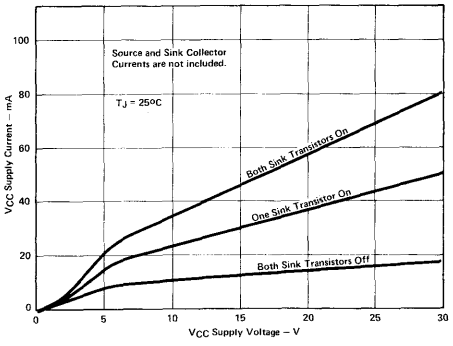




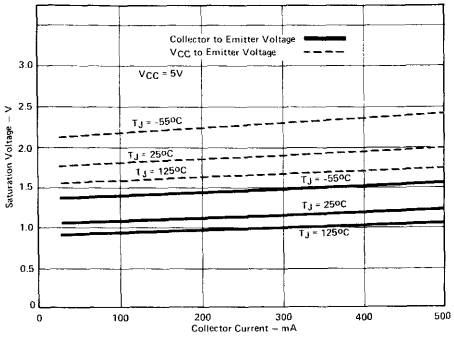
INPUT THRESHOLD vs. TEMPERATURE



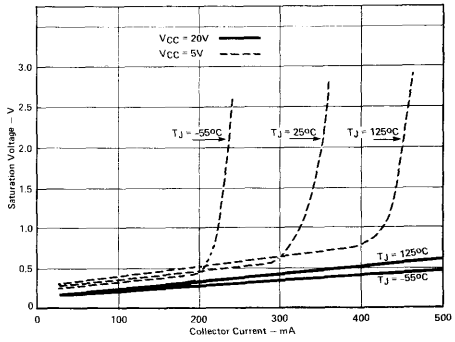
V_{CC} SUPPLY CURRENT vs. VOLTAGE



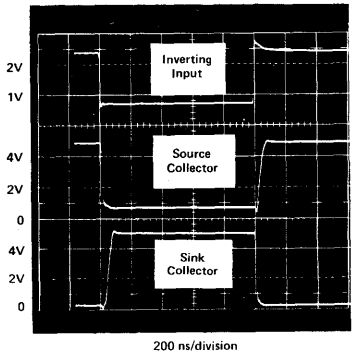
SOURCE TRANSISTOR SATURATION

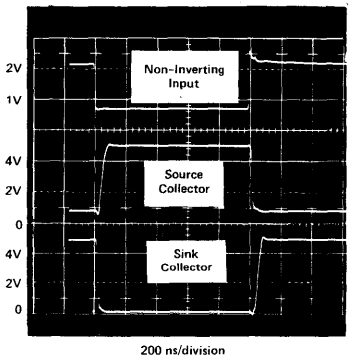


SINK TRANSISTOR SATURATION



DYNAMIC RESPONSE (See Figure 4 for Test Circuit, R_L = 24Ω)





APPLICATIONS

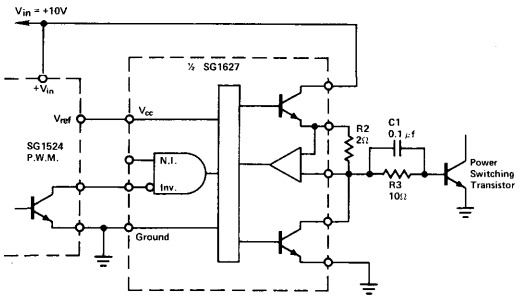


Figure 1. Basic 300 mA switched drive circuit. If the external output transistor is to be on when the driving transistor is on, use the inverting input with the non-inverting input left open. For opposite phasing, use the non-inverting input with the inverting input grounded.

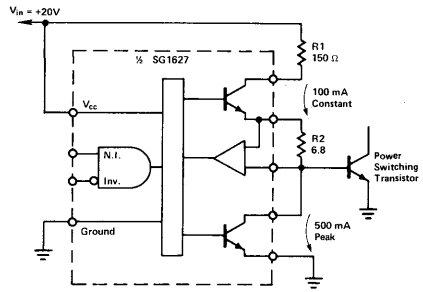


Figure 2. Use of higher input voltage provides greater drive for higher sink-transistor peak current while R2 provides constant source current. R1 helps minimize power in the SG1627. Although the sink emitter may be connected to a different ground point from pin 5, any voltage differences between them will directly affect the input threshold level.

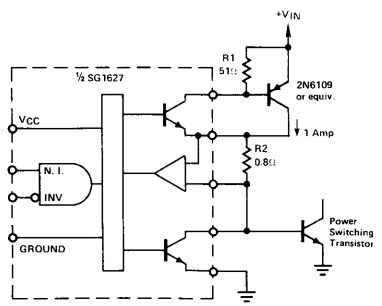


Figure 3. Additional source current or power handling capability may be added with the use of an external PNP transistor. For optimum performance, a low storage-time unit should be selected. If current limiting is not required, an NPN emitter follower could also be used for source boost.

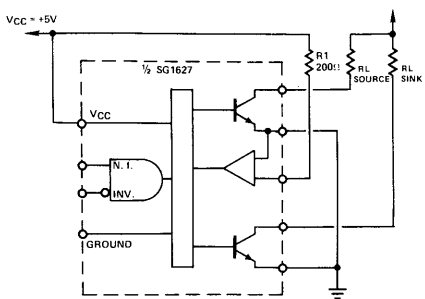


Figure 4. Source and sink transistors can be used separately for complementary outputs. At low supply voltages the sink current is limited to approximately 100mA, but if current limiting is not required sink drive boost may be added with R1. The current in R1 should be .05 times the sink load current to insure saturation.

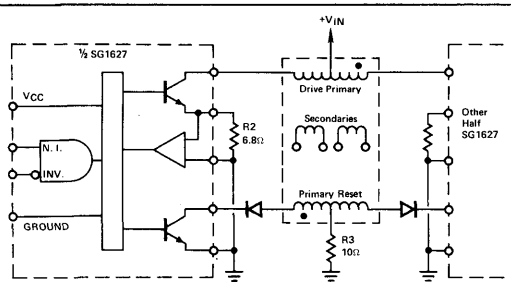


Figure 5. Source and sink transistors can be used separately for an efficient transformer driver. Here the source provides constant current drive with magnetic reset accomplished by a flux clamp utilizing the sink transistor. With the source current sense terminal connected to ground, there will be a residual collector current of approximately 300µA. If this is objectionable, insert a diode between current sense and ground.

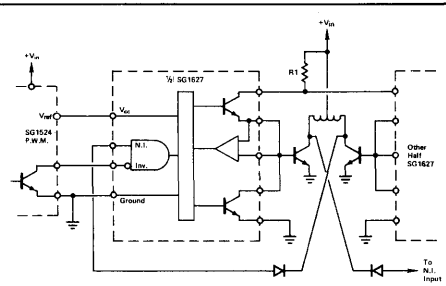


Figure 6. Simultaneous conduction of the output switching transistors can be positively prevented by using diodes to cross-couple a gating signal into the non-inverting inputs. For maximum power handling capability, the source transistor is driven into saturation with the current limiting provided by R1.

See Applications Notes for additional information.

Data subject to change without notice.

HIGH-CURRENT FLOATING SWITCH DRIVER

DESCRIPTION

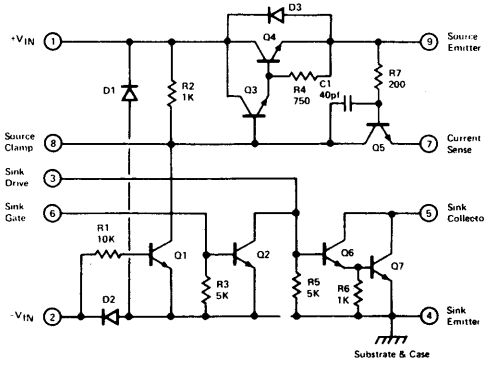
The SG1629 and SG3629 are monolithic integrated circuits designed to generate the positive and negative base drive currents (I_{b1} and I_{b2}) required for high-speed, high power switching transistors. These units are intended to interface between the secondary of a drive transformer and the base of an NPN switching device. Positive drive current can be made constant with an external programming resistor, or can be clamped with a diode to keep the switching device out of saturation. Negative turn-off current is derived from a negative voltage generated in an external capacitor. All operating power is supplied by the transformer secondary and these devices can be floated at high levels with respect to ground for off-line, bridge converters.

For medium power applications, these units are available in 10-pin, TO-100 package; while high power capability is offered in a 9-pin, TO-66 case. In either package , the SG1629 is specified for operation over an ambient temperature range of -55°C to +125°C while the SG3629 is intended for industrial applications of 0 to 70°C.

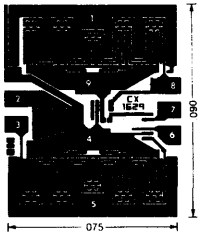
FEATURES

- **Self-generating positive and negative currents**
- **Constant source current (I_{b1}) to one amp**
- **Two amp peak sink current (I_{b2}) to negative voltage**
- **Floating operation**
- **Baker clamp input for non-saturated switching**
- **Provisions for source and sink gating**
- **100 nanosecond response**

SCHEMATIC



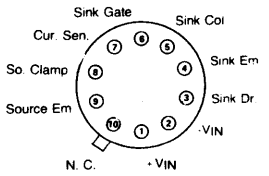
CHIP LAYOUT



CONNECTION DIAGRAMS

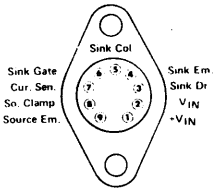
T-Package

TO-100



R-PACKAGE
TO-66

TOP VIEWS



Note: Case is internally connected to pin 4.

ABSOLUTE MAXIMUM RATINGS

Input Voltage + or - Inputs	20V
Collector to Emitter Voltage, Source or Sink	20V
Source Current	2.0 A
Sink Current	3.0 A
Sink Rectifier Current (peak)	2.0 A
Average Total Power Dissipation (Note 1)	
R-Package (TO-66)	3000 mW
Derate above 50°C	24 mW/°C
T-Package (TO-100)	680 mW
Derate above 50°C	5.4 mW/°C

Operating Junction Temperature Range	
SG1629	-55°C to +150°C
SG3629	0°C to +125°C
Storage Temperature Range	-65°C to +175°C

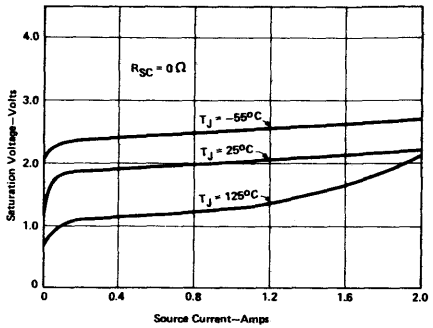
Note 1: Total power dissipation must include the power in both source and sink transistors times the duty cycle for each.

ELECTRICAL CHARACTERISTICS

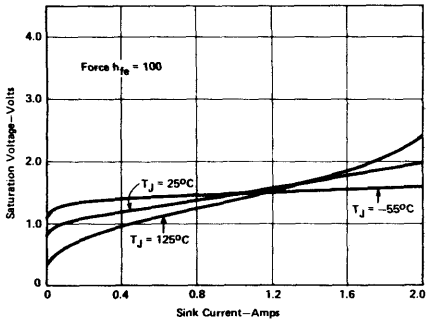
Unless otherwise stated, these specifications apply for T_J = –55°C to +150°C for the SG1629 and 0°C to 125°C for the SG3629.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Collector to Emitter Voltage Source or Sink	V_{BE} = 0		20	30	–	Volts
Collector to Emitter Leakage Source or Sink	V_{BE} = 0, V_{CE} = 15V		–	5	100	μA
Input Leakage V+ to V-	Input Voltage = +15V		–	1	100	μA
Input Leakage V- to V+	Input Voltage = -15V		–	2	4	mA
Standby Current from Sink Emitter Voltage	Sink Emitter = -5V 1kΩ from $-V_{IN}$ to Sink Drive Source Emitter Connected to Sink Collector $+V_{IN} = -V_{IN}$ = 0V		–	5	10	mA
Clamp Current	$+V_{IN}$ = 15V V clamp = 0V			15	20	mA
Source Saturation Voltage	I source = 100 mA (T-Package)		–	1.7	–	Volts
	I source = 500 mA (R-Package)		–	1.8	–	Volts
	I source = 1A T_J = 25°C		–	2.0	3	Volts
Sink Saturation Voltage Force beta = 100	I sink = 100 mA (T-Package)		–	1.2	–	Volts
	I sink = 500 mA (R-Package)		–	1.3	–	Volts
	I sink = 1A T_J = 25°C		–	1.5	2	Volts
Sink Current Gain	I sink = 2A, V_{CE} = 3V		300	500	–	
Current Limit Sense Voltage	R_{SC} = 0.7Ω T_J = 25°C		0.55	0.65	0.80	Volts
Sink Rectifier Forward Voltage	I_F = 1A T_J = 25°C		–	1.0	2.0	Volts
Sink Gate Output Saturation	Sink Drive = 10 mA Sink Gate Input Current = 1 mA		–	0.2	0.4	Volts
Source Response	I source = 1A		–	100	–	nS
Sink Response	I sink = 1A		–	100	–	nS
Thermal Resistance	R-Package	θJA	–	40	–	°C/W
		θJC	–	5	–	°C/W
	T-Package	θJA	–	150	–	°C/W
		θJA	–	25	–	°C/W

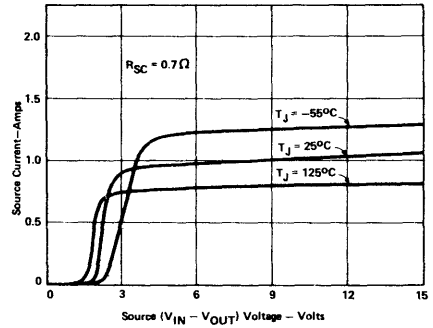
SOURCE SATURATION



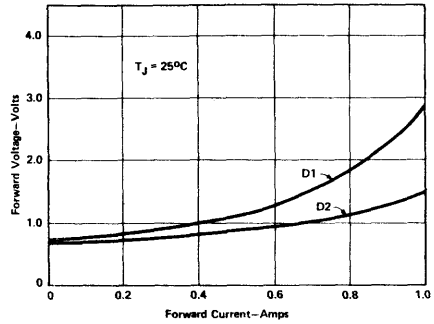
SINK SATURATION



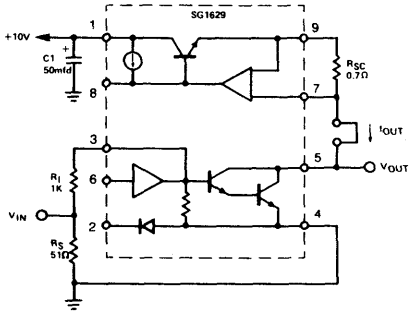
CONSTANT SOURCE CURRENT

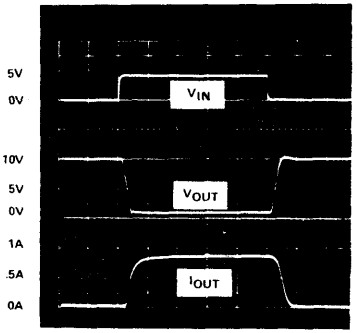


RECTIFIER FORWARD VOLTAGE



DYNAMIC RESPONSE





200 nS/Division

APPLICATIONS

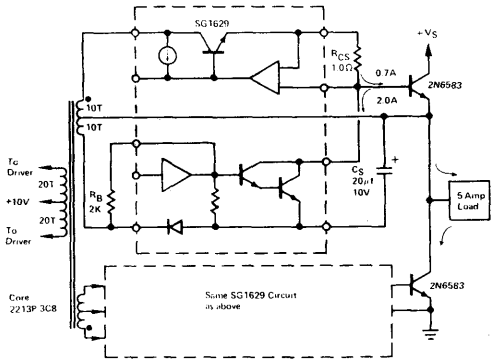


Figure 1. Two SG1629 devices can be combined to form the drive signals for the power transistors in a 5-amp, half-bridge switching supply.

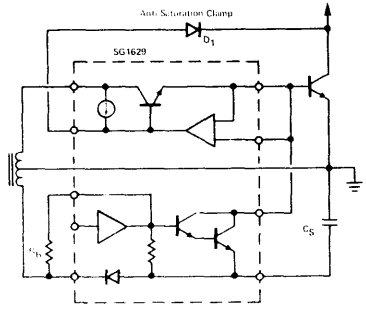


Figure 2. A load-dependent drive current may be provided by eliminating the current sensing resistor and adding the anti-saturation clamp diode D1.

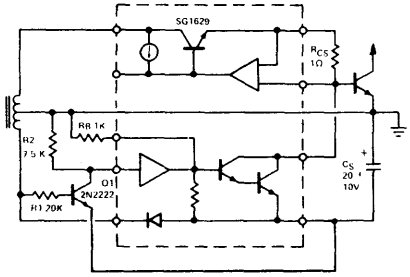


Figure 3. Where transformer inductance would normally degrade turn-on current rise time, the use of the sink gate with a relatively slow external transistor, Q1, will delay the sink turn-off until after source current has been established.

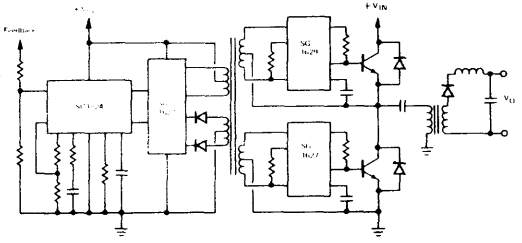


Figure 4. A simplified drive system for a half-bridge switched mode converter. A full bridge drive may be accommodated with four SG1629 drivers and additional current boosting for the SG1627.

TWO-AMP, HALF-BRIDGE DRIVER

DESCRIPTION

The SG1635 and SG3635 are monolithic integrated circuits designed to interface low-level, logic signals with high-current, inductive or capacitive loads. These devices are particularly adept at high speed pulse width modulation for motor drives or Class D audio amplifiers, and when used in pairs, they can provide full bridge drive for bi-directional control.

With TTL compatible inputs, these devices will either source or sink up to 5 amps of peak current with interlock protection to insure that source and sink cannot be on simultaneously. Additional protection is provided by thermal shutdown of the source output if the chip temperature rises above 160°C. High speed internal commutating diodes are also included.

FEATURES

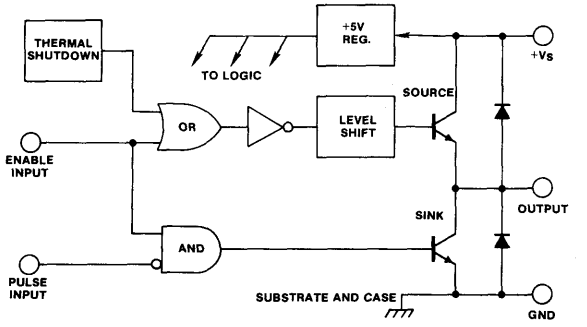
- **Source or sink five amps peak**
- **100 nanosecond response**
- **Half-bridge with internal diodes**
- **TTL input compatibility**
- **Either dual or tri-state output**
- **Direct PWM motor drive from microprocesser**
- **Built-in thermal protection**

TRUTH TABLE

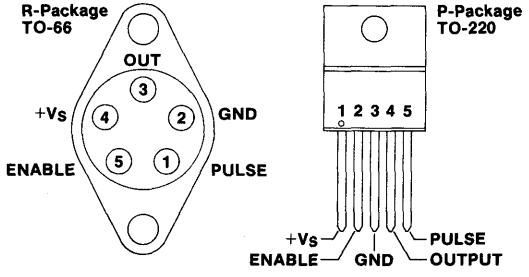
Enable	Pulse	Output
1	1	Off (High with no load)
0	1	High
1	0	Low
0	0	High

(1= open or high)

LOGIC DIAGRAM

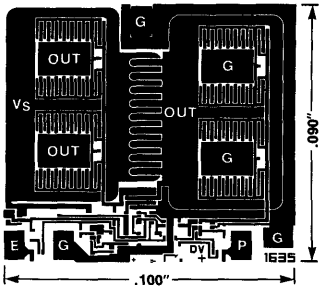


CONNECTION DIAGRAMS (Top Views)



Note: Case and mounting tab are internally connected to ground pin.

CHIP LAYOUT



ABSOLUTE MAXIMUM RATINGS

Input supply voltage,
SG1635/3635, V_S 35V
SG1635A/3635A, V_S 40V
Peak output current 5A
Continuous output current 2A
Peak diode current 5A

Operating junction temperature range
SG1635/1635A -55°C to +150°C
SG3635/3635A - 0°C to +125°C
Storage temperature range -65°C to +150°C

Average total power dissipation without heat sink (Note 1)
P-Package (TO-220) 2W
Derate above 50°C 20mW/°C
R-Package (TO-66) 3W
Derate above 50°C 30mW/°C

NOTE 1: Total power dissipation must include power in both source and sink plus diodes, with factors for duty cycle.

ELECTRICAL CHARACTERISTICS

Unless otherwise stated, VS = 24V VE = 2V, VP = 2V, and T_J = -55°C to +125°C for the SG1635 and 0°C to 70°C for the SG3635. Input limits apply to either Enable or Pulse inputs.

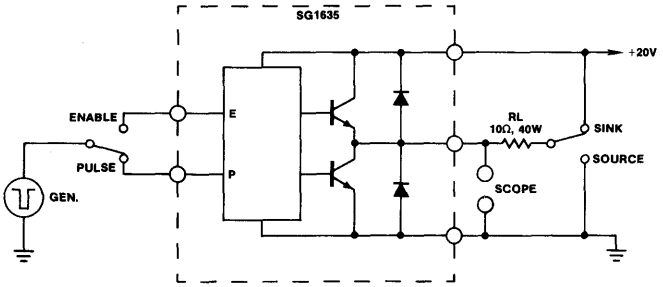
PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNITS
Input Voltage	I_{IN} = 0		1.0	1.8	2.5	V
Input High Current	V_{IN} = 4.5V		—	3	200	μA
Input Low Current	V_{IN} = OV		—	−1	−3.2	mA
Input Threshold			0.8	1.2	2.0	V
Output High Leakage	V_O = 24V		—	1.0	500	μA
Output Low Leakage	V_O = OV		—	20	40	mA
Source Saturation $V_S - V_{OH}$	V_E = 0.8V, I_0 = −100mA		—	1.4	2	V
	V_E = 0.8V, I_0 = −2A		—	2.0	3	V
Sink Saturation V_{OL}	VP = 0.8V, I_0 = 100mA		—	0.8	2	V
	V_P = 0.3V, I_0 = 2A		—	2.0	3	V
Source Diode Forward Voltage	I_D = 2A		—	2.2	3	V
Sink Diode Forward Voltage	I_D = 2A		—	1.8	3	V
Supply Current	SG1635A/3635A	V_S = 40V	—	10	25	mA
		V_{OH}, V_E = OV	—	10	25	mA
		V_{OL}, V_P = OV	—	27	70	mA
	SG SG1635/3635	V_S = 35V	—	10	25	mA
		V_{OH}, V_E = OV	—	10	25	mA
		V_{OL}, V_P = V	—	27	65	mA
Thermal Resistance	P-pkg	θ_{JA}	—	60	70	°C/W
		θ_{JC}	—	3.0	5.0	°C/W
	R-pkg	θ_{JA}	—	40	50	°C/W
		θ_{JC}	—	4.0	6.0	°C/W

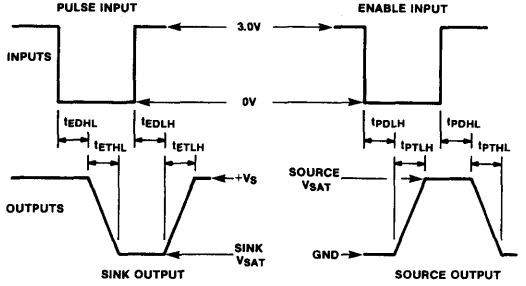
SWITCHING CHARACTERISTICS See test circuit, T_J = 25°C.

PARAMETER	TEST CONDITION			MIN.	TYP.	MAX.	UNITS
Pulse Switching Characteristics	Turn on	Delay Time	t_{PDHL}	—	50	—	nSec
		Transition Time	t_{PTHL}	—	200	—	nSec
	Turn off	Delay Time	t_{PDLH}	—	100	—	nSec
		Transition Time	t_{PTLH}	—	100	—	nSec
Enable Switching Characteristics	Turn on	Delay Time	t_{EDLH}	—	200	—	nSec
		Transition Time	t_{ETLH}	—	100	—	nSec
	Turn off	Delay Time	t_{EDHL}	—	100	—	nSec
		Transition Time	t_{ETHL}	—	100	—	nSec

6

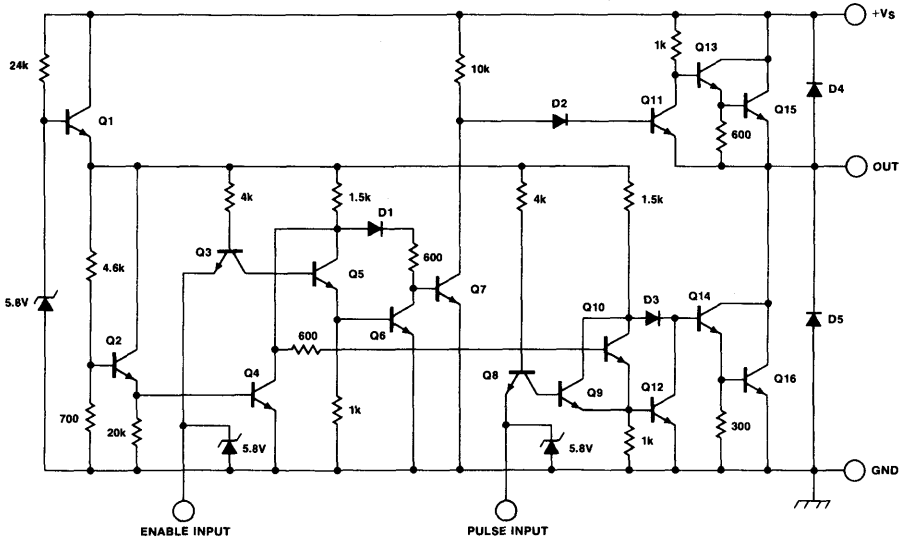
SWITCHING TEST CIRCUIT



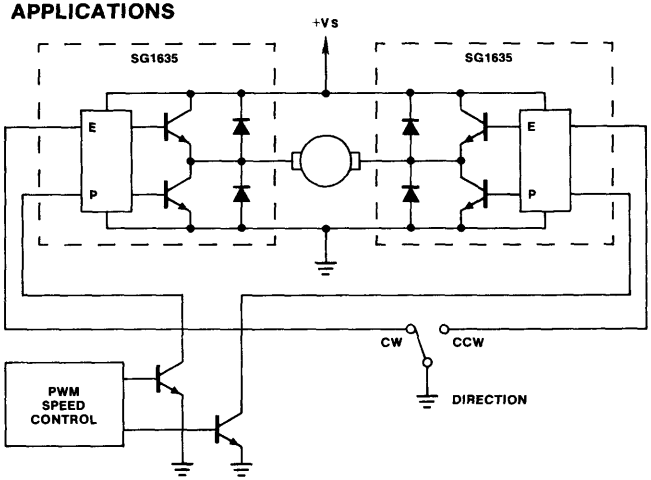


Notes:
A. Pulse Generator has: Width = 0.5 μSec, Rep. rate = 20kHz.
B. R_L must be non inductive for equivalent current waveforms.

SCHEMATIC



APPLICATIONS

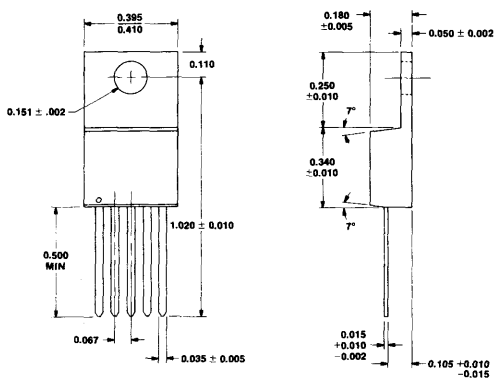


Typical Motor Drive Application

Two SG1635's form a full bridge motor drive circuit with the appropriate Enable Input determining motor direction and a PWM signal into the Pulse Inputs determining speed. Because of the internal Enable interlock, both Pulse Inputs may be connected together to a single-ended PWM signal.

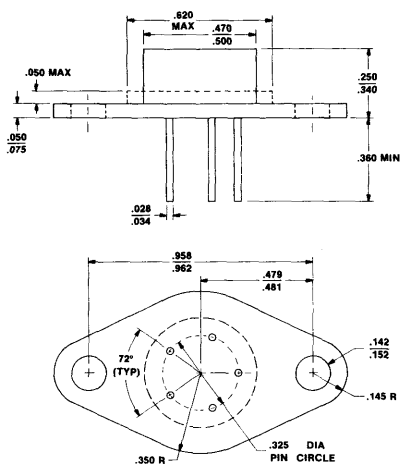
6

PACKAGE DIMENSIONS



P-Package TO-220

R-Package TO-66



HIGH VOLTAGE, HIGH CURRENT DRIVER ARRAYS

DESCRIPTION

These high voltage, medium current driver arrays are comprised of seven silicon NPN Darlington pairs on a common monolithic substrate. All units feature open collector outputs and integral suppression diodes for inductive loads. Peak inrush currents to 600 mA are allowable, making these devices ideal for driving tungsten filament lamps.

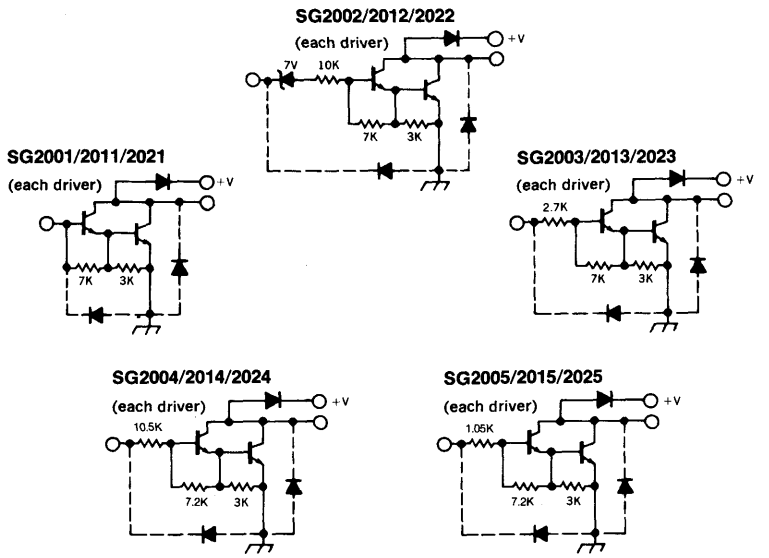
Five different input configurations provide optimized designs for interfacing with TTL, DTL, PMOS or CMOS drive signals.

In all cases, the individual Darlington pair collector current rating is 500 mA. However, outputs may be paralleled for higher load current capability. All devices are supplied in a 16-pin dual in-line ceramic package.

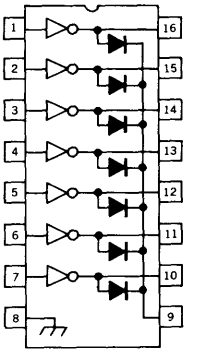
FEATURES

- **Collector currents to 600 mA**
- **Low saturation voltage**
- **High speed switching**
- **Closely matched parameters**
- **Plastic and hermetic packages**

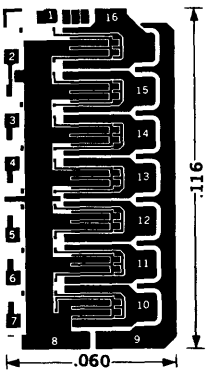
PARTIAL SCHEMATICS



CONNECTION DIAGRAM



CHIP LAYOUT



ABSOLUTE MAXIMUM RATINGS (Note 1)

Output Voltage (V_{CE})	50V
Input Voltage (V_{IN})	20V
Peak Collector Current, IC	600 mA
Continuous Collector Current, IC	500 mA
Continuous Base Current, IB	25 mA
Power Dissipation (PD) (per device)	1.0W
Total Package Limitation (Note 2)	2.0W
Derating Factor Above 25° C	13mW/° C
Ambient Operating Temperature Range (TA)	−55° C to +125° C
Storage Temperature Range (TS)	−65° C to +175° C

Note 1. At 25° C free-air temperature for any one Darlington unless otherwise noted.

Note 2. Under normal operating conditions, these units will sustain 350 mA per output with VCC = 1.6V at 70° C with a pulse width of 20mS and a duty cycle of 30%.

SG2001 through SG2005 Electrical Characteristics

(Parameters are specified at $T_A = +25°C$ unless otherwise noted)

CHARACTERISTIC	SYMBOL	APPLICABLE DEVICES	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Output Leakage Current	I_{CEX}	ALL	$V_{CE} = 50V$, $T_A = 25°C$	—	—	50	μA
			$V_{CE} = 50V$, $T_A = 70°C$	—	—	100	μA
		SG2002	$V_{CE} = 50V$, $T_A = 70°C$, $V_{IN} = 6.0V$	—	—	500	μA
		SG2004	$V_{CE} = 50V$, $T_A = 70°C$, $V_{IN} = 1.0V$	—	—	500	μA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	ALL	$I_C = 100$ mA, $I_B = 250$ μA	—	0.9	1.1	V
			$I_C = 200$ mA, $I_B = 350$ μA	—	1.1	1.3	V
			$I_C = 350$ mA, $I_B = 500$ μA	—	1.3	1.6	V
Input Current	$I_{IN(ON)}$	SG2002	$V_{IN} = 17V$	—	0.82	1.25	mA
		SG2003	$V_{IN} = 3.85V$	—	0.93	1.35	mA
		SG2004	$V_{IN} = 5.0V$	—	0.35	0.5	mA
			$V_{IN} = 12V$	—	1.0	1.45	mA
		SG2005	$V_{IN} = 3.0V$	—	1.5	2.4	mA
	$I_{IN(OFF)}$	ALL	$I_C = 500$ μA, $T_A = 70°C$	50	65	—	μA
Input Voltage	$V_{IN(ON)}$	SG2002	$V_{CE} = 2.0V$, $I_C = 300$ mA	—	—	13	V
		SG2003	$V_{CE} = 2.0V$, $I_C = 200$ mA	—	—	2.4	V
			$V_{CE} = 2.0V$, $I_C = 250$ mA	—	—	2.7	V
			$V_{CE} = 2.0V$, $I_C = 300$ mA	—	—	3.0	V
		SG2004	$V_{CE} = 2.0V$, $I_C = 125$ mA	—	—	5.0	V
			$V_{CE} = 2.0V$, $I_C = 200$ mA	—	—	6.0	V
			$V_{CE} = 2.0V$, $I_C = 275$ mA	—	—	7.0	V
			$V_{CE} = 2.0V$, $I_C = 350$ mA	—	—	8.0	V
		SG2005	$V_{CE} = 2.0V$, $I_C = 350$ mA	—	—	2.4	V
D-C Forward Current Transfer Ratio	h_{FE}	SG2001	$V_{CE} = 2.0V$, $I_C = 350$ mA	1000	—	—	
Input Capacitance	C_{IN}	ALL		—	15	25	pF
Turn-On-Delay	t_{PLH}	ALL	0.5 E_{IN} to 0.5 E_{OUT}	—	0.25	1.0	μSec.
Turn-Off Delay	t_{PHL}	ALL	0.5 E_{IN} to 0.5 E_{OUT}	—	0.25	1.0	μSec.
Clamp Diode Leakage Current	I_R	ALL	$V_R = 50V$, $T_A = 25°C$	—	—	50	μA
			$V_R = 50V$, $T_A = 70°C$	—	—	100	μA
Clamp Diode Forward Voltage	V_F	ALL	$I_F = 350$ mA	—	1.7	2.0	V

SG2011 through SG2015 Electrical Characteristics

(Parameters are specified at $T_A = +25°C$ unless otherwise noted)

CHARACTERISTIC	SYMBOL	APPLICABLE DEVICES	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Output Leakage Current	I_{CEX}	ALL	$V_{CE} = 50V$, $T_A = 25°C$	—	—	50	μA
			$V_{CE} = 50V$, $T_A = 70°C$	—	—	100	μA
		SG2012	$V_{CE} = 50V$, $T_A = 70°C$, $V_{IN} = 6.0V$	—	—	500	μA
		SG2014	$V_{CE} = 50V$, $T_A = 70°C$, $V_{IN} = 1.0V$	—	—	500	μA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	ALL	$I_C = 200$ mA, $I_B = 350$ μA	—	1.1	1.3	V
			$I_C = 350$ mA, $I_B = 500$ μA	—	1.3	1.6	V
			$I_C = 500$ mA, $I_B = 600$ μA	—	1.7	1.9	V
Input Current	$I_{IN(ON)}$	SG2012	$V_{IN} = 17V$	—	0.82	1.25	mA
		SG2013	$V_{IN} = 3.85V$	—	0.93	1.35	mA
		SG2014	$V_{IN} = 5.0V$	—	0.35	0.5	mA
			$V_{IN} = 12V$	—	1.0	1.45	mA
		SG2015	$V_{IN} = 3.0V$	—	1.5	2.4	mA
	$I_{IN(OFF)}$	ALL	$I_C = 500$ μA, $T_A = 70°C$	50	65	—	μA

SG2011 through SG2015 Electrical Characteristics (continued) (Parameters are specified at $T_A = +25°$ unless otherwise noted)

Input Voltage	$V_{IN(ON)}$	SG2012	$V_{CE} = 2.0V, I_C = 500$ mA	—	—	17	V
		SG2013	$V_{CE} = 2.0V, I_C = 250$ mA	—	—	2.7	V
			$V_{CE} = 2.0V, I_C = 300$ mA	—	—	3.0	V
			$V_{CE} = 2.0V, I_C = 500$ mA	—	—	3.5	V
		SG2014	$V_{CE} = 2.0V, I_C = 275$ mA	—	—	7.0	V
			$V_{CE} = 2.0V, I_C = 350$ mA	—	—	8.0	V
			$V_{CE} = 2.0V, I_C = 500$ mA	—	—	9.5	V
		SG2015	$V_{CE} = 2.0V, I_C = 500$ mA	—	—	2.6	V
D-C Forward Current Transfer Ratio	h_{FE}	SG2011	$V_{CE} = 2.0V, I_C = 350$ mA	1000	—	—	
			$V_{CR} = 2.0V, I_C = 500$ mA	900	—	—	
Input Capacitance	C_{IN}	ALL		—	15	25	pF
Turn-On Delay	t_{PLH}	ALL	0.5 E_{IN} to 0.5 E_{OUT}	—	0.25	1.0	μSec.
Turn-Off Delay	t_{PHL}	ALL	0.5 E_{IN} to 0.5 E_{OUT}	—	0.25	1.0	μSec.
Clamp Diode Leakage Current	I_R	ALL	$V_R = 50V, T_A = 25°C$	—	—	50	μA
			$V_R = 50V, T_A = 70°C$	—	—	100	μA
Clamp Diode Forward Voltage	V_F	ALL	$I_F = 350$ mA	—	1.7	2.0	V
			$I_F = 500$ mA	—	2.1	2.5	V

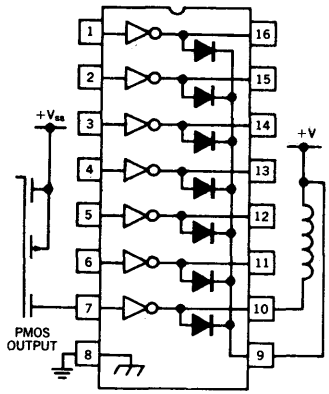
SG2021 through SG2025 Electrical Characteristics

(Parameters are specified at $T_A = +25°C$ unless otherwise noted)

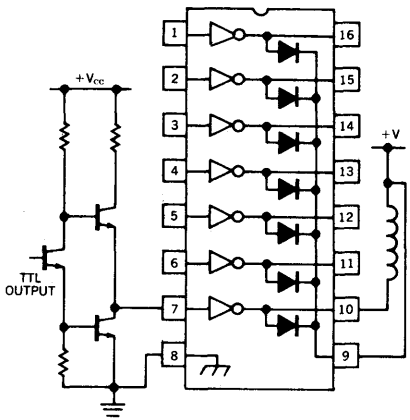
CHARACTERISTIC	SYMBOL	APPLICABLE DEVICES	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Output Leakage Current	I_{CEX}	ALL	$V_{CE} = 95V, T_A = 25°C$	—	—	50	μA
			$V_{CE} = 95V, T_A = 70°C$	—	—	100	μA
		SG2022	$V_{CE} = 95V, T_A = 70°C, V_{IN} = 6.0V$	—	—	500	μA
		SG2024	$V_{CE} = 95V, T_A = 70°C, V_{IN} = 1.0V$	—	—	500	μA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	ALL	$I_C = 100$ mA, $I_B = 250$ μA	—	0.9	1.1	V
			$I_C = 200$ mA, $I_B = 350$ μA	—	1.1	1.3	V
			$I_C = 350$ mA, $I_B = 500$ μA	—	1.3	1.6	V
Input Current	$I_{IN(ON)}$	SG2022	$V_{IN} = 17V$	—	0.82	1.25	mA
		SG2023	$V_{IN} = 3.85V$	—	0.93	1.35	mA
		SG2024	$V_{IN} = 5.0V$	—	0.35	0.5	mA
			$V_{IN} = 12V$	—	1.0	1.45	mA
		SG2025	$V_{IN} = 3.0V$	—	1.5	2.4	mA
	$I_{IN(OFF)}$	ALL	$I_C = 500$ μA, $T_A = 70°C$	50	65	—	μA
Input Voltage	$V_{IN(ON)}$	SG2022	$V_{CE} = 2.0V, I_C = 300$ mA	—	—	13	V
		SG2023	$V_{CE} = 2.0V, I_C = 200$ mA	—	—	2.4	V
			$V_{CE} = 2.0V, I_C = 250$ mA	—	—	2.7	V
			$V_{CE} = 2.0V, I_C = 300$ mA	—	—	3.0	V
		SG2024	$V_{CE} = 2.0V, I_C = 125$ mA	—	—	5.0	V
			$V_{CE} = 2.0V, I_C = 200$ mA	—	—	6.0	V
			$V_{CE} = 2.0V, I_C = 275$ mA	—	—	7.0	V
			$V_{CE} = 2.0V, I_C = 350$ mA	—	—	8.0	V
		SG2025	$V_{CE} = 2.0V, I_C = 350$ mA	—	—	2.4	V
D-C Forward Current Transfer Ratio	h_{FE}	SG2021	$V_{CE} = 2.0V, I_C = 350$ mA	1000	—	—	
Input Capacitance	C_{IN}	ALL		—	15	25	pF
Turn-On Delay	t_{PLH}	ALL	0.5 E_{IN} to 0.5 E_{OUT}	—	0.25	1.0	μSec.
Turn-Off Delay	t_{PHL}	ALL	0.5 E_{IN} to 0.5 E_{OUT}	—	0.25	1.0	μSec.
Clamp Diode Leakage Current	I_R	ALL	$V_R = 95V, T_A = 25°C$	—	—	50	μA
			$V_R = 95V, T_A = 70°C$	—	—	100	μA
Clamp Diode Forward Voltage	V_F	ALL	$I_F = 350$ mA	—	1.7	2.0	V

TYPICAL APPLICATIONS

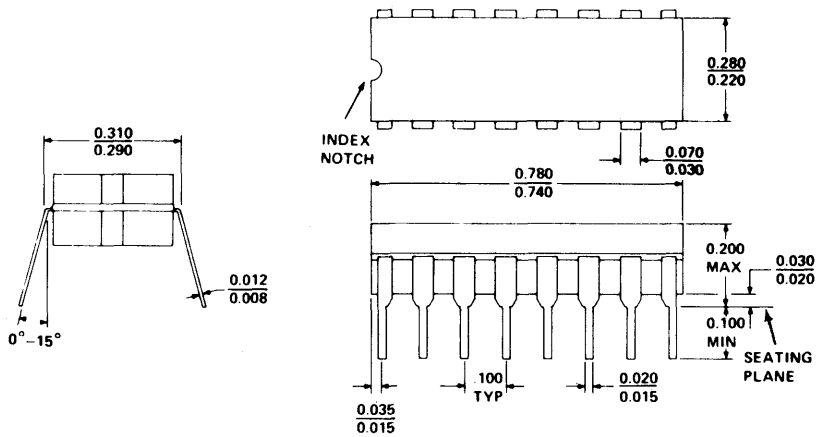
PMOS TO LOAD



TTL TO LOAD



PACKAGE CONFIGURATION



J PACKAGE 16-PIN CERDIP

ORDERING INFORMATION

DEVICE	V_{CE} MAX	I_C MAX	LOGIC INPUTS
SG2001	50V	500mA	General Purpose PMOS, CMOS
SG2002	50V	500mA	14-25V PMOS
SG2003	50V	500mA	5V TTL, CMOS
SG2004	50V	500mA	6-15V CMOS, PMOS
SG2005	50V	500mA	High Output TTL
SG2011	50V	600mA	General Purpose PMOS, CMOS
SG2012	50V	600mA	14-25V PMOS
SG2013	50V	600mA	5V TTL, CMOS

DEVICE	V_{CE} MAX	I_C MAX	LOGIC INPUTS
SG2014	50V	600mA	6-15V CMOS, PMOS
SG2015	50V	600mA	High Output TTL
SG2021	95V	500mA	General Purpose PMOS, CMOS
SG2022	95V	500mA	14-25V PMOS
SG2023	95V	500mA	5V TTL, CMOS
SG2024	95V	500mA	6-15V CMOS, PMOS
SG2025	95V	500mA	High Output TTL

SG2064 THRU SG2077

QUAD 1.5 AMP DARLINGTON SWITCHES

DESCRIPTION

These high-voltage, high-current Darlington arrays are monolithic bipolar devices especially designed for interfacing low-level control logic and peripheral loads such as relays, solenoids, DC and stepping motors; multiplexed LED and incandescent displays; and heaters. The logic inputs are designed to be compatible with TTL, DTL, LSTTL, CMOS and NMOS logic families. Several of the arrays include integral clamp diodes for driving inductive loads, and breakdown voltage ratings to 80 volts are available.

All devices are supplied in a modified 16-lead plastic dual-in-line package. A copper alloy lead frame with webbing between the central pins provides low thermal resistance to ambient air, and allows a 2.8 watt total power dissipation rating within a standard footprint.

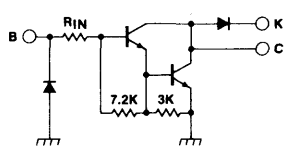
These devices are direct replacements for ULN-2064B thru ULN-2077B devices.

FEATURES

- **Four power drivers per package**
- **1.5 amp collector currents**
- **80 and 50 volt BV_{CEX} ratings**
- **Integral clamp diodes for inductive loads**
- **Compatibility with all popular logic families**
- **Low internal parasitics**

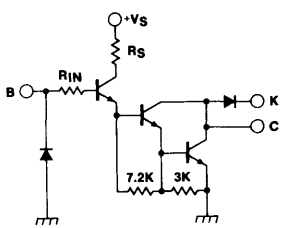
SG2064 thru SG2067	SG2068 thru SG2071	SG2074 thru SG2077

SCHEMATIC DIAGRAMS



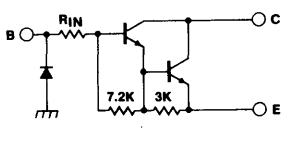
SG2064/2065: R_{IN} = 350Ω
SG2066/2067: R_{IN} = 3K

¼ SCHEMATIC SHOWN



SG2068/2069: R_{IN} = 2.5K, R_S = 900Ω
SG2070/2071: R_{IN} = 11.6K, R_S = 3.4K

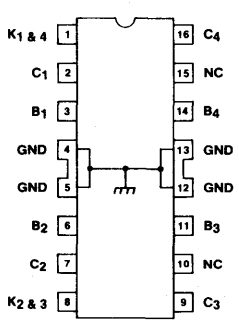
¼ SCHEMATIC SHOWN

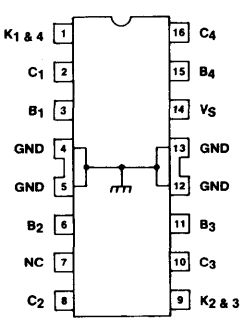


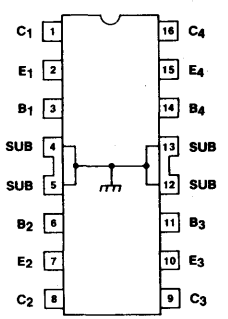
SG2074/2075: R_{IN} = 350Ω
SG2076/2077: R_{IN} = 3K

¼ SCHEMATIC SHOWN

CONNECTION DIAGRAMS







SG2064 THRU SG2077

ABSOLUTE MAXIMUM RATINGS (Note 1)

Logic Input Voltage	See Selection Guide
Logic Input Current	25mA
Supply Voltage	
SG2068, 2069	10V
SG2070, 2071	20V
Output Voltage	See Selection Guide
Output Current	1.75A

Power Dissipation at T_A = +25°C (Note 2)	2.77W
Thermal Resistance: junction to ambient	45°C/W
Operating Junction Temperature	+150°C
Operating Ambient Temperature Range	0°C to +70°C
Storage Temperature Range	−55°C to +125°C
Lead Temperature (Soldering, 10 seconds)	+300°C

Note 1. Values beyond which damage may occur. Note 2. Derate at 22.2 mW/°C for ambient temperatures above +25°C.

SELECTION GUIDE

DEVICE	V_{CEX} MAX	$V_{CE\ (SUS)}$ MAX	V_{IN} MAX	LOGIC INPUTS
SG2064W	50V	35V	15V	TTL, DTL, Schottky TTL, 5V CMOS and NMOS
SG2065W	80V	50V	15V	
SG2066W	50V	35V	30V	6 to 15V CMOS and PMOS
SG2067W	80V	50V	30V	
SG2068W	50V	35V	15V	TTL, DTL, Schottky TTL, 5V CMOS and NMOS
SG2069W	80V	50V	15V	
SG2070W	50V	35V	30V	6 to 15V CMOS and PMOS
SG2071W	80V	50V	30V	
SG2074W	50V	35V	30V	General Purpose
SG2075W	80V	50V	60V	
SG2076W	50V	35V	30V	6 to 15V CMOS and PMOS
SG2077W	80V	50V	60V	

SG2064 THRU SG2067 ELECTRICAL CHARACTERISTICS

(Parameter limits are specified at T_A = +25°C unless otherwise noted.)

PARAMETER	DEVICES	CONDITIONS	MIN	MAX	UNITS
Output Leakage Current	SG2064/66	V_{CE} = 50V		100	μA
		V_{CE} = 50V, T_A = 70°C		500	μA
	SG2065/67	V_{CE} = 80V		100	μA
		V_{CE} = 80V, T_A = 70°C		500	μA
Output Sustaining Voltage	SG2064/66	I_C = 100 mA, V_{IN} = 0.4V	35		V
	SG2065/67	I_C = 100 mA, V_{IN} = 0.4V	50		V
Collector-Emitter Saturation Voltage	All	I_C = 500 mA, I_B = 625 μA		1.1	V
		I_C = 750 mA, I_B = 935 μA		1.2	V
		I_C = 1.0 A, I_B = 1.25 mA		1.3	V
	SG2064/66	I_C = 1.25 A, I_B = 2.0 mA		1.4	V
	SG2065/67	I_C = 1.5 A, I_B = 2.25 mA		1.5	V
Input Current	SG2064/65	V_{IN} = 2.4V	1.4	4.3	mA
		V_{IN} = 3.75V	3.3	9.6	mA
	SG2066/67	V_{IN} = 5.0V	0.6	1.8	mA
		V_{IN} = 12V	1.7	5.2	mA
Input Voltage	SG2064/65	V_{CE} = 2.0V, I_C = 1.0 A		2.0	V
		V_{CE} = 2.0V, I_C = 1.5 A		2.5	V
	SG2066/67	V_{CE} = 2.0V, I_C = 1.0 A		6.5	V
		V_{CE} = 2.0V, I_C = 1.5 A		10	V
Turn-On Delay	All	0.5 E_{in} to 0.5 E_{out}		1.0	μS
Turn-Off Delay	All	0.5 E_{in} to 0.5 E_{out}		1.5	μS
Clamp Diode Leakage Current	SG2064/66	V_R = 50V		50	μA
		V_R = 50V, T_A = 70°C		100	μA
	SG2065/67	V_R = 80V		50	μA
		V_R = 80V, T_A = 70°C		100	μA
Clamp Diode Forward Voltage	All	I_F = 1.0 A		1.75	V
		I_F = 1.5 A		2.0	V

SG2068 THRU SG2071 ELECTRICAL CHARACTERISTICS

(Parameter limits are specified at T_A = +25°C unless otherwise noted.)

PARAMETER	DEVICES	CONDITIONS	MIN	MAX	UNITS
Output Leakage Current	SG2068/70	V_{CE} = 50V		100	µA
		V_{CE} = 50V, T_A = 70°C		500	µA
	SG2069/71	V_{CE} = 80V		100	µA
		V_{CE} = 80V, T_A = 70°C		500	µA
Output Sustaining Voltage	SG2068/70	I_C = 100 mA, V_{IN} = 0.4V	35		V
	SG2069/71	I_C = 100 mA, V_{IN} = 0.4V	50		V
Collector-Emitter Saturation Voltage	SG2068/69	I_C = 500 mA, V_{IN} = 2.75V		1.1	V
		I_C = 750 mA, V_{IN} = 2.75V		1.2	V
		I_C = 1.0 A, V_{IN} = 2.75V		1.3	V
		I_C = 1.25 A, V_{IN} = 2.75V		1.4	V
	SG2069	I_C = 1.5 A, V_{IN} = 2.75V		1.5	V
	SG2070/71	I_C = 500 mA, V_{IN} = 5.0V		1.1	V
		I_C = 750 mA, V_{IN} = 5.0V		1.2	V
		I_C = 1.0 A, V_{IN} = 5.0V		1.3	V
		I_C = 1.25 A, V_{IN} = 5.0V		1.4	V
	SG2071	I_C = 1.5 A, V_{IN} = 5.0V		1.5	V
Input Current	SG2068/69	V_{IN} = 2.75V		550	µA
		V_{IN} = 3.75V		1000	µA
	SG2070/71	V_{IN} = 5.0V		400	µA
		V_{IN} = 12V		1250	µA
Input Voltage	SG2068/69	V_{CE} = 2.0V, I_C = 1.5A		2.75	V
	SG2070/71	V_{CE} = 2.0V, I_C = 1.5A		5.0	V
Supply Current	SG2068/69	I_C = 500 mA, V_{IN} = 2.4V		6.0	mA
	SG2070/71	I_C = 500 mA, V_{IN} = 5.0V		4.5	mA
Turn-On Delay	All	0.5 E_{in} to 0.5 E_{out}		1.0	µS
Turn-Off Delay	All	0.5 E_{in} to 0.5 E_{out}		1.5	µS
Clamp Diode Leakage Current	SG2068/70	V_R = 50V		50	µA
		V_R = 50V, T_A = 70°C		100	µA
	SG2069/71	V_R = 80V		50	µA
		V_R = 80V, T_A = 70°C		100	µA
Clamp Diode Forward Voltage	All	I_F = 1.0 A		1.75	V
		I_F = 1.5 A		2.0	V

SG2074 THRU SG2077 ELECTRICAL CHARACTERISTICS

(Parameter limits are specified at T_A = +25°C unless otherwise noted.)

PARAMETER	DEVICES	CONDITIONS	MIN	MAX	UNITS
Output Leakage Current	SG2074/76	V_{CE} = 50V		100	µA
		V_{CE} = 50V, T_A = 70°C		500	µA
	SG2075/77	V_{CE} = 80V		100	µA
		V_{CE} = 80V, T_A = 70°C		500	µA
Output Sustaining Voltage	SG2074/76	I_C = 100 mA, V_{IN} = 0.4V	35		V
	SG2075/77	I_C = 100 mA, V_{IN} = 0.4V	50		V
Collector-Emitter Saturation Voltage	All	I_C = 500 mA, I_B = 625 µA		1.1	V
		I_C = 750 mA, I_B = 935 µA		1.2	V
		I_C = 1.0 A, I_B = 1.25 mA		1.3	V
	SG2074/76	I_C = 1.25 A, I_B = 2.0 mA		1.4	V
	SG2075/77	I_C = 1.5 A, I_B = 2.25 mA		1.5	V
Input Current	SG2074/75	V_{IN} = 2.4V	2.0	4.3	mA
		V_{IN} = 3.75V	4.5	9.6	mA
	SG2076/77	V_{IN} = 5.0V	0.9	1.8	mA
		V_{IN} = 12V	2.75	5.2	mA
Input Voltage	SG2074/75	V_{CE} = 2.0V, I_C = 1.0A		2.0	V
		V_{CE} = 2.0V, I_C = 1.5A		2.5	V
	SG2076/77	V_{CE} = 2.0V, I_C = 1.0 A		6.5	V
		V_{CE} = 2.0V, I_C = 1.5 A		10	V
Turn-On Delay	All	0.5 E_{in} to 0.5 E_{out}		1.0	µS
Turn-Off Delay	All	0.5 E_{in} to 0.5 E_{out}		1.5	µS

CHARACTERISTIC CURVES

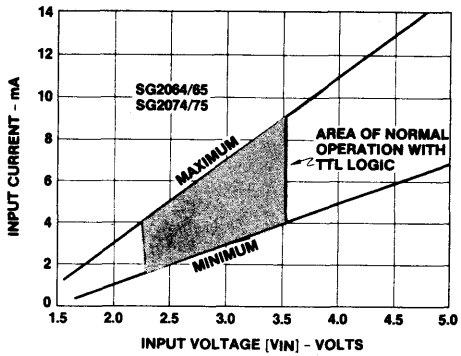


Figure 1. Logic Input Current vs. Input Voltage — 5V Logic.

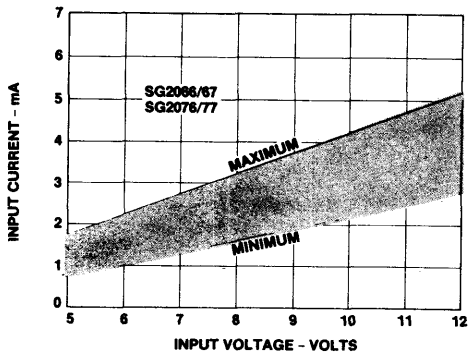


Figure 2. Logic Input Current vs. Input Voltage — High Level Logic.

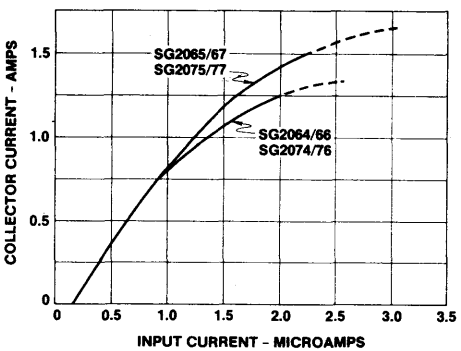


Figure 3. Maximum Required Logic Input Current vs. Collector Current.

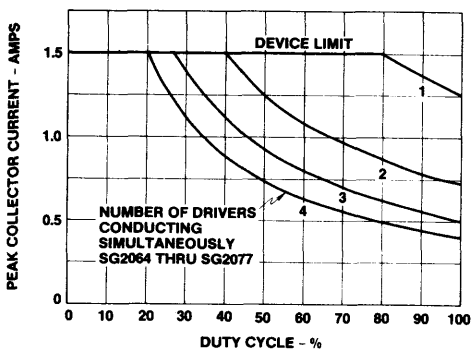
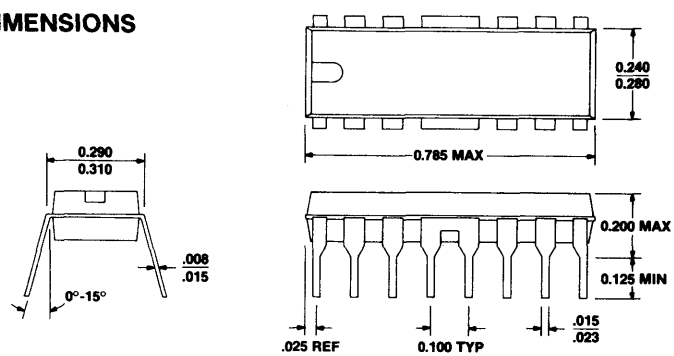


Figure 4. Peak Allowable Collector Current vs. Duty Cycle at T_A = + 70°C.

PHYSICAL DIMENSIONS



W-PACKAGE
16-PIN PLASTIC

ADVANCED DATA
SG3636

Performance data described herein represent design goals.
Final device specifications are subject to change.

1.5 AMP DUAL HALF BRIDGE DRIVER

DESCRIPTION

The SG3636 is a monolithic integrated circuit designed especially for driving loads connected in an H bridge configuration. Inputs to this device are TTL compatible and the outputs are capable of sourcing and sinking up to 1.5 Amps of current. Suppression diodes are included on chip for use with inductive loads.

FEATURES

- **Low voltage operation 8 to 25 volts**
- **Source or sink up to 1.5 Amps**
- **TTL compatible inputs**
- **Built-in clamp diodes for inductive loads**
- **Built in thermal protection**

ABSOLUTE MAXIMUM RATINGS

V_S = 30 volts
I_{OUT} = 2.0A
Diode current 2.0A
V_{IN} = 7 volts

ELECTRICAL CHARACTERISTICS

Unless otherwise stated, V_S = 25 Volts

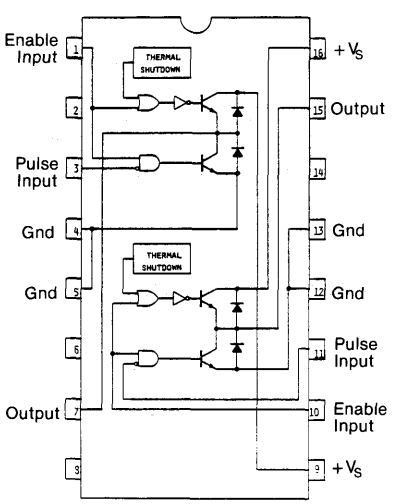
PARAMETER	SYMBOL	TEST CONDITIONS	TYP	UNITS
Input High Current	I_{in} (1)	V_{in} = 2.4V	200	μA
Input Low Current	I_{in} (0)	V_{in} = 0V	2.4	mA
Low Level Input Voltage	V_{in} (0)		0.8	Volts
High Level Input Voltage	V_{in} (1)		2.0	Volts
Source Saturation	V_{ce} (sat)	I_{source} = 1 amp	2.0	Volts
Sink Saturation	V_{ce} (sat)	I_{sink} = 1 amp	2.0	Volts
Supply Current	I_S	V_S = 25v	50	mA
Diode Forward Voltage	V_F	I_F = 1.0A	1.2	Volt

TRUTH TABLE EACH HALF BRIDGE

Enable	Pulse	Output
1	1	Off (High with no load)
0	1	High
1	0	Low
0	0	High

(1= open or high)

LOGIC DIAGRAM



ADVANCED DATA
SG3637

Performance data described herein represent design goals.
Final device specifications are subject to change.

UNIVERSAL QUAD 2 AMP DRIVER

DESCRIPTION

The SG3637 is a four channel high current, high voltage integrated circuit designed to provide the interface between stepper motors and micro-processor or logic motor control circuitry. The SG3637 will accept most standard logic signal inputs and provide motor drive current to both positive and negative supply rails.

FEATURES

- **Output currents to 2.0 amps**
- **40 volt outputs to positive or negative rails**
- **Compatibility with all popular logic families**
- **Built-in clamp diodes for inductive loads**
- **Chip enable for microprocessor control**

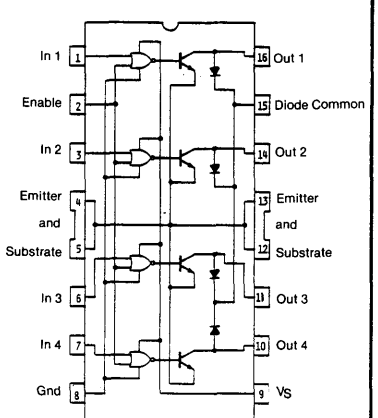
ABSOLUTE MAXIMUM RATINGS

V_{SS} = 20 volts
I_{OUT} = 2.5 amps
V_{OUT} = 45 volts
V_{IN} = 25 volts

ELECTRICAL CHARACTERISTICS @ 25°C

Unless otherwise stated, V_{SS} = 15V, pins 4, 5, 12 and 13 are ground

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNITS
"O" Level Supply Current	I_{SS} (O)				40	mA
"I" Level Supply Current	I_{SS} (1)	All inputs = 5.0V			20	mA
"O" Input Current Except Enable	I_{IN} (O)	All inputs ground			200	μA
"O" Input Current Enable Input	I_{INE} (O)	Enable input ground			400	μA
"I" Input Current All Inputs	I_{IN} (1)	Driven input = 15V			50	μA
Output Leakage Current	I_{cex}	V_{out} = 60V, V_{in} = 2.0V, other inputs ground			500	μA
Output Sustaining Voltage	V_{ce} (sus)	I_{out} = 100mA, inputs = 5.0V	35			Volts
Output ON Voltage	V_{ce} (sat)	I_{out} = 2.0 Amp, inputs ground			2.2	Volts
Diode Leakage	I_R	V_R = 60V			50	μA
Diode Forward Voltage	V_F	I_F = 2.0 Amp			2.5	Volts



ADVANCED DATA
SG3638/SG3638A
SG3639/SG3639A

Performance data described herein represent design goals.
Final device specifications are subject to change.

4 AMP SOLENOID AND MOTOR DRIVER

DESCRIPTION

The SG3638 and SG3639 are high voltage integrated circuits designed to be used as "H" bridge drivers, dual solenoid drivers and more. These devices allow current control of loads by means of external series sense resistors and a threshold control input. The SG3638 and SG3639 feature built-in thermal protection. They are designed for use with a split power supply for the motor or solenoid.

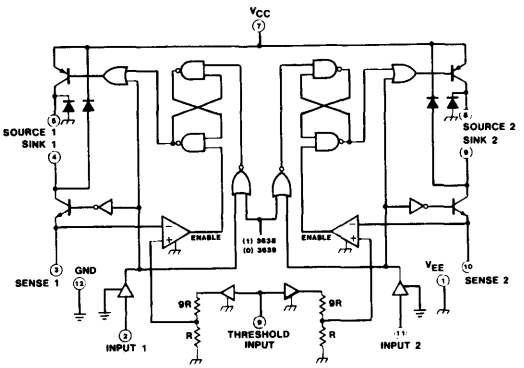
FEATURES

- **Chopped Mode Current Control**
- **Output Current to 4 Amps**
- **60 Volt Output Drivers (A Suffix)**
- **TTL Compatible INPUT and MODE pins**
- **Combined Threshold and Logic Input**
- **Built-in Thermal Protection**
- **Built-in Clamp Diodes for Inductive Loads**
- **Split Voltage Power Supply Operation**
- **Packaged in a 12 Lead Power SIP**

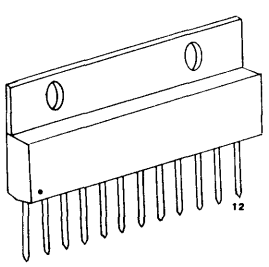
TRUTH TABLE

	In	Enable	Sink	Source
SG3638	I	O/I	Off	Off
	O	I	On	On
	O	O	On	Off
SG3639	I	O/I	Off	Off
	O	I	On	On
	O	↓	On	Off
	O	↑	On	Off

BLOCK DIAGRAM



CONNECTION DIAGRAM (Top View)



Pin	Function
1	V_{EE}
2	Input 1
3	Sense 1
4	Sink 1
5	Source 1
6	Threshold Input
7	V_{CC}
8	Source 2
9	Sink 2
10	Sense 2
11	Input 2
12	GND

ORDER INFORMATION

Part Number	Max Voltage (V_{CC} to V_{EE})	Package
SG3638S	40V	12 pin SIP
SG3638AS	50V	12 pin SIP
SG3639S	40V	12 pin SIP
SG3639AS	50V	12 pin SIP

ABSOLUTE MAXIMUM RATINGS

Supply Voltage V_{EE} to V_{CC}	±20 (±25)
Input Voltage Range	0.0V to 7.0V
Peak Output Current	±5A
Output Current 33% D.C.	±4.4A

Continuous Output Current	±1A
Package Power Dissipation (average) (without heatsink T_A = 25°C)	4.5 watts
Operating Temperature Range	−20°C to +85° C
Storage Temperature Range	−55°C to +150°C

ELECTRICAL CHARACTERISTICS (V_S = 40V, T_A = −20°C to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}, V_{EE}	operating	±15	—	±20 (±25)	volts
Package Power Dissipation		V_S = ±20 (±25)	—	10	—	Watts
Supply Current		V_S = ±20 (±25)	—	12	20	mA
Signal Input Threshold	$V_{\overline{sig}}$		—	1.4	—	volts
Mode Input Threshold	V_{mode}		—	1.4	—	volts
Internal Chopping Threshold	$V_{THE\ chop}$		—	4.0	—	volts
Threshold Input Disable Voltage	$V_{THE\ enable}$		—	0.45	—	volts
Signal Input Current (low)	$I_{\overline{sig}\ L}$	$V_{\overline{sig}}$ = .4V	−1.6	—	—	mA
Signal Input Current (high)	$I_{\overline{sig}\ H}$	$V_{\overline{sig}}$ = 2.4V	—	—	100	µA
Mode Input Current (low)	$I_{mode\ L}$	V_{mode} = .4V	−1.6	—	—	mA
Mode Input Current (high)	$I_{mode\ H}$	V_{mode} = 2.4V	—	—	100	µA
Threshold Input Current (low)	$I_{THE\ L}$	$V_{THE} < V_{THE\ enable}$	—	−6.0	—	µA
Threshold Input Current (high)	$I_{THE\ H}$	$V_{THE} > V_{THE\ enable}$	—	−2.0	—	µA
Internal Hysteresis Current	I_{HYS}		—	.1 I peak	—	
External Hysteresis Current	$I_{HYS\ ext}$		140	200	260	µA
Output SAT Voltage sink	$V_{SAT\ sink}$	I_{at} = 4.4A	—	2.0	2.5	volts
Output SAT Voltage source	$V_{SAT\ source}$	I_{out} = −4.4A	—	2.5	3.0	volts
Output SAT Voltage sink	$V_{SAT\ sink}$	I_{out} = 1.0A	—	1.0	1.2	volts
Output SAT Voltage source	$V_{SAT\ source}$	I_{out} = −1.0A	—	1.5	1.8	volts
Output Leakage sink	$I_{OL\ sink}$	V_{CE} = 40V (60)	—	—	1.0	mA
Output Leakage source	$I_{OL\ source}$	V_{CE} = 40V (50)	—	—	1.0	mA
Output Current		30% on	—	+4.0	+4.4	A
Transconductance Tolerance	(note 1)	V_{THE} = 2.0 to 3.6V V_{THE} = 1.0 to 2.0V V_{THE} = 0.6 to 1.0V		−5% −10% −25%	— — —	+ 5% +10% +25%
Clamp Diode Voltage sink	$V_{C\ sink}$	I = 4.4A	—	2.0	2.5	volts
Clamp Diode Voltage source	$V_{C\ source}$	I = 4.4A	—	3.0	3.5	volts
GAIN I_{out} / V_{THE} (R_S)			—	.1		

NOTE (1) Assumes R_S is exactly known. R_S includes parasitic wiring resistances external to the I.C. package in addition to the intended sense resistor.

SWITCHING CHARACTERISTICS (V_S = 20°C to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Source Turn On Delay	t_{D} on	1.4V $V_{\overline{sig}}$ to 10% V_{source}		300		ns
Source Rise Time	t_{R} on	V_{source} 10% to 90%		100		ns
Source Fall Time	t_{F} on	V_{source} 90% to 10%		500		ns
Sink Turn Off Delay	t_{D} off	1.4V $V_{\overline{sig}}$ to 10% V_{sink}		500		ns
Sink Rise Time	t_{R} off	V_{sink} 10% to 90%		400		ns
Sense Loop Turn On Delay	t_{DS} on	$V_{TH\ sense\ 1}$ to 50% V_{source}		TBD*		
Sense Loop Turn Off Delay	t_{DS} off	$V_{TH\ sense\ 2}$ to 50% V_{sink}		TBD*		

*To Be Determined

6

FUNCTIONAL DESCRIPTION

SG3638 (non-chop drive)
The state of the INPUT pin directly controls the state of the sink transistor. When INPUT ($V_{\overline{sig}}$) is is high the sink transistor is turned off. When INPUT is low sink transistor acts as a saturation switch.
The source transistor is directly controlled by a high to the INPUT pin. When INPUT is low the source is controlled by the result of a comparison of the voltage across an external resistor and the THRESHOLD INPUT.
With a high on the INPUT, both the output sink and source transistors are turned off which force SENSE to be pulled to ground through an external resistor. This produces a high on the output of the internal comparator and forces the output of the latch to a low state. As INPUT is switched low, both the sink and source transistors are turned on. This causes both the current in a coil, located between the SINK and SOURCE outputs, as well as the voltage across the sense resistor to rise. When the voltage across the sense resistor reaches one tenth the THRESHOLD INPUT voltage the comparator trips and sets the latch thus turning the source transistor off. The latch is reset when the INPUT returns to a high state.

SG3639 (chop drive)
The initial conditions are the same as in the SG3638 except the latch is disabled and acts as a simple inverter. Both SINK and SOURCE turn on as INPUT goes low. When the voltage across the external sense resistor reaches one tenth the THRESHOLD INPUT voltage the comparator switches turning SOURCE off and causing the voltage across the sense resistor to decay. The tripping of the comparator also turns on a current source (I_{HYS}, typically 200 μA) which is tied to the THRESHOLD INPUT and lowers the threshold by an amount determined by the external impedance at the THRESHOLD INPUT (R_{HYS}). This impedance sets up the externally adjustable hysteresis. When the current decays to the new lower threshold level the comparator trips again turning the SOURCE on and resetting the threshold to its original value.

Chop Mode Default Hysteresis
In the Chop Mode, if the THRESHOLD INPUT signal becomes larger than 4 volts (approx.) the output current will no longer increase. At this point the chop hysteresis will switch to an internally controlled value of approximately 10%. This allows the threshold to be left floating and provides a default to the maximum operating current with a 10% hysteresis.

THERMAL AND POWER CHARACTERISTICS

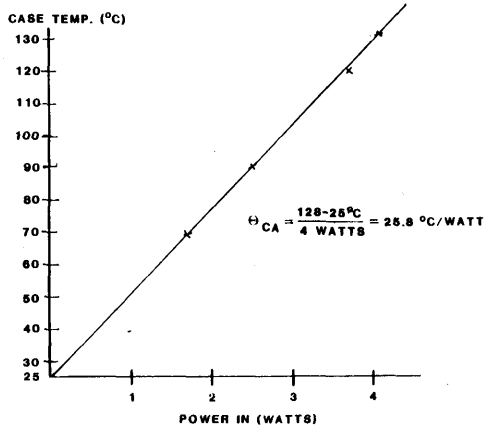


Figure 2 SIP Package Dissipation
(No Air Flow or Heat Sink)

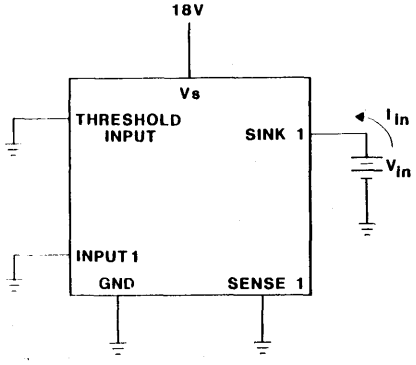
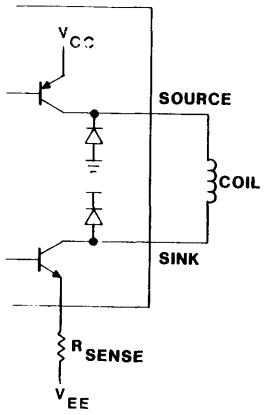
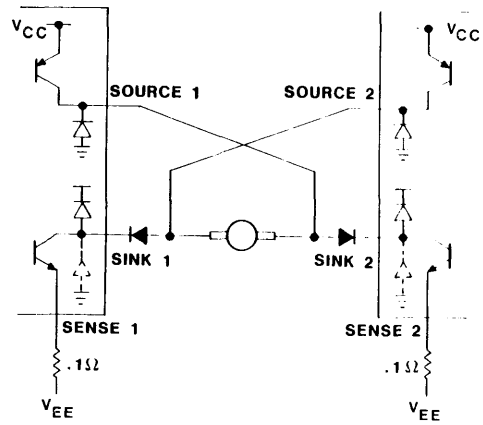


Figure 5 Test Fixture for Thermal Measurements

Thermal Shutdown	$T_{J_{SD}}$ = 160°
Thermal Resistance	Θ_{JA} = 30° C/W (typical)
	Θ_{JC} = 2° C/W (typical)





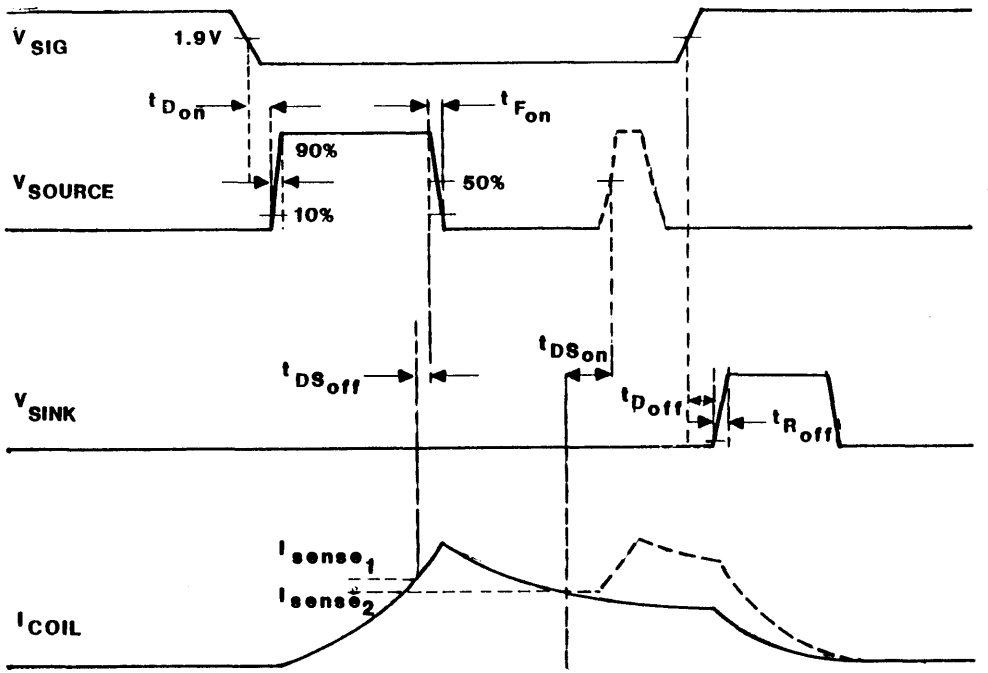
APPLICATIONS

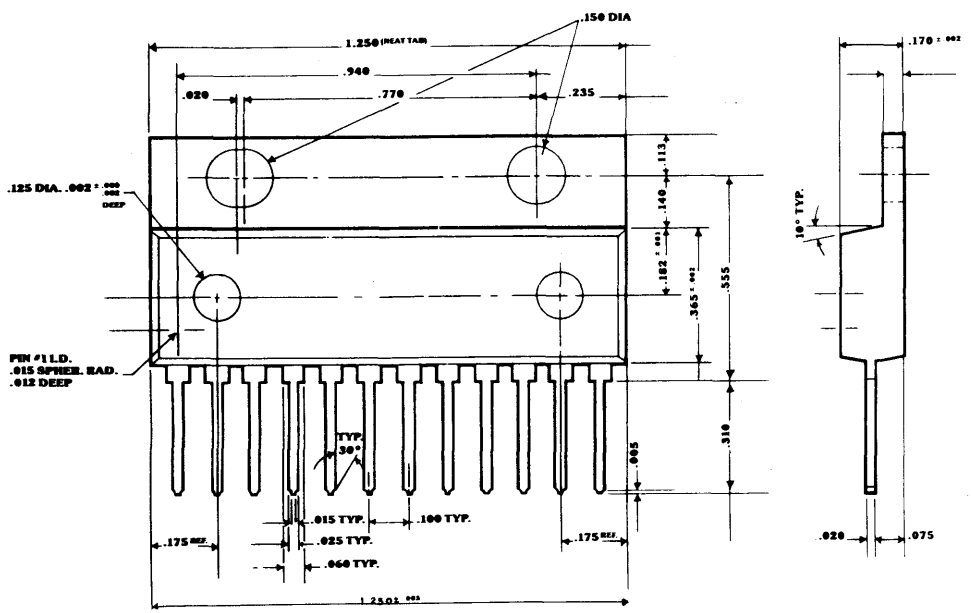
The SG3638 or 3639 can be used to drive a solenoid as seen in Figure 4. The coil is connected between the collector of the source and the collector of the sink transistors. The internal clamp diodes make this application possible without external diodes.
When driving a motor, both halves of the device are used in a cross coupled configuration as seen in Figure 5. In this configuration external diodes must be used to isolate an internal paracitic diodes. Without these external diodes the device will be damaged. These diodes must be of the high speed type with voltage ratings above 70 volts and capable of handling 4 Amps. Both inputs should not be turned on at the same time.
The SG3639 requires a resistor (R_{HYS}) in series with the THRESHOLD INPUT and the external circuit which controls the THRESHOLD INPUT to set the amount of hysteresis.

CIRCUIT CONSIDERATIONS

PC Board Layout — The output current is controlled by both the voltage at the SENSE pin and the sense resistor. Because of the large currents and low resistances, it is critical to have an extremely good PC board layout to reduce paracitic wiring resistances which could add to the sense resistor and reduce the output current.

Thermal — Because of the large power dissipation usually associated with this device, a heat sink is recommended. Air flow around the package may also reduce package temperature. The device has built in thermal shutdown capabilities which will turn the output off when the substrate reaches a temperature of 140 to 160 degrees C.


V SIG
1.9V
t Don
t Fon
90%
50%
10%
V SOURCE
t DSoff
t DSon
t Doff
t Roff
V SINK
I sense1
I sense2
I COIL


.150 DIA
1.250 (REAT TAB)
.940
.020
.770
.235
.125 DIA. .002
DEEP
PIN #1 I.D.
.015 SPHER. RAD.
.012 DEEP
TYP.
30°
.015 TYP.
.100 TYP.
.025 TYP.
.060 TYP.
.175 REF.
.175 REF.
.113
.140
.555
.310
.065
10° TYP.
.020
.075

4 AMP SOLENOID AND MOTOR DRIVER

DESCRIPTION

The SG3640 and SG3641 are high voltage integrated circuits designed to be used as ½ "H" bridge drivers, solenoid drivers and more. Both devices allow current control of loads by means of internal series sense resistors and a current level control input. Both feature built-in thermal protection.

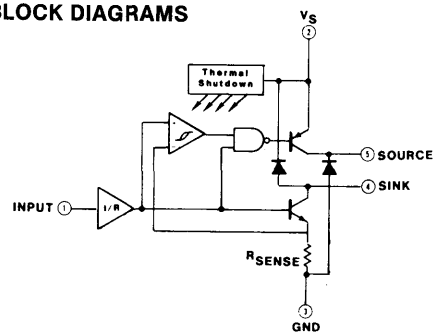
The built-in sense resistors, the current input and the 5 lead TO-220 package offer substantial advantages over the SG3638 and SG3639 in many applications.

The SG3640 provides continuous chop mode control, while the SG3641 provides a single pulse which drives the source output to the controlled current.

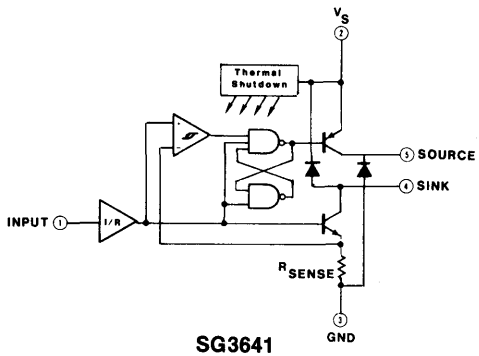
FEATURES

- **Chopped Mode Current Control**
- **Output Current to 4 Amps**
- **40 Volt Output Drivers**
- **Source Current 500 Times Input Current**
- **Combined Threshold and Logic Input**
- **Built-in Thermal Protection**
- **Built-in Clamp Diodes for Inductive Loads**
- **Available in a 5 lead Power TO-220 Package**

BLOCK DIAGRAMS

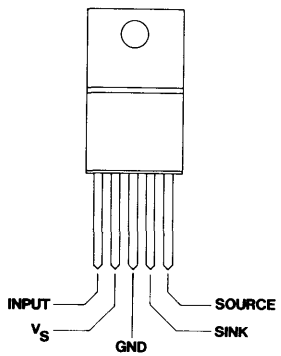


SG3640



SG3641

CONNECTION DIAGRAM (Top View)



TO-220 Package

ORDER INFORMATION

Part Number	Mode	Package
SG3640P	Chop	TO-220
SG3641P	Non-Chop	TO-220
SG3640R	Chop	TO-66
SG3641R	Non-Chop	TO-66

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	40V
Input Voltage Range	−1.0V to 7.0V
Peak Output Current	±5A
Output Current 33% D.C.	±4.4A
Continuous Output Current	±1A
Operating Temperature Range	−20°C to +85° C
Storage Temperature Range	−55°C to +150°C

ELECTRICAL CHARACTERISTICS

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Temperature Range, Operating	T_A	−20	—	85	°C
Package Power Dissipation	V_S = 40V	—	10	—	Watts
Supply Voltage, V_S	Operating	15	—	40	Volts
Supply Current, Idle	V_S = 40	—	12	20	mA
Input Voltage Range	All	−0.1	—	6	Volts
Input Current	V_{IN} = 2.5V	—	−2.0	−10.0	μA
Input Hysteresis Current	V_{IN} = 2.5V	140	200	260	μA
Current Regulation	V_{IN} = 2 to 4V	—	—	5	%
Output Current	30% ON	—	±4.0	±4.4	A
Output Sat Voltage, Sink	+4.4A	—	2.0	2.5	Volts
Output Sat Voltage, Source	−4.4A	—	2.5	3.0	Volts
Output Sat Voltage, Sink	+1.0A	—	1.0	1.2	Volts
Output Sat Voltage, Source	−1.0A	—	1.5	1.8	Volts
Output Leakage	V_{CE} = 40V	—	—	±1	mA
Clamp Diode, V_F	4.4A	—	2.0	2.5	Volts

SWITCHING CHARACTERISTICS (V_S = −20°C to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Source Turn On Delay	t_D on	1.4V $V_{\overline{sig}}$ to 10% V_{source}		300		ns
Source Rise Time	t_R on	V_{source} 10% to 90%		100		ns
Source Fall Time	t_F on	V_{source} 90% to 10%		500		ns
Sink Turn Off Delay	t_D off	1.4V $V_{\overline{sig}}$ to 10% V_{sink}		500		ns
Sink Raise Time	t_R off	V_{sink} 10% to 90%		400		ns
Sense Loop Turn On Delay	t_{DS} on	$V_{TH\ sense\ 1}$ to 50% V_{source}		TBD*		
Sense Loop Turn Off Delay	t_{DS} off	$V_{TH\ sense\ 2}$ to 50% V_{sink}		TBD*		

*To Be Determined

FUNCTIONAL DESCRIPTION

The following discussion assumes an inductive load between the SOURCE and SINK outputs. Current into the INPUT pin directly controls the state of the SINK output. When the INPUT is above 1.4 volts the SINK output will be held low. When the INPUT is below 0.8 volts the SINK output will be off.

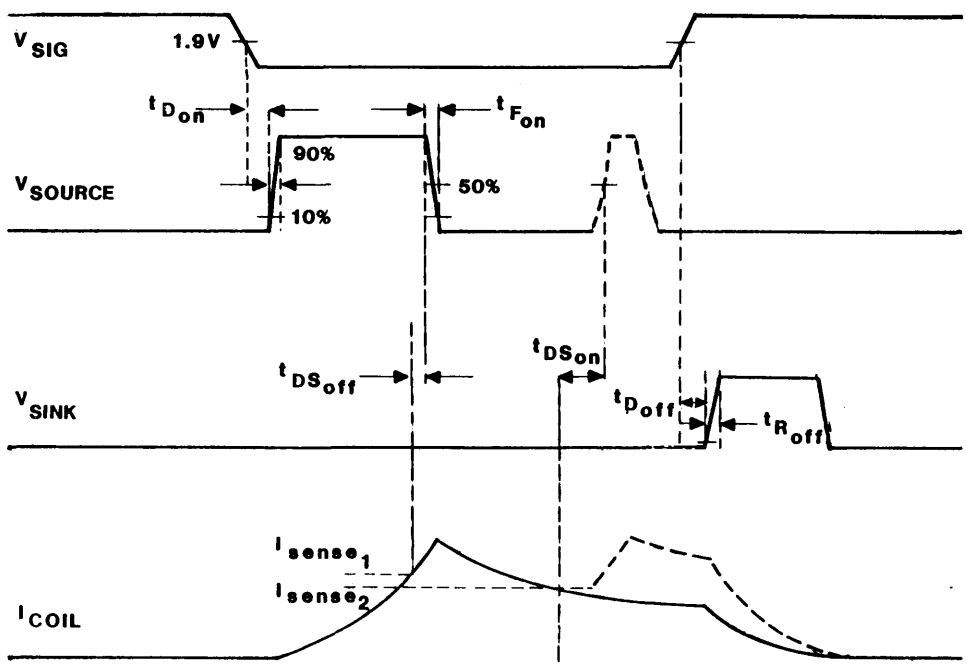
SG3640

The SOURCE output is controlled by the INPUT current and the state of an internal comparator. One input to the comparator is the voltage across the internal sense resistor and the other is a voltage produced by the INPUT current. Initially, when the INPUT goes above the threhold both the SOURCE and SINK transistors are turned on. When current through the sense resistor reaches 500 times the INPUT current the SOURCE will be turned off. Threshold hysteresis of 10% is built into the comparator. When the voltage across the sense resistor falls to the new threshold the SOURCE transistor will again be turned on and the comparator threshold will be raised to its initial state.

SG3641

The SG3641 works in the same manner as the SG3640 except that when the comparator turns the SOURCE transistor off it also sets a flip/flop to inhibit the SOURCE from being turned on until the flip/flop is reset by INPUT going low.

TIMING DIAGRAM



APPLICATIONS

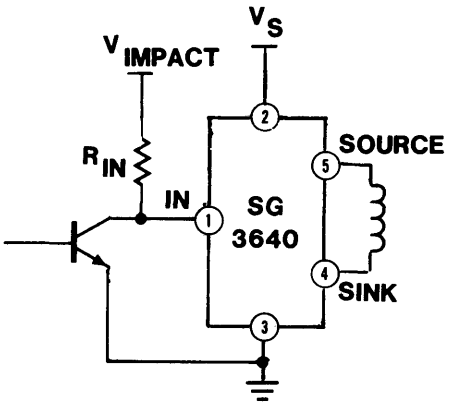


Figure 1

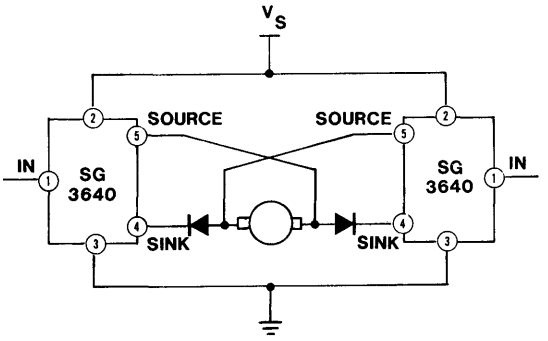


Figure 2

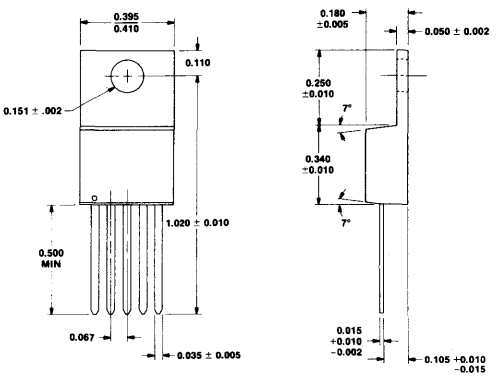
APPLICATIONS

The SG3640 or SG3641 can be used to drive a solenoid as illustrated in Figure 1. R IN and V IMPACT should be chosen to provide input current to the SG 3640 or SG3641 (8 mA will provide 4 Amps of peak SOURCE current). Changing V IMPACT will control the peak current. No external diodes are required.

Two SG3640 or SG3641 devices can be used to drive a motor as illustrated in Figure 2. When used in this way external diodes are required to protect the devices against parasitic diodes which may form in the devices when the source is turned off. These external diodes must be the high speed type with voltage ratings above 70 volts and capable of handling 4Amps. Care should be taken to insure that both INPUTS are not on at the same time. 10 to 20 ms off dead time may be required from the time one INPUT is turned off and the alternate INPUT is turned on.

6

PACKAGE DIMENSIONS



P-Package TO-220

ADVANCED DATA
SG3643/SG3643A

Performance data described herein represent design goals.
Final device specifications are subject to change.

4 AMP SOLENOID AND MOTOR DRIVER

DESCRIPTION

The SG3643 is a high voltage integrated circuit designed to be used as a "H" bridge driver, dual solenoid driver and more. This device allows current control of loads by means of external series sense resistors and a threshold control input. The SG3643 and SG3643A feature built-in thermal protection.

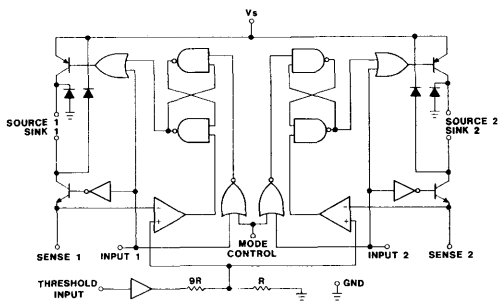
FEATURES

- **Chopped Mode Current Control**
- **Output Current to 4 Amps**
- **60 Volt Output Drivers (A suffix)**
- **TTL compatable INPUT and MODE pins**
- **Combined Threshold and Logic Input**
- **Built-in Thermal Protection**
- **Built-in Clamp Diodes for Inductive Loads**
- **Single Voltage Power Supply Operation**
- **Packaged in a 12 lead power SIP**

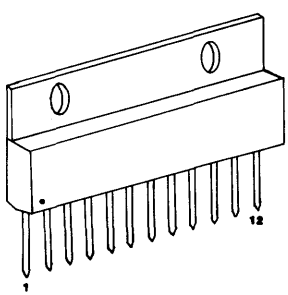
TRUTH TABLE

	Mode	IN	Enable	Sink	Source
	0/1	1	0/1	OFF	OFF
NonChop Mode	0	0	1	ON	ON
	0	0	1	ON	ON
	0	0	0	ON	OFF
	1	0	1	ON	ON
CHOP MODE	1	0	↓	ON	OFF
	1	0	↑	ON	ON

BLOCK DIAGRAM



PIN ASSIGNMENTS



Pin # Function

1 Ground
2 In 1
3 Sense 1
4 Sink 1
5 Source 1
6 Threshold Input
7 V_S
8 Source 2
9 Sink 2
10 Sense 2
11 In 2
12 Mode Control

ORDER INFORMATION

Part Number	*Max Voltage*	*Package*
SG3643S	40V	12 pin SIP
SG3643AS	60V	12 pin SIP

6

ABSOLUTE MAXIMUM RATINGS

Supply Voltage SG3643 SG3643A	45V 60V
Input Voltage Range	0V to 7V
Peak Output Current	±5A
Output Current 33% D.C.	±4.4A

Continuous Output Current	±1A
Package Power Dissipation (average)	4.5 watts
(without heatsink T_A = 25°C) Operating Temperature Range	−20°C to +85° C
Storage Temperature Range	−55°C to +150°C

ELECTRICAL CHARACTERISTICS (V_S = 40V, T_A = −20°C to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Supply Voltage	V_S	operating	15	—	40(60)	volts
Package Power Dissipation		V_S = 40	—	10	—	Watts
Supply Current		V_S = 40	—	12	20	mA
Signal Input Threshold	$V_{\overline{sig}}$		—	1.4	—	volts
Mode Input Threshold	V_{mode}		—	1.4	—	volts
Internal Chopping Threshold	$V_{THE\ chop}$		—	4.0	—	volts
Threshold Input Disable Voltage	$V_{THE\ enable}$		—	0.45	—	volts
Signal Input Current (low)	$I_{\overline{sig}\ L}$	$V_{\overline{sig}}$ = .4V	−1.6	—	—	mA
Signal Input Current (high)	$I_{\overline{sig}\ H}$	$V_{\overline{sig}}$ = 2.4V	—	—	100	μA
Mode Input Current (low)	$I_{mode\ L}$	V_{mode} = .4V	−1.6	—	—	mA
Mode Input Current (high)	$I_{mode\ H}$	V_{mode} = 2.4V	—	—	100	μA
Threshold Input Current (low)	$I_{THE\ L}$	$V_{THE} < V_{THE\ enable}$	—	−6.0	—	μA
Threshold Input Current (high)	$I_{THE\ H}$	$V_{THE} < V_{THE\ enable}$	—	−2.0	—	μA
Internal Hysteresis Current	I_{HYS}		—	.11 peak	—	
External Hysteresis Current	$I_{HYS\ ext}$		140	200	260	μA
Output SAT Voltage sink	$V_{SAT\ sink}$	I_{at} = 4.4A	—	2.0	2.5	volts
Output SAT Voltage source	$V_{SAT\ source}$	I_{out} = −4.4A	—	2.5	3.0	volts
Output SAT Voltage sink	$V_{SAT\ sink}$	I_{out} = 1.0A	—	1.0	1.2	volts
Output SAT Voltage source	$V_{SAT\ source}$	I_{out} = −1.0A	—	1.5	1.8	volts
Output Leakage sink	$I_{OL\ sink}$	V_{CE} = 40V (60)	—	—	1.0	mA
Output Leakage source	$I_{OL\ source}$	V_{CE} = 40V	—	—	1.0	mA
Output Current		30% on	—	+4.0	+4.4	A
Transconductance Tolerance	(note 1)	V_{THE} = 2.0 to 3.6V V_{THE} = 1.0 to 2.0V V_{THE} = 0.6 to 1.0V		−5% −10% −25%	— — —	+ 5% +10% +25%
Clamp Diode Voltage sink	$V_{C\ sink}$	I = 4.4A	—	2.0	2.5	volts
Clamp Diode Voltage source	$V_{C\ source}$	I = 4.4A	—	3.0	3.5	volts
GAIN I_{out} / V_{THE} (R_S)			—	.1		

NOTE (1) Assumes R_S is exactly known. R_S includes parasitic wiring resistances external to the I.C. package in addition to the intended sense resistor.

SWITCHING CHARACTERISTICS (V_S = 20°C to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Source Turn On Delay	t_D on	1.4V $V_{\overline{sig}}$ to 10% V_{source}		300		ns
Source Rise Time	t_R on	V_{source} 10% to 90%		100		ns
Source Fall Time	t_F on	V_{source} 90% to 10%		500		ns
Sink Turn Off Delay	t_D off	1.4V $V_{\overline{sig}}$ to 10% V_{sink}		500		ns
Sink Rise Time	t_R off	V_{sink} 10% to 90%		400		ns
Sense Loop Turn On Delay	t_{DS} on	$V_{TH\ sense\ 1}$ to 50% V_{source}		TBD*		
Sense Loop Turn Off Delay	t_{DS} off	$V_{TH\ sense\ 2}$ to 50% V_{sink}		TBD*		

*To Be Determined

FUNCTIONAL DESCRIPTION

Non-Chop Mode (MODE Pin tied low):
The state of the INPUT pin directly controls the state of the sink transistor. When INPUT (V_{sig}) is high the sink transistor is turned off. When INPUT is low the sink transistor acts as a saturation switch.

The source transistor is directly controlled by a high to the INPUT pin. When INPUT is low the source is controlled by the result of a comparison of the voltage across an external sense resistor and the THRESHOLD INPUT.

With a high on the INPUT, both the output sink and source transistors are turned off which force SENSE to be pulled to ground through an external resistor. This produces a high on the output of the internal comparator and forces the output of the latch to a low state. As INPUT is switched low, both the sink and source transistors are turned on. This causes both the current in a coil, located between the SINK and SOURCE outputs, as wells as the voltage across the sense resistor to rise. When the voltage across the sense resistor reaches one tenth the THRESHOLD INPUT voltage the comparator trips and sets the latch thus turning the source transistor off. The latch is reset when the INPUT returns to a high state.

Chop Mode (MODE pin tied high):
The initial conditions are the same as in the non-chop mode except the latch is disabled and acts as a simple inverter. Both SINK and SOURCE turn on as INPUT goes low. When the voltage across the external sense resistor reaches one tenth the THRESHOLD INPUT voltage the comparator switches turning SOURCE off and causing the voltage across the sense resistor to decay. The tripping of the comparator also turns on a current source (I_{HYS}, typically 200 μA) which is tied to the THRESHOLD INPUT and lowers the threshold by an amount determined by the external impedance at the THRESHOLD INPUT (R_{HYS}). This impedance sets up the externally adjustable hysteresis. When the current decays to the new lower threshold level the comparator trips again turning the SOURCE on and resetting the threshold to its oroiginal value.

Chop Mode Default Hysteresis:
In the Chop Mode, if the THRESHOLD INPUT signal becomes larger than 4 volts (approx.) the output current will no longer increase. At this point the chop hysteresis will switch to an internally controlled value of approximately 10%. This allows the threshold to be left floating and provides a default to the maximum operating current with a 10% hysteresis.

THERMAL AND POWER CHARACTERISTICS

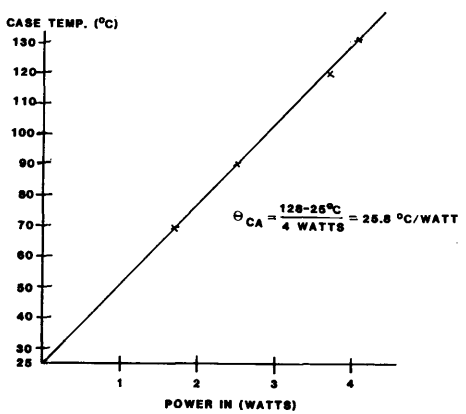


Figure 2 SIP Package Dissipation
(No Air Flow or Heat Sink)

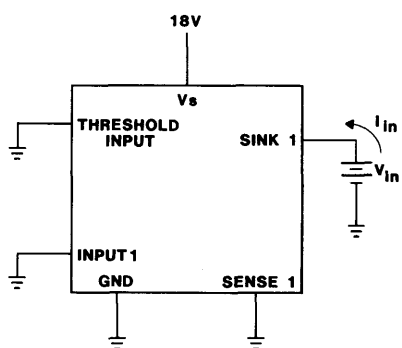


Figure 5 Test Fixture for Thermal Measurements

Thermal Shutdown	T_{JSD} = 160°
Thermal Resistance	Θ_{JA} = 30° C/W (typical)
	Θ_{JC} = 2° C/W (typical)

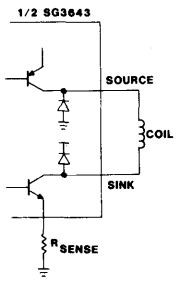


Figure 4

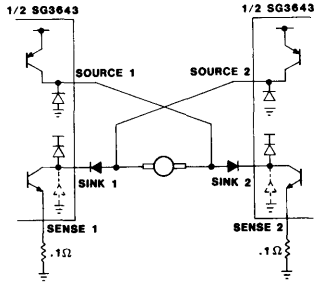


Figure 5

APPLICATIONS

The SG3643 can be used to drive a solenoid as seen in Figure 4. the coil is connected between the collector of the source and the collector of the sink transistors. the internal clamp diodes make this application possible without external diodes.

When driving a motor, both halves of the SG3643 are used in a cross coupled configuration as seen in Figure 5. In this configuration external diodes must be used to isolate an internal paracitic diode. Without these external diodes the device will be damaged. These diodes must be of the high speed type with voltage ratings above 70 volts and capable of handling 4 Amps. Both inputs should not be turned on at the same time.

When in the Chop Mode a resistor (R_{HYS}) in series with the THRESHOLD INPUT and the external circuit which controls the THREHOLD INPUT will set the amount of hysteresis (see the design example).

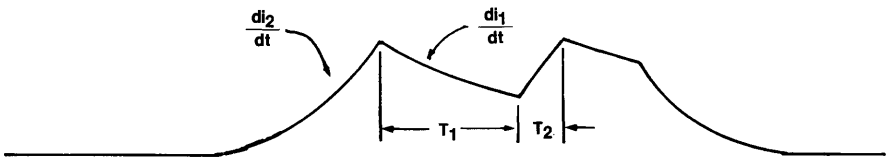
6

CIRCUIT CONSIDERATIONS

PC Board Layout — The output current is controlled by both the voltage at the SENSE pin and the sense resistor. Because of the large currents and low resistances, it is critical to have an extremely good PC board layout to reduce paracitic wiring resistances which could add to the sense resistor and reduce the output current.

Thermal — Because of the large power dissipation usually associated with this device, a heat sink is recommended. Air flow around the package may also reduce package temperature. the device has built in thermal shutdown capabilities which will turn the output off when the substrate reaches a temperature of 140 to 160 degrees C.

DESIGN EXAMPLE — Chop Mode



Desired: A 3.0A Peak, 20KHz chop frequency.

Given: $V_S = 40V, L = 2mh$

Assume: $R_S = .1\Omega$

Procedure: For a 3 Amp Peak and $R_S = .1\Omega$;

1) $V_{sense} = 3(.1) = 300mV$

$V_{threshold} = 10V \cdot V_{sense} = 3V;$

2) $T = T_1 + T_2 = \frac{1}{20KHz}$

$= \frac{I_{HYS}}{2.5A/ms} + \frac{I_{HYS}}{17.5A/ms}$

$T = I_{HYS}\left(\frac{1}{2.5} + \frac{1}{17.5}\right)ms$

$\therefore I_{HYS} = \frac{\frac{1}{20KHz}}{\left(\frac{1}{2.5} + \frac{1}{17.5}\right) \times 10^{-3}} = .109 \text{ Amps}$

3) $\%\ HYS = \frac{I_{HYS}}{I_{peak}} = \frac{.109}{3} = 3.65\%$

$\Delta V_{threshold} = .0365\,(3V) = 109mV$

$R_{HYS} = \frac{\Delta V_{threshold}}{200\mu A} = 547\Omega$

$\frac{d_{i1}}{d_t} = \frac{V_S - 2V_{sat}}{L}$

$= \frac{40 - 2(2.5)}{2}$

$= 17.5A/ms$

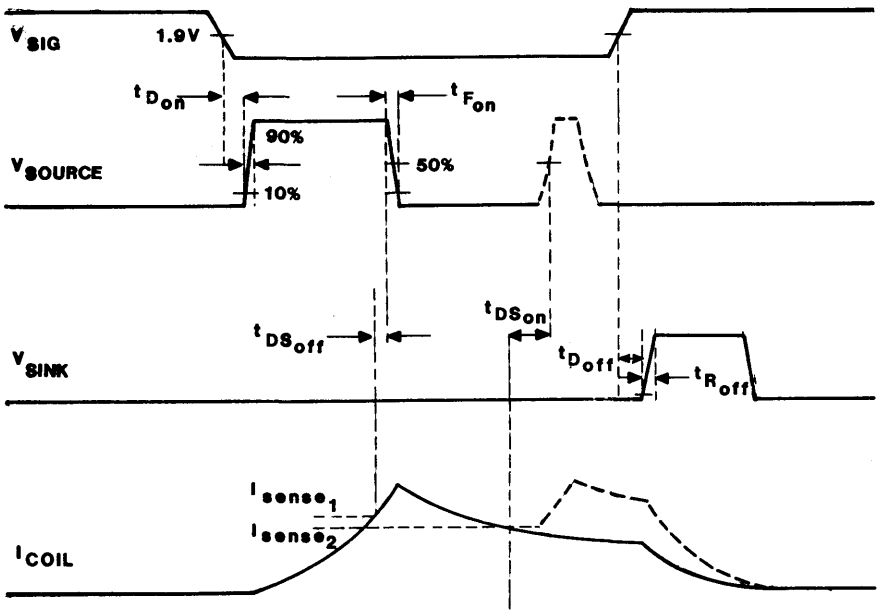
$\frac{d_{i2}}{d_t} = \frac{V_{sat} - V_{c\,1\,amp}}{L}$

$= \frac{2.5 + 2.5}{2}$

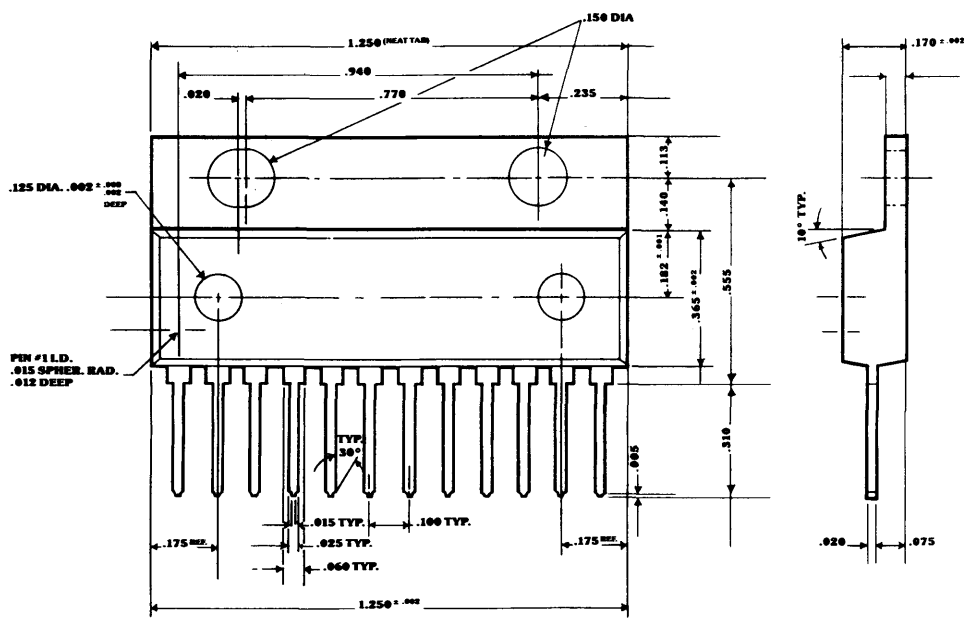
$= 2.5A/ms$

6

TIMING DIAGRAM



PACKAGE DIMENSIONS



DUAL HAMMER DRIVER

DESCRIPTION

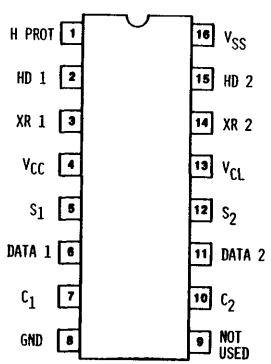
The SG3700 is a monolithic integrated circuit that will provide up to 1 Amp of current to each output. An external sense resistor and an external reference control voltage is required for programming the output current to the desired value. On chip TTL compatible logic is provided for timing of the output current pulse duration.

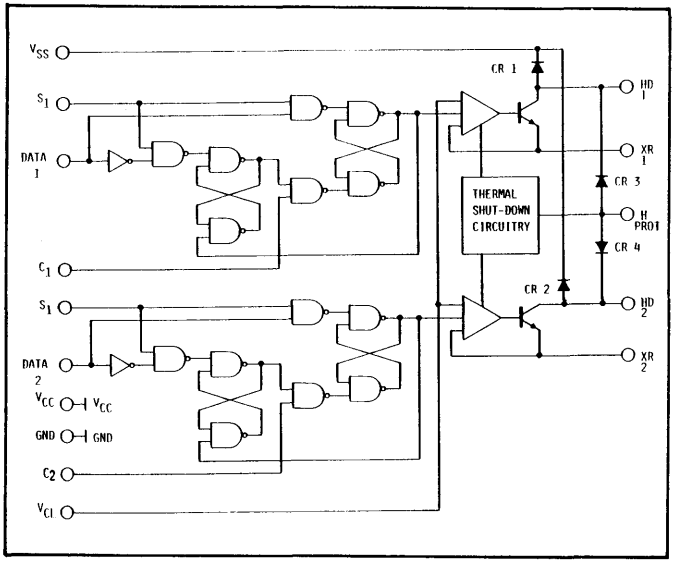
FEATURES:

- Output Currents to 1 Amp
- Output Voltage to 35 Volts
- Built in Clamp Diodes
- Thermal Protection
- Logic Control of Pulse Duration

16-PIN

CONFIGURATION





6

ABSOLUTE MAXIMUM RATINGS

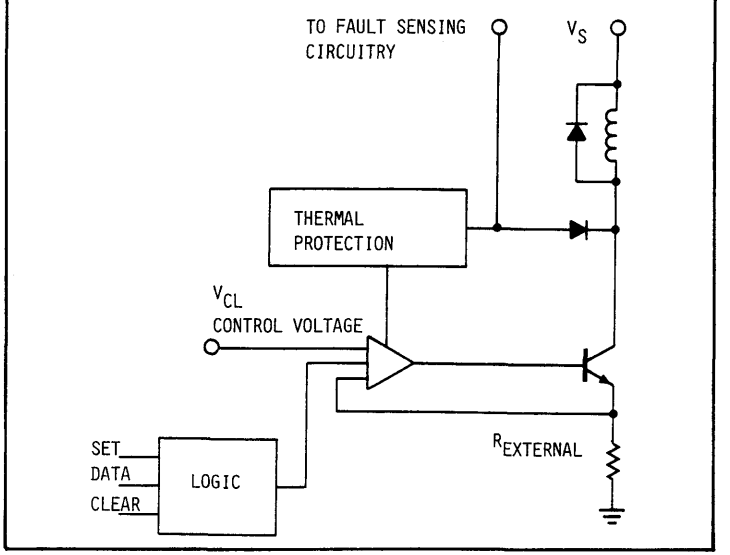
V_{CC} = 7 Volts
V_{in} = 5.5 Volts
V_S = 40 Volts
I_{OUT} = 1 Amp

ELECTRICAL CHARACTERISTICS

Vcc = 5V T = 25°C

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
"0" Input Current	$I_{in}(0)$	Logic inputs Vin = gnd		200		µA
"1" Input Current	$I_{in}(1)$	Logic inputs Vin = gnd		10		µA
"0" Input Voltage	$V_{in}(0)$				0.8	Volts
"1" Input Voltage	$V_{in}(1)$		2.0			Volts
Control Voltage Input Current	I_{cl}	V_{cl} = 1.0 to 1.8 Volts			10	µA
Output Leakage	I_{off}	V_S = 35 Volts			500	µA
V_{fault} Sense Output	$V_{prot.}$	$I_{prot.}$ = 1.5 mA			1.5	Volts
Clamp Diode Forward Voltage	V_F	I_F = 1.0 Amp			3.0	Volts
Clamp Diode Leakage Current	I_R	V_R = 35 Volts			100	µA

TYPICAL APPLICATIONS



POWER OUTPUT STAGES

SWITCHING REGULATOR POWER OUTPUT STAGES

Power Output Stages for 5 Amp Positive and Negative Switching Regulators

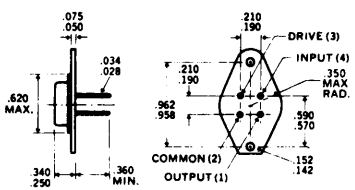
FEATURES

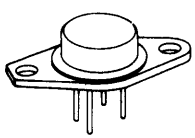
- **Equivalent to the Unitrode PIC 600, 601, 602, 610, 611, 612**
- **Designed and characterized for switching regulator applications**
- **Cost saving design reduces size, improves efficiency, reduces noise and RFI (See note 4)**
- **High operating efficiency, Typical 2A circuit performance —**
  Rise and Fall time < 75ns
  Efficiency > 85%
- **No reverse recovery spike generated by commutating diode. (See note 4 and Fig. 2)**
- **Electrically isolated, 4-Pin, TO-66 hermetic case**

DESCRIPTION

The SM600 series Power Output Stages are designed and characterized to be driven with standard integrated circuit voltage regulators. They are completely characterized over their entire operating range of −55°C to +125°C. The devices are enclosed in a special 4-pin TO-66 package, hermetically sealed for high reliability. The hybrid circuit construction utilizes thick film resistors on a beryllia substrate for maximum thermal conductivity and resultant low thermal impedance. All of the active elements in the hybrid are fully passivated.

MECHANICAL SPECIFICATIONS SM600, 601, 602, 610, 611, 612

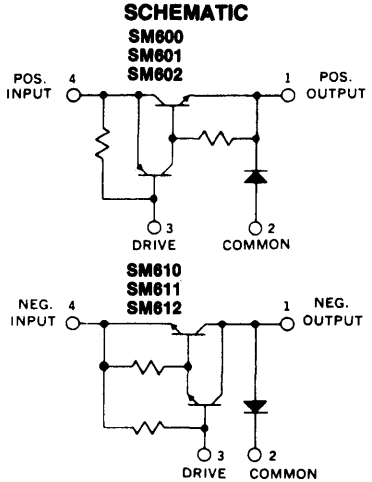




4-Pin TO-66

NOTES:
1. Case is electrically isolated.
2. Loads may be soldered to within 1/16" of base provided temperature-time exposure is less than 260°C for 10 seconds.

SCHEMATIC



600 Series Power Output Stages

ABSOLUTE MAXIMUM RATINGS	SM600	SM601	SM602	SM610	SM611	SM612
Input Voltage, V_{4-2}	60V	80V	100V	−60V	−80V	−100V
Output Voltage, V_{1-2}	60V	80V	100/V	−60V	−80V	−100V
Drive Input Reverse Voltage, V_{3-4}	5V	5V	5V	−5V	−5V	−5V
Output Current, I_1	5A	5A	5A	−5A	−5A	−5A
Drive Current, I_3	−0.2A	−0.2A	−0.2A	0.2A	0.2A	0.2A
Thermal Resistance						
Junction to Case, θ_{J-C} Power Switch						4.0°C/W
Commutating Diode						4.0°C/W
Case to Ambient, θ_{C-A}						60.0°C/W
Operating Temperature Range, T_C						−55°C to +125°C
Maximum Junction Temperature, T_j						+150°
Storage Temperature Range						−65°C to +150°C

ELECTRICAL SPECIFICATIONS (at 25°C unless noted)

Test	Symbol	SM600, 601, 602 Min	Typ	Max	SM610, 611, 612 Min	Typ	Max	Units	Conditions
Current Delay Time	t_{di}	–	20	40	–	20	40	ns	V_{in}=25V(−25V)
Current Rise Time	t_{ri}	–	50	75	–	50	75	ns	V_{out}=5V(−5V)
Voltage Rise Time	t_{rv}	–	30	50	–	30	50	ns	I_{out}=2A(−2A)
Voltage Storage Time	t_{sv}	–	175	500	–	150	700	ns	I_3=−20mA(20mA)
Voltage Fall Time	t_{fv}	–	50	75	–	50	75	ns	See Figure 2.
Current Fall Time	t_{fi}	–	70	150	–	70	150	ns	See notes 1, 2, 4
Efficiency (Notes 2 & 4))	η	–	85	–	–	85	–	%	
On-State Voltage (Note 3)	$V_{4-1(on)}$	–	1.0	1.5	–	−1.0	−1.5	V	I_4=2A(−2A),I_3=−.02A(.02A)
On-State Voltage (Note 3)	$V_{4-1(on)}$	–	2.5	3.5	–	−2.5	−3.5	V	I_4=5A(−5A),I_3=−.02A(.02A)
Diode Forward Voltage (Note 3)	$V_{2-1(on)}$	–	.8	1.0	–	−.8	−1.0	V	I_2=2A(−2A)
Diode Forward Voltage (Note 3)	$V_{2-1(on)}$	–	1.0	1.5	–	−1.0	−1.5	V	I_2=5A(−5A)
Off-State Current	I_{4-1}	–	0.1	10	–	−0.1	−10	μA	V_4=Rated input voltage
Off-State Current	I_{4-1}	–	.10	1.0		−.10	1.0	mA	V_4 = Rated input volt.,T_A = 100°C
Diode Reverse Current	I_{1-2}	–	1.0	10	–	−1.0	−10	μA	V_1=Rated output voltage
Diode Reverse Current	1_{1-2}	+	.500	1.0	–	.500	1.0	mA	V_1=Rated output volt., T_A=100°C

Notes:

1. In switching an inductive load, the current will lead the voltage on turn-on and lag the voltage on turn-off (see Figure 2). Therefore, Voltage Delay Time (t_{DV}) ≅ t_{di} + t_{ri} and Current Storage Time (t_{si}) ≅ t_{sv} + t_{fv}.
2. The efficiency is a measure of internal power losses and is equal to Output Power divided by Input Power. The switching speed circuit of Figure 1, in which the efficiency is measured, is representative of typical operating conditions for the SM600 series switching regulators.
3. Pulse test: Duration = 300ms, Duty Cycle ≤ 2%.
4. As can be seen from the switching waveforms shown in Figure 2, no reverse or forward recovery spike is generated by the commutating diode during switching! This reduces self-generated noise, so no current spike is fed through the switching regulator. It also improves efficiency and reliability, since the power only carries current during turn-on.

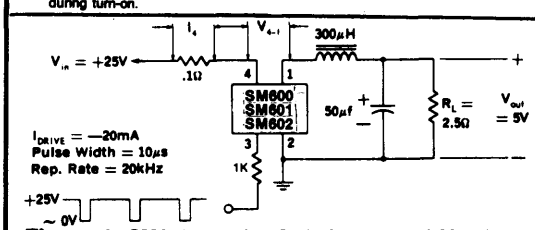


Figure 1. SM600, 601, 602 Switching Speed Circuit

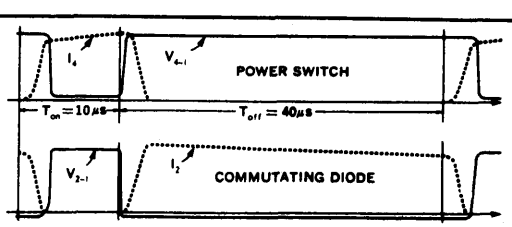


Figure 2. SM600, 601, 602 Switching Waveforms

Note: SM610, 611, 612 Test Circuit and waveforms are identical but of opposite polarity (V_{in} = −25V, V_{out} = −5V, I_{DRIVE} = +20mA).

SWITCHING REGULATOR POWER OUTPUT STAGES

Power Output Stages for 15 Amp Positive and Negative Switching Regulators

FEATURES

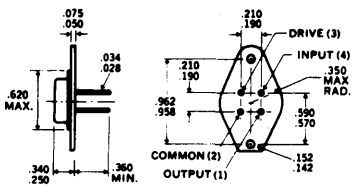
- **Equivalent to PIC 625, 626, 627, 635, 636, 637**
- **Designed and characterized for switching regulator applications**
- **Cost saving design reduces size, improves efficiency, reduces noise and RFI (See note 4)**
- **High operating frequency (to > 100kHz) results in smaller inductor-capacitor filter and improved power supply response time**
- **High operating efficiency: Typical 7A circuit performance —**
  Rise and Fall time < 300ns
  Efficiency > 85%
- **Electrically isolated, 4-pin, TO-66 hermetic case**

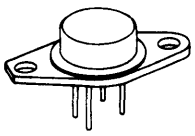
DESCRIPTION

The SM600 series Power Output stages are designed and characterized to be driven with standard integrated circuit voltage regulators. They are completely characterized over their entire operating range of −55°C to +125°C. The devices are enclosed in a special 4-pin TO-66 package, hermetically sealed for high reliability. The hybrid circuit construction utilizes thick film resistors on a beryllia substrate for maximum thermal conductivity and resultant low thermal impedance. All of the active elements in the hybrid are fully passivated.

7

MECHANICAL SPECIFICATIONS SM625, 626, 627, 635, 636, 637

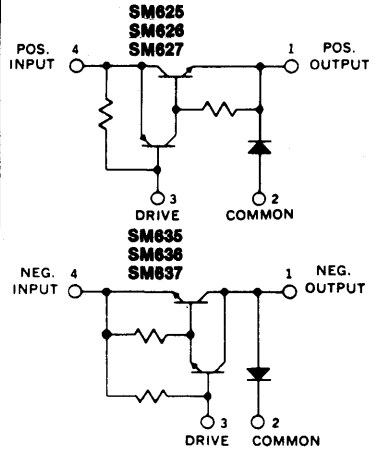




4-Pin TO-66

NOTES:
1. Case is electrically isolated.
2. Loads may be soldered to within 1/16" of base provided temeperature-time exposure is less than 260°C for 10 seconds.

SCHEMATIC



600 Series Power Output Stages

ABSOLUTE MAXIMUM RATINGS	SM625	SM626	SM627	SM635	SM636	SM637
Input Voltage, V_{4-2}	60V	80V	100V	−60V	−80V	−100V
Output Voltage, V_{1-2}	60V	80V	100/V	−60V	−80V	−100V
Drive Input Reverse Voltage, V_{3-4}	5V	5V	5V	−5V	−5V	−5V
Output Current, I_1	15A	15A	15A	−15A	−15A	−15A
Drive Current, I_3	−0.4A	−0.4A	−0.4A	0.4A	0.4A	0.4A

Thermal Resistance	
Junction to Case, Θ_{J-C}	
Power Switch	4.0°C/W
Commutating Diode	4.0°C/W
Case to Ambient, θ_{C-A}	60.0°C/W
Operating Temperature Range, T_C	−55°C to +125°C
Maximum Junction Temperature, T_j	+150°C
Storage Temperature Range	−65°C to +150°C

ELECTRICAL SPECIFICATIONS (at 25°C unless noted)

Test	Symbol	SM625/625/627 Min.	Typ.	Max.	SM635/636/637 Min.	Typ.	Max.	Units	Conditions
Current Delay Time	t_{di}	–	35	60	–	35	60	ns	V_{in}=25V(−25V)
Current Rise Time	t_{ri}	–	65	150	–	65	175	ns	V_{out}=5V(−5V)
Voltage Rise Time	t_{rv}	–	40	60	–	40	60	ns	I_{out}=7A(−7A)
Voltage Storage Time	t_{sv}	–	500	1000	–	500	1000	ns	I_3=−30mA(30mA)
Voltage Fall Time	t_{fv}	–	70	175	–	100	300	ns	See Figure 2
Current Fall Time	t_{fi}	–	175	300	–	175	300	ns	See notes 1, 2, 4
Efficiency (Notes 2 and 4)	η	–	85	–	–	85	–	%	
On-State Voltage (Note 3)	$V_{4-1(on)}$	–	1.0	1.5	–	−1.0	−1.5	V	I_4=7A(−7A), I_3=−.03A(.03A)
On-State Voltage (Note 3)	$V_{4-1(on)}$	–	2.5	3.5	–	−2.5	−3.5	V	I_4=15A(−15A), I_3=−.03A(.03A)
Diode Fwd, Voltage (Note 3)	$V_{2-1(on)}$	–	.85	1.25	–	−.85	−1.25	V	I_2=7A(−7A)
Diode Fwd. Voltage (Note 3)	$V_{2-1(on)}$	–	.95	1.75	–	−.95	−1.75	V	I_2=15A(−15A)
Off-State Current	I_{4-1}	–	0.1	10	–	−0.1	−10	μA	V_4=Rated input voltage
Off-State Current	I_{4-1}	–	.10	1.0	–	−.10	1.0	mA	V_4=Rated input voltage, T_A=100°C
Diode Reverse Current	I_{1-2}	–	1.0	10	–	−1.0	−10	μA	V_1=Rated output voltage
Diode Reverse Current	I_{1-2}	–	.500	1.0	–	.500	1.0	mA	V_1=Rated output voltage, T_A=100°C

Notes:
1. In switching an inductive load, the current will lead the voltage on turn-on and lag the voltage on turn-off (see **Figure 2**). Therefore, Voltage Delay Time (t_{DV}) ≅ t_{di} + t_{ri} and Current Storage Time (t_{si}) ≅ t_{sv} + t_{fv}.
2. The efficiency is a measure of internal power losses and is equal to Output Power divided by Input Power. The switching speed circuit of Figure 1, in which the efficiency is measured, is representative of typical operating conditions for the **SM600 series switching regulators.**
3. Pulse Test: Duration = 300ms, Duty Cycle ≤ 2%.
4. As can be seen from the switching waveforms shown in Figure 2, no reverse or forward recovery spike is generated by the commutating diode during switching! This reduces self-generated noise, since no current spike is fed through the switching regulator. It also improved efficiency and reliability, since the power switch only carries current during turn-on.

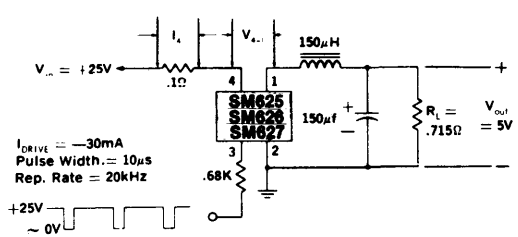


Figure 1. SM625, 626, 627 Switching Speed Circuit

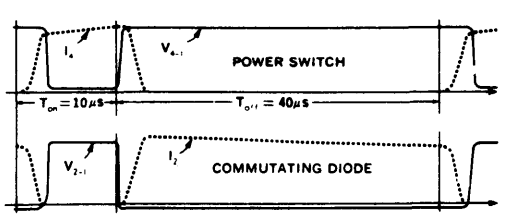


Figure 2. SM625, 626, 627 Switching Waveforms

Note: SM635, 636, 637 Circuit and waveforms are identical but of opposite polarity (V_{in} = −25V, V_{out} = −5V, I_{DRIVE} = +30mA).

SWITCHING REGULATOR POWER OUTPUT STAGES

Power Output Stages for 15 Amp Positive and Negative Switching Regulators

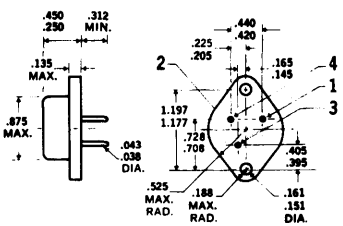
FEATURES

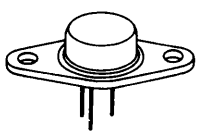
- **Equivalent to the Unitrode PIC 645, 646, 647, 655, 656, 657**
- **Cost saving design reduces size, improves efficiency, reduces noise and RFI (See note 4)**
- **High operating frequency (to > 100kHz) results in smaller inductor-capacitor filter and improved power supply response time**
- **High operating efficiency: Typical 7A circuit performance —**
  Rise and Fall time < 300ns
  Efficiency > 85%

DESCRIPTION

The SM600 series Power Output stages are designed and characterized to be driven with standard integrated circuit voltage regulators. They are completely characterized over their entire operating range of −55°C to + 125°C. The devices are enclosed in a special 3-pin TO-3 package, hermetically sealed for high reliability. The hybrid circuit construction utilizes thick film resistors on a beryllia substrate for maximum thermal conductivity and resultant low thermal impedance. All of the active elements in the hybrid are fully passivated.

MECHANICAL SPECIFICATIONS SM645, 646, 647, 655, 656, 657

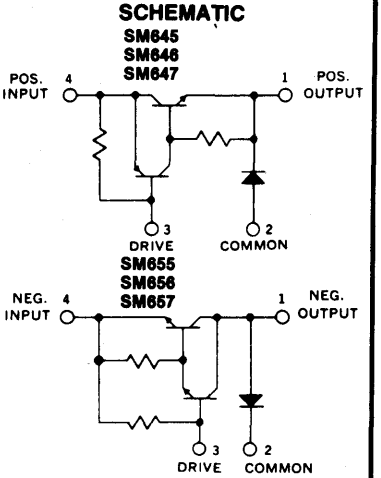




3-Pin TO-3

NOTE:
Loads may be soldered to within 1/16" of base provided temperature-time exposure is less than 260°C for 10 seconds.

SCHEMATIC



600 Series Power Output Stages

ABSOLUTE MAXIMUM RATINGS	SM645	SM646	SM647	SM655	SM656	SM657
Input Voltage, V_{4-2}	60V	80V	100V	−60V	−80V	−100V
Output Voltage, V_{1-2}	60V	80V	100/V	−60V	−80V	−100V
Drive Input Reverse Voltage, V_{3-4}	5V	5V	5V	−5V	−5V	−5V
Continuous Output Current, I_1	15A	15A	15A	−15A	−15A	−15A
Peak Output Current	20A	20A	20A	−20A	−20.A	−20.A
Drive Current, I_3	−0.4A	−0.4A	−0.4A	0.4A	0.4A	0.4A

Thermal Resistance

Junction to Case, θ_{J-C} Power Switch	2°C/W
Commutating Diode	2°C/W
Case to Ambient, θ_{C-A}	30.0°C/W
Operating Temperature Range, T_C	−55°C to +125°C
Maximum Junction Temperature, T_j	+150°C
Storage Temperature Range	−65°C to +150°C

ELECTRICAL SPECIFICATIONS (at 25°C unless noted)

Test	Symbol	SM645/646/647 Min.	Typ.	Max.	SM655/656/657 Min.	Typ.	Max.	Units	Conditions
Current Delay Time	t_{di}	–	35	60	–	35	60	ns	V_{in}=25V(−25V)
Current Rise Time	t_{ri}	–	65	150	–	65	175	ns	V_{out}=5V(−5V)
Voltage Rise Time	t_{rv}	–	40	60	–	40	60	ns	I_{out}=7A(−7A)
Voltage Storage Time	t_{sv}	–	500	1000	–	500	1000	ns	I_3=−30mA(30mA)
Voltage Fall Time	t_{fv}	–	70	175	–	100	300	ns	See Figure 2
Current Fall Time	t_{fi}	–	175	300	–	175	300	ns	See notes 1, 2, 4
Efficiency (Notes 2 and 4)	η	–	85	–	–	85	–	%	
On-State Voltage (Note 3)	$V_{4-1(on)}$	–	1.0	1.5	–	−1.0	−1.5	V	I_4=7A(−7A), I_3=−.03A(.03A)
On-State Voltage (Note 3)	$V_{4-1(on)}$	–	2.5	3.5	–	−2.5	−3.5	V	I_4=15A(−15A), I_3=−.03A(.03A)
Diode Fwd, Voltage (Note 3)	$V_{2-1(on)}$	–	.85	1.25	–	−.85	−1.25	V	I_2=7A(−7A)
Diode Fwd. Voltage (Note 3)	$V_{2-1(on)}$	–	.95	1.75	–	−.95	−1.75	V	I_2=15A(−15A)
Off-State Current	I_{4-1}	–	0.1	10	–	−0.1	−10	μA	V_4=Rated input voltage
Off-State Current	I_{4-1}	–	.10	1.0	–	−.10	1.0	mA	V_4=Rated input voltage, T_A=100°C
Diode Reverse Current	I_{1-2}	–	1.0	10	–	−1.0	−10	μA	V_1=Rated output voltage
Diode Reverse Current	I_{1-2}	–	.500	1.0	–	.500	1.0	mA	V_1=Rated output voltage, T_A=100°C

Notes:
1. In switching an inductive load, the current will lead the voltage on turn-on and lag the voltage on turn-off (see Figure 2). Therefore, Voltage Delay Time (t_{DV})≅t_{di} + t_{ri} and Current Storage Time (t_{si})≅t_{sv} + t_{fv}.
2. The efficiency is a measure of internal power losses and is equal to Output Power divided by Input Power. The switching speed circuit of Figure 1, in which the efficiency is measured, is representative of typical operating conditions for the SM600 series switching regulators.
3. Pulse Test: Duration = 300ms, Duty Cycle ≤ 2%.
4. As can be seen from the switching waveforms shown in Figure 2, no reverse or forward recovery spike is generated by the commutating diode during switching! This reduces self-generated noise, since no current spike is fed through the switching regulator. It also improved efficiency and reliability, since the power switch only carries current during turn-on.

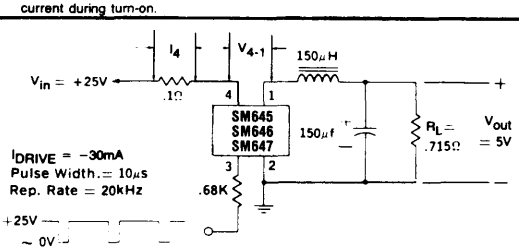


Figure 1. SM645, 646, 647 Switching Speed Circuit

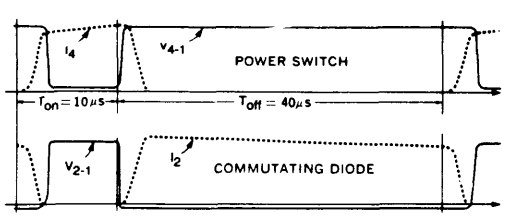


Figure 2. SM645, 646, 647 Switching Waveforms

Note: SM655, 656, 657 Circuit and waveforms are identical but of opposite polarity (V_{in} = −25V, V_{out} = −5V, I_{DRIVE} = −30mA).

SILICON GENERAL INC.
11651 Monarch Street, Garden Grove, California 92641 • 714/892-5531 • TWX: 910-596-1804

SPECIFICATION HRT 600-1

HYBRID SWITCHING REGULATORS
HIGH RELIABILITY TYPES
(4 LEAD TO-66)

SM600A,B/SM601A,B/SM602A,B
SM610A,B/SM611A,B/SM612A,B
SM625A,B/SM626A,B/SM627A,B
SM635A,B/SM636A,B/SM637A,B

CONTENTS

JANUARY 1984

Standard Type	High Rel Construction with T_1 Testing	High Rel Construction with T_2 Testing
SM600	SM600B	SM600A
SM601	SM601B	SM601A
SM602	SM602B	SM602A
SM610	SM610B	SM610A
SM611	SM611B	SM611A
SM612	SM612B	SM612A
SM625	SM625B	SM625A
SM626	SM626B	SM626A
SM627	SM627B	SM627A
SM635	SM635B	SM635A
SM636	SM636B	SM636A
SM637	SM637B	SM637A

1.0 SCOPE

This specification defines the detail requirements for High Reliability Hybrid Switching Regulators. (Reference MIL-STD-750). Extensive 100% testing for parameter stability has been included in the Quality Assurance Provisions.

1.1a ABSOLUTE MAXIMUM RATINGS

	SM600	SM601	SM602	SM610	SM611	SM612
Input Voltage, V_{4-2}	60V	80V	100V	−60V	−60V	−100V
Output Voltage, V_{1-2}	60V	80V	100V	−60V	−80V	−100V
Drive-Input Reverse Voltage, V_{3-4}	5V	5V	5V	−5V	−5V	−5V
Output Current, I_1	5A	5A	5A	−5A	−5A	−5A
Drive Current, I_3	−0.2A	−0.2A	−0.2A	0.2A	0.2A	0.2A
Thermal Resistance						
Junction to Case, θ_{J-C}						
Power Switch	4.0°C/W					
Commutating Diode	4.0°C/W					
Case to Ambient, θ_{C-A}	60.0°					
Operating Temperature Range, T_C	−55°C to +125°C					
Maximum Junction Temperature, T_j	+150°C					
Storage Temperature Range	−65°C to +150°C					

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1.1b ABSOLUTE MAXIMUM RATINGS

	SM625	SM626	SM627	SM610	SM611	SM612
Input Voltage, V_{4-2}	60V	80V	100V	−60V	−60V	−100V
Output Voltage, V_{1-2}	60V	80V	100V	−60V	−80V	−100V
Drive-Input Reverse Voltage, V_{3-4}	5V	5V	5V	−5V	−5V	−5V
Output Current, I_1	15A	15A	15A	−15A	−15A	−15A
Drive Current, I_3	−0.4A	−0.4A	−0.4A	0.4A	0.4A	0.4A
Thermal Resistance						
Junction to Case, θ_{J-C}						
Power Switch	4.0°C/W					
Commutating Diode	4.0°C/W					
Case to Ambient, θ_{C-A}	60.0°					
Operating Temperature Range, T_C	−55°C to +125°C					
Maximum Junction Temperature, T_j	+150°C					
Storage Temperature Range	−65°C to +150°C					

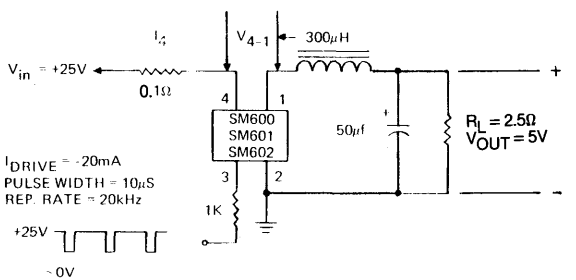
1.1c ELECTRICAL SPECIFICATIONS (at 25°C unless noted)

	Test	Symbol	SM600, 601 AND 602 Min.	Typ.	Max.	SM610, 611 AND 612 Min.	Typ.	Max.	Units	Conditions
1	Current Delay Time ($I_3 - I_4$)	t_{di}	–	20	40	–	20	40	ns	V_{in} = 25V (-25V)
2	Current Rise Time (I_4)	t_{ri}	–	50	75	–	50	75	ns	V_{out} = 5V (-5V)
3	Voltage Rise Time (V_{4-1})	t_{rv}	–	30	50	–	30	50	ns	I_{out} = 2A (-2A)
4	Voltage Storage Time ($V_{4-1} - I_3$)	t_{sv}	–	700	–	–	700	–	ns	I_3 = -20 mA (20 mA)
5	Voltage Fall Time (V_{4-1})	t_{fv}	–	50	75	–	50	75	ns	
6	Current Fall Time (I_4)	t_{fi}	–	70	150	–	70	150	ns	
7	Efficiency (Note 1)	η	–	85	–	–	85	–	%	
8	On-State Voltage (Note 2)	V_{4-1} (on)	–	1.0	1.5	–	-1.0	-1.5	V	I_4 = 2A (-2A), I_3 = -0.02A (0.02A)
9	On-State Voltage (Note 2)	V_{4-1} (on)	–	2.5	3.5	–	-2.5	-3.5	V	I_4 = 5A (-5A), I_3 = -0.02A (0.02A)
10	Diode Forward Voltage (Note 2)	V_{2-1} (on)	–	0.8	1.0	–	-0.8	-1.0	V	I_2 = 2A (-2A)
11	Diode Forward Voltage (Note 2)	V_{2-1} (on)	–	1.0	1.5	–	-1.0	-1.5	V	I_2 = 5A (-5A)
12	Off-State Current	I_{4-1}	–	0.1	10.0	–	-0.1	-10.0	μA	V_4 = Rated input voltage
13	Off-State Current	I_{4-1}	–	0.01	1.0	–	-0.1	- 1.0	mA	V_4 = Rated input voltage, T_A = 100°C
14	Diode Reverse Current	I_{1-2}	–	1.0	10.0	–	-1.0	-10.0	μA	V_1 = Rated output voltage
15	Diode Reverse Current	I_{1-2}	–	0.5	1.0	–	0.5	- 1.0	mA	V_1 = Rated output voltage, T_A = 100°C

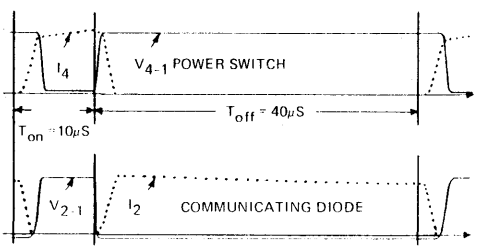
	Test	Symbol	SM625, 626 AND 627 Min.	Typ.	Max.	SM635, 636 AND 637 Min.	Typ.	Max.	Units	Conditions
1	Current Delay Time ($I_3 - I_4$)	t_{di}	–	35	60	–	35	60	ns	V_{in} = 25V (-25V)
2	Current Rise Time (I_4)	t_{ri}	–	65	150	–	65	175	ns	V_{out} = 5V (-5V)
3	Voltage Rise Time (V_{4-1})	t_{rv}	–	40	60	–	40	60	ns	I_{out} = 7A (-7A)
4	Voltage Storage Time ($V_{4-1} - I_3$)	t_{sv}	–	900	–	–	900	–	ns	I_3 = -30 mA (30 mA)
5	Voltage Fall Time (V_{4-1})	t_{fv}	–	70	175	–	100	300	ns	
6	Current Fall Time (I_4)	t_{fi}	–	175	300	–	175	300	ns	
7	Efficiency (Note 1)	η	–	85	–	–	85	–	%	
8	On-State Voltage (Note 2)	V_{4-1} (on)	–	1.0	1.5	–	-1.0	-1.5	V	I_4 = 7A (-7A), I_3 = -0.03A (0.03A)
9	On-State Voltage (Note 2)	V_{4-1} (on)	–	2.5	3.5	–	-2.5	-3.5	V	I_4 = 15A (-15A), I_3 = -0.03A (0.03A)
10	Diode Forward Voltage (Note 2)	V_{2-1} (on)	–	0.85	1.25	–	-0.85	-1.25	V	I_2 = 7A (-7A)
11	Diode Forward Voltage (Note 2)	V_{2-1} (on)	–	0.95	1.75	–	-0.95	-1.75	V	I_2 = 15A (-15A)
12	Off-State Current	I_{4-1}	–	0.1	10.0	–	-0.1	-10.0	μA	V_4 = Rated input voltage
13	Off-State Current	I_{4-1}	–	0.01	1.0	–	-0.1	-1.0	mA	V_4 = Rated input voltage, T_A = 100°C
14	Diode Reverse Current	I_{1-2}	–	1.0	10.0	–	-1.0	-10.0	μA	V_1 = Rated output voltage
15	Diode Reverse Current	I_{1-2}	–	0.5	1.0	–	–0.5	-1.0	mA	V_1 = Rated output voltage, T_A = 100°C

Notes:

1. The efficiency is a measure of internal power losses and is equal to Output Power divided by Input Power. The switching speed circuit of Figure 1, in which the efficiency is measured, is representative of typical operating conditions for the SM600 series switching regulators.
2. Pulse test: Duration = 300μs, Duty Cycle ≤2%, 25°C.



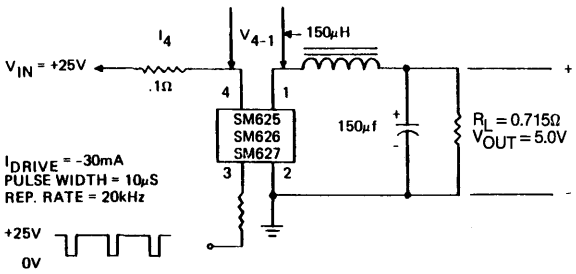
SM600, 601, 602 Switching Speed Circuit



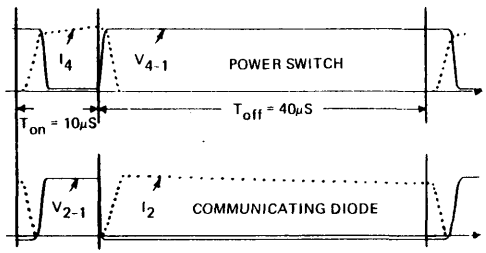
SM600, 601, 602 Switching Waveforms

Note: SM610, 611, 612 Test Circuit and waveforms are identical but of opposite polarity (V_{in} = -25V, V_{out} = -5V, I_{DRIVE} = +20mA).

Figure 1a



SM625, 626, 627 Switching Speed Circuit

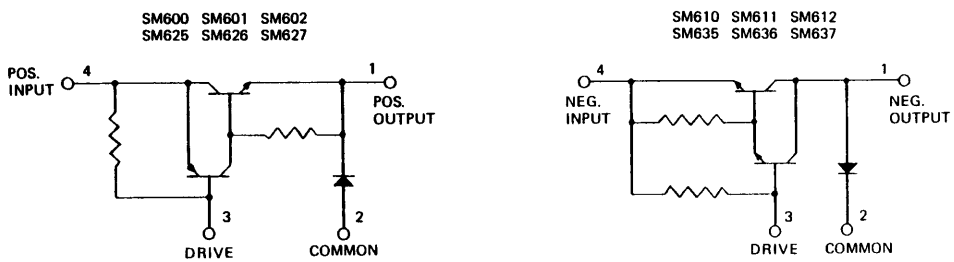


SM625, 626, 627 Switching Waveforms

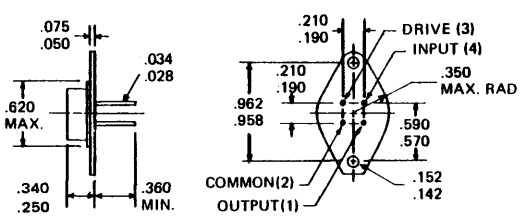
Note: SM635, 636, 637 Circuit and waveforms are identical but of opposite polarity (V_{in} = -25V, V_{out} = -5V, I_{DRIVE} = +30mA.

Figure 1b

SCHEMATIC



MECHANICAL SPECIFICATION



NOTES:
1. Case is electrically isolated.
2. Loads may be soldered to within $^1/_{16}$" of base provided temperature-time exposure is less than 260°C for 10 seconds.

4-Pin TO-66

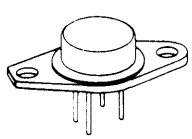


Figure 2. Physical Dimensions and Biasing Diagrams

2.0 APPLICABLE DOCUMENTS

The following documents of the issue in effect on the date of invitations for bids, form a part of this specification to the extent specified herein.

MIL-S-19500 – General Specification for Semiconductor Devices

MIL-S-19491 – Preparation for Delivery of Semiconductor Devices

3.0 Requirements

3.1 Design and Construction

The Hybrid devices supplied under this specification shall have a design and construction such that they will meet all of the requirements specified herein. The dimensions and physical characteristics shall be as specified in Figure 2.

3.2 Performance Characteristics

The performance characteristics of the Hybrid device supplied under this specification shall be as specified in Group A inspection defined in Table I.

3.3 Quality Assurance

The Quality Assurance Provisions shall be as defined in paragraph 4.0.

3.4 Test Methods

Test methods shall be as specified herein.

3.5 Marking

The markings on the devices supplied shall be permanent and legible and shall include the Manufacturer's name or trademark, a Manufacturing Date Code in accordance with MIL-S-19500 and the specific device type number.

3.6 Preparation for Delivery

The Hybrid devices supplied under this specification shall be preapred for delivery in accordance with level C of MIL-S-19491 unless otherwise directed in the specific contract or purchase order.

3.7 Ordering Data

Procurement document should specify the following:

a. Specific item type number
b. Number and date of this specification
c. Quality Assurance Test level required
d. Any special packaging if required

4.0 QUALITY ASSURANCE PROVISIONS

4.1 General Provisions

4.1.1 Inspection Responsibility – The supplier is responsible for the performance of all inspection requirements and acceptability of results as specified herein for the Test Level identified in the contract or purchase order.

4.1.2 Controlled Manufacturer – The devices supplied under this specification shall be manufactured under controlled conditions using formally defined quality assurance methods and systems.

4.1.3 Manufacturing Traceability – Each device supplied under this specification shall be traceable to a specific process group, to permit tracing of its full manufacturing history. Process group records shall indicate the exact date that each manufacturing operation was performed and identify materials and process procedures which were used. The manufacturer shall keep these records on file for at least five years.

4.1.4 Definitions

4.1.4.1 Inspection Lot – An "inspection lot" is a collection of devices from which a sample is withdrawn and inspected to determine compliance with the acceptability criterion. It shall consist of one or more "inspection sublots" of the device types defined in this specification. The maximum inspection lot size shall be 5000 units.

4.1.4.2 Inspection Sublot – An "inspection sublot" shall consist of a collection of devices of a single type which have been manufactured under the same conditions and with the same materials.

4.1.4.3 Shipment Lot – A "shipment lot" shall consist of devices taken from an accepted inspection lot for the purpose of shipment on a specific contract or order.

4.1.4.4 Group A Inspection – Group A inspection shall consist of the examinations and tests specified in Table I, and shall be performed on a sublot basis.

4.1.4.5 Controlled Inventory – The controlled inventory shall consist of lots which have successfully passed the acceptance inspection and are being held in storage prior to actual shipment. A controlled inventory shall have adequate safeguards to insure that no defective or untested devices can be included in it. It shall be accessible only to those individuals who are formally identified as authorized personnel.

4.2 Acceptance Inspection

The acceptance inspection requirements shall be as defined by the applicable test level. The procedures of MIL-S-19500 shall apply to Group A inspection. Inspection lots which have been inspected and accepted shall be kept in a controlled inventory. Shipment lots shall be formed using devices taken from accepted inspection lots.

4.2.1 Test Level T2 Requirements – Test level T2 shall consist of the following requirements.

4.2.1.1 The supplier shall perform the Parameter Stability Testing defined in paragraph 4.3 on each device to be supplied. Prior to starting the Blocking Stability test defined in paragraph 4.3.6, each device shall be serialized for individual identity. Variables test data for the controlled electrical parameters shall be recorded before and after stressing. The same procedure shall apply for the Power Stress stability test defined in paragraph 4.3.8.

4.2.1.2 The supplier shall perform the Group A inspections in accordance with the defined LTPD requirements on each inspection sublot. Electrical parameter testing as specified shall be performed by variables with test data recorded.

4.2.1.3 With each shipment lot, the supplier shall provide a Certificate of Compliance to test level T2 of this specification.

4.2.2 Test Level T1 Requirements – Test level T1 shall consist of the following requirements.

4.2.2.1 The supplier shall perform the Parameter Stability Testing defined in paragraph 4.3 on each device to be supplied. Electrical parameter testing as specified shall be performed by attributes.

4.2.2.2 The supplier shall perform the Group A inspections in accordance with the defined LTPD requirements on each inspection sublot. Electrical parameter testing as specified shall be performed by attributes with test data recorded.

4.2.2.3 With each shipment lot, the supplier shall provide a Certification of Compliance to test level T1 of this specification.

4.3 Parameter Stability Tests

Each Hybrid device is to be supplied under this specification and shall receive the following tests in addition to other standard testing performed by the manufacturer.

4.3.1 Hermetic Seal Test – Fine Leak – Each Hybrid device shall be tested for a case leakage rate of 1×10^{-8} cc/sec or smaller using a helium mass spectrometer or equivalent method. Devices with a case leakage rate greater than specified shall be removed from the lot.

4.3.2 Hermetic Seal Test – Gross Leak – Each Hybrid device shall be tested for gross leaks using fluorocarbon gross leak test or equivalent method. Devices with any indication of case leakage shall be removed from the lot.

4.3.3 Temperature Storage – Each Hybrid device shall be subjected, in a non-operating state, to a temperature of 150°C for a minimum period of 48 hours.

4.3.4 Temperature Cycling – Each Hybrid device shall be temperature cycled from -55°C to 150°C for a minimum of 10 cycles. Each cycle shall consist of at least 15 minutes at each temperature extreme with a maximum transition time of 5 minutes between each temperature extreme.

4.3.4 Reverse Bias Clamp Inductive Test –

V_{CEO} = Rated Input Voltage
I_C = 5A, f = 25 kHz, E_{out} = 5V
T_C = 25°C, see Figure 4

4.3.6 High Temperature Reverse Bias – Each Hybrid device will be high temperature reversed biased in the circuit shown in Figure 3. The conditions of this test are as follows:

T_A = +125°C
Time = 16 hours $^{+8}_{-0}$ hours

Circuit and voltages as shown in Figure 3.

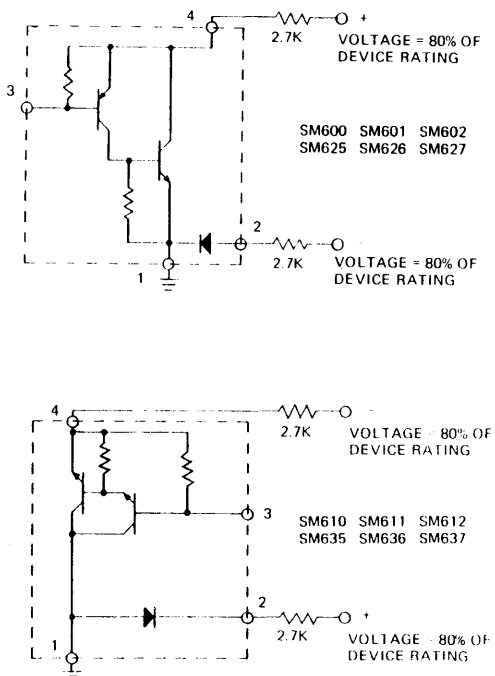


Figure 3. High Temperature Reverse Bias Circuit

4.3.7 The following measurements will be made before and after the high temperature reverse bias test. The unit measurements shall be recorded or the devices will be celled in order to compare and guarantee the delta (Δ) requirements depending on the test level to which the lot is being prepared.

Device Type	Test 1.1.C	Maximum Readings Initial and Final	Delta Change	Symbol
SM600-602	8	1.5V	±0.3V	V4-1 (on)
SM625-627	8	1.5V	±0.3V	V4-1 (on)
SM610-612	8	-1.5V	±0.3V	V4-1 (on)
SM635-637	8	--1.5V	±0.3V	V4-1 (on)
SM600-602	10	1.0V	±0.25V	V2-1 (on)
SM625-627	10	1.25V	±0.30V	V2-1 (on)
SM610-612	10	-1.0V	±0.25V	V2-1 (on)
SM635-637	10	-1.25V	±0.30V	V2-1 (on)
SM600-602	12	10μA	±1.0[1]μA	I4-1
SM625-627	12	10μA	±1.0[1]μA	I4-1
SM610-612	12	-10μA	±1.0[1]μA	I4-1
SM635-637	12	-10μA	±1.0[1]μA	I4-1
SM600-602	14	10μA	±2.0[1]μA	I1-2
SM625-627	14	10μA	±2.0[1]μA	I1-2
SM610-612	14	-10μA	±2.0[1]μA	I1-2
SM635-637	14	-10μA	±2.0[1]μA	I1-2

[1] or ±100% whichever is greater

4.38 Power Stress – Each Hybrid device shall be burned-in using the circuit shown in Figure 4. The conditions are as follows:

$T_C = 140^O$ C

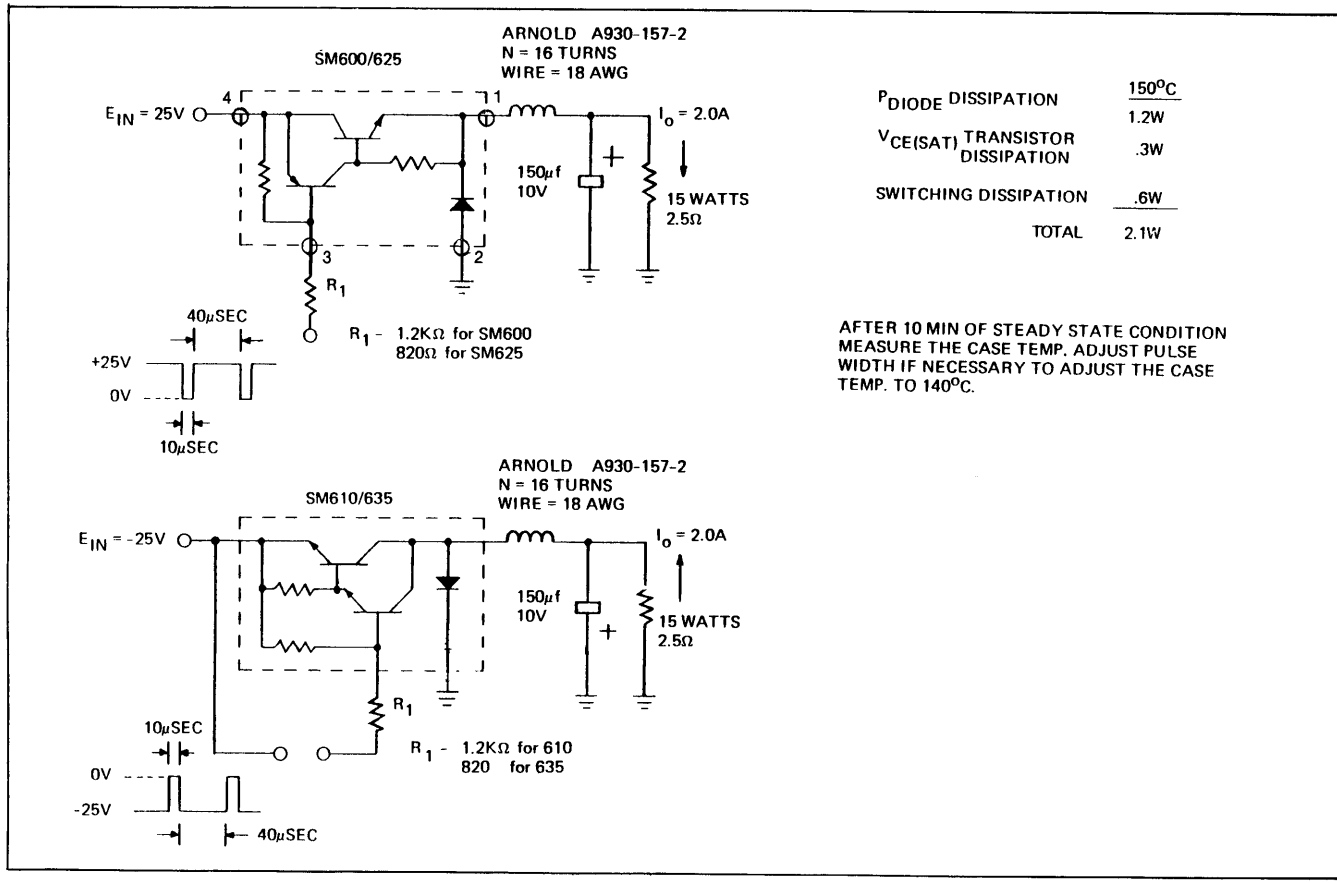
Time = 40 hours minimum

Circuit and conditions as shown in Figure 4.

4.3.9 The readings before and after burn-in shall be as specified in paragraph 4.3.7 above.

TABLE I. GROUP A INSPECTION

Examination or Test	Symbol	Electrical Spec Test Number	Sample Size (LTPD)	Max. Acc. No. of Failures
Subgroup 1				
Visual and Mechanical	..	..	22 (10)	0
Subgroup 2 25°C Tests				
On-State Voltage	V4-1 on	8		
On-State Voltage	V4-1 on	9		
Diode Forward Voltage	V2-1 on	10	45	0
Diode Forward Voltage	V2-1 on	11	(5)	
Off State Current	I4-1	12		
Diode Reverse Current	I1-2	14		
Subgroup 3 100°C Tests				
Off State Current	I4-1	13	45	0
Off State Current	I1-2	15	(5)	
Subgroup 4 25°C Tests				
Current Delay Time	tdi	1		
Current Rise Time	tri	2		
Voltage Rise Time	trv	3	45	0
Voltage Fall Time	tfv	5	(5)	
Current Fall Time	rfi	6		



	150°C
P_{DIODE} DISSIPATION	1.2W
$V_{CE(SAT)}$ TRANSISTOR DISSIPATION	.3W
SWITCHING DISSIPATION	.6W
TOTAL	2.1W

AFTER 10 MIN OF STEADY STATE CONDITION MEASURE THE CASE TEMP. ADJUST PULSE WIDTH IF NECESSARY TO ADJUST THE CASE TEMP. TO 140°C.

Figure 4. POWER BURN-IN CIRCUIT

SILICON GENERAL INC.
11651 Monarch Street, Garden Grove, California 92641 • 714/892-5531 • TWX: 910-596-1804

SPECIFICATION HRT 600-2

HYBRID SWITCHING REGULATORS
HIGH RELIABILITY TYPES
(3 LEAD TO-3)

SM645
SM646
SM647
SM655
SM656
SM657

7

CONTENTS

Standard Type	High Rel Construction with T_1 Testing	High Rel Construction with T_2 Testing
SM645	SM645B	SM645A
SM646	SM646B	SM646A
SM647	SM647B	SM647A
SM655	SM655B	SM655A
SM656	SM656B	SM656A
SM657	SM657B	SM657A

1.0 SCOPE

This specification defines the detail requirements for High Reliability Hybrid Switching Regulators. (Reference MIL-STD-750). Very extensive 100% testing for parameter stability has been included in the Quality Assurance Provisions.

1.1a ABSOLUTE MAXIMUM RATINGS

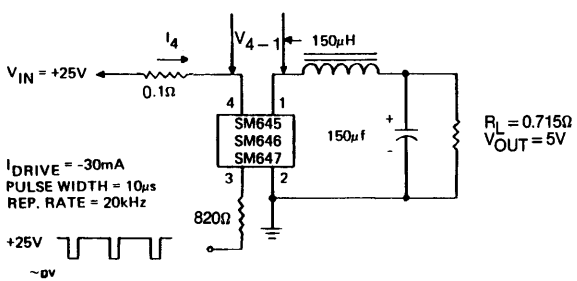
	SM645	SM646	SM647	SM655	SM656	SM657
Input Voltage, V_{4-2}	60V	80V	100V	-60V	-80V	-100V
Output Voltage, V_{1-2}	60V	80V	100V	-60V	-80V	-100V
Drive-Input Reverse Voltage, V_{3-4}	5V	5V	5V	-5V	-5V	-5V
Output Current, I_1	15A	15A	15A	-15A	-15A	-15A
Peak Output Current	20A	20A	20A	-20A	-20A	-20A
Drive Current, I_3	-0.4A	-0.4A	-0.4A	0.4A	0.4A	0.4A
Thermal Resistance						
Junction to Case, θ_{J-C}						
Power Switch	2^{o} C/W					
Commutating Diode	2^{o} C/W					
Case to Ambient, θ_{C-A}	30.0^{o} C/W					
Operating Temperature Range, T_C	-55^{o} C to $+125^{o}$ C					
Maximum Junction Temperature, T_j	$+150^{o}$ C					
Storage Temperature Range	-65^{o} C to $+150^{o}$ C					

	Test	Symbol	SM645, 646 AND 647			SM655, 656 AND 657			Units	Conditions
			Min.	Typ.	Max.	Min.	Typ.	Max.		
1	Current Delay Time ($I_3 - I_4$)	t_{di}	–	35	60	–	35	60	ns	V_{in} = 25V (-25V)
2	Current Rise Time (I_4)	t_{ri}	–	65	150	–	65	175	ns	V_{out} = 5V (-5V)
3	Voltage Rise Time (V_{4-1})	t_{rv}	–	40	60	–	40	60	ns	I_{out} = 7A (-7A)
4	Voltage Storage Time ($V_{4-1} - I_3$)	t_{sv}	–	900	–	–	900	–	ns	I_3 = -30 mA (30 mA)
5	Voltage Fall Time (V_{4-1})	t_{fv}	–	70	175	–	100	300	ns	
6	Current Fall Time (I_4)	t_{fi}	–	175	300	–	175	300	ns	
7	Efficiency (Note 1)	η	–	85	–	–	85	–	%	
8	On-State Voltage (Note 2)	V_{4-1} (on)	–	1.0	1.5	–	-1.0	-1.5	V	I_4 = 7A (-7A), I_3 = -0.03A (0.03A)
9	On-State Voltage (Note 2)	V_{4-1} (on)	–	2.5	3.5	–	-2.5	-3.5	V	I_4 = 15A (-15A), I_3 = -0.03A (0.03A)
10	Diode Forward Voltage (Note 2)	V_{2-1} (on)	–	0.85	1.25	–	-0.85	-1.25	V	I_2 = 7A (-7A)
11	Diode Forward Voltage (Note 2)	V_{2-1} (on)	–	0.95	1.75	–	-0.95	-1.75	V	I_2 = 15A (-15A)
12	Off-State Current	I_{4-1}	–	0.1	10.0	–	-0.1	-10.0	μA	V_4 = Rated input voltage
13	Off-State Current	I_{4-1}	–	10.0	1000.0	–	-10.1	-1000.0	μA	V_4 = Rated input voltage, T_A = 100°C
14	Diode Reverse Current	I_{1-2}	–	1.0	10.0	–	-1.0	-10.0	μA	V_1 = Rated output voltage
15	Diode Reverse Current	I_{1-2}	–	500.0	1000.0	–	-500.0	-1000.0	μA	V_1 = Rated output voltage, T_A = 100°C

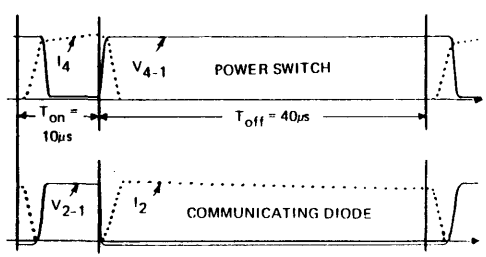
Notes:
1. The efficiency is a measure of internal power losses and is equal to Output Power divided by Input Power. The switching speed circuit of Figure 1, in which the efficiency is measured, is representative of typical operating conditions for the SM600 series switching regulators.
2. Pulse test: Duration = 300μs, Duty Cycle ≤2%, 25°C.

POWER DISSIPATION CONSIDERATIONS

The total power losses in the switching regulator is the sum of the switching losses, and the power switch and diode D.C. losses. Once total power dissipation has been determined, the Power Dissipation curve, or thermal resistance data may be used to determine the allowable case or ambient temperature for any operating condition.



SM645,646,647 Switching Speed Circuit



SM645,646,647 Switching Waveforms

Note: SM655, SM656, SM657 Circuit and waveforms are identical but of opposite polarity (V_{in} = -25V, V_{out} = -5V, I_{DRIVE} = +30mA).

Figure 1.

2.0 APPLICABLE DOCUMENTS

The following documents of the issue in effect on the date of invitations for bids, form a part of this specification to the extent specified herein.

MIL-S-19500 – General Specification for Semiconductor Devices

MIL-S-19491 – Preparation for Delivery of Semiconductor Devices

3.0 Requirements

3.1 Design and Construction

The Hybrid devices supplied under this specification shall have a design and construction such that they will meet all of the requirements specified herein. The dimensions and physical characteristics shall be as specified in Figure 2.

3.2 Performance Characteristics

The performance characteristics of the Hybrid device supplied under this specification shall be as specified in Group A inspection defined in Table I.

3.3 Quality Assurance

The Quality Assurance Provisions shall be as defined in paragraph 4.0.

3.4 Test Methods

Test methods shall be as specified herein.

3.5 Marking

The markings on the devices supplied shall be permanent and legible and shall include the Manufacturer's name or trademark, a Manufacturing Date Code in accordance with MIL-S-19500 and the specific device type number.

3.6 Preparation for Delivery

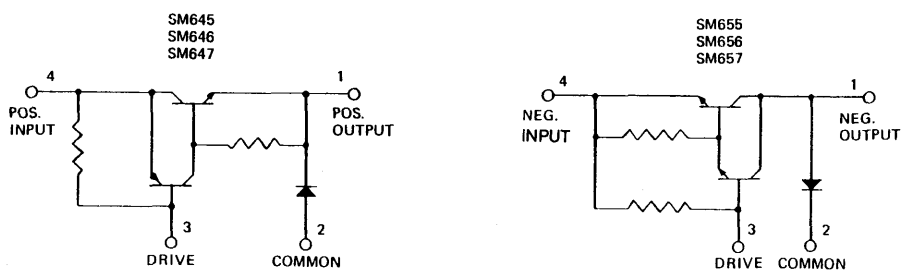
The Hybrid devices supplied under this specification shall be prepared for delivery in accordance with level C of MIL-S-19491 unless otherwise directed in the specific contract or purchase order.

3.7 Ordering Data

Procurement document should specify the following:

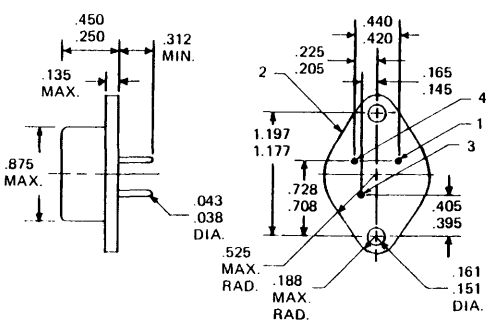
a. Specific item type number
b. Number and date of this specification
c. Quality Assurance Test level required
d. Any special packaging if required

SCHEMATIC



SCHEMATIC

MECHANICAL SPECIFICATION



NOTE:
Loads may be soldered to within 1/16" of base provided temperature-time exposure is less than 260°C for 10 seconds.

3 Pin TO-3

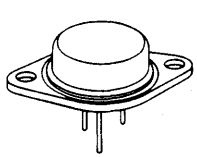


Figure 2. Physical Dimensions and Biasing Diagrams

4.0 QUALITY ASSURANCE PROVISIONS

4.1 General Provisions

4.1.1 Inspection Responsibility – The supplier is responsible for the performance of all inspection requirements and acceptability of results as specified herein for the Test Level identified in the contract or purchase order.

4.1.2 Controlled Manufacturer – The devices supplied under this specification shall be manufactured under controlled conditions using formally defined quality assurance methods and systems.

4.1.3 Manufacturing Traceability – Each device supplied under this specification shall be traceable to a specific process group, to permit tracing of its full manufacturing history. Process group records shall indicate the exact date that each manufacturing operation was performed and identify materials and process procedures which were used. The manufacturer shall keep these records on file for at least five years.

4.1.4 Definitions

4.1.4.1 Inspection Lot – An "inspection lot" is a collection of devices from which a sample is withdrawn and inspected to determine compliance with the acceptability criterion. It shall consist of one or more "inspection sublots" of the device types defined in this specification. The maximum inspection lot size shall be 5000 units.

4.1.4.2 Inspection Sublot – An "inspection sublot" shall consist of a collection of devices of a single type which have been manufactured under the same conditions and with the same materials.

4.1.4.3 Shipment Lot – A "shipment lot" shall consist of devices taken from an accepted inspection lot for the purpose of shipment on a specific contract or order.

4.1.4.4 Group A Inspection – Group A inspection shall consist of the examinations and tests specified in Table I, and shall be performed on a sublot basis.

4.1.4.5 Controlled Inventory – The controlled inventory shall consist of lots which have successfully passed the acceptance inspection and are being held in storage prior to actual shipment. A controlled inventory shall have adequate safeguards to insure that no defective or untested devices can be included in it. It shall be accessible only to those individuals who are formally identified as authorized personnel.

4.2 Acceptance Inspection

The acceptance inspection requirements shall be as defined by the applicable test level. The procedures of MIL-S-19500 shall apply to Group A inspection. Inspection lots which have been inspected and accepted shall be kept in a controlled inventory. Shipment lots shall be formed using devices taken from accepted inspection lots.

4.2.1 Test Level T2 Requirements – Test level T2 shall consist of the following requirements.

4.2.1.1 The supplier shall perform the Parameter Stability Testing defined in paragraph 4.3 on each device to be supplied. Prior to starting the Blocking Stability test defined in paragraph 4.3.6, each device shall be serialized for individual identity. Variables test data for the controlled electrical parameters shall be recorded before and after stressing. The same procedure shall apply for the Power Stress stability test defined in paragraph 4.3.8.

4.2.1.2 The supplier shall perform the Group A inspections in accordance with the defined LTPD requirements on each inspection sublot. Electrical parameter testing as specified shall be performed by variables with test data recorded.

4.2.1.3 With each shipment lot, the supplier shall provide a Certificate of Compliance to test level T2 of this specification.

4.2.2 Test Level T1 Requirements – Test level T1 shall consist of the following requirements.

4.2.2.1 The supplier shall perform the Parameter Stability Testing defined in paragraph 4.3 on each device to be supplied. Electrical parameter testing as specified shall be performed by attributes.

4.2.2.2 The supplier shall perform the Group A inspections in accordance with the defined LTPD requirements on each inspection sublot. Electrical parameter testing as specified shall be performed by attributes with test data recorded.

4.2.2.3 The supplier shall provide a Certificate of Compliance to test level T1 of this specification with each shipment lot.

4.3 Parameter Stability Tests

Each Hybrid device is to be supplied under this specification and shall receive the following tests in addition to other standard testing performed by the manufacturer.

4.3.1 Hermetic Seal Test – Fine Leak – Each Hybrid device shall be tested for a case leakage rate of 1×10^{-8} cc/sec or smaller using a helium mass spectrometer or equivalent method. Devices with a case leakage rate greater than specified shall be removed from the lot.

4.3.2 Hermetic Seal Test – Gross Leak – Each Hybrid device shall be tested for gross leaks using fluorocarbon gross leak test or equivalent method. Devices with any indication of case leakage shall be removed from the lot.

4.3.3 Temperature Storage – Each Hybrid device shall be subjected, in a non-operating state, to a temperature of $150^{\circ}C$ for a minimum period of 48 hours.

4.3.4 Temperature Cycling – Each Hybrid device shall be temperature cycled from -55°C to 150°C for a minimum of 10 cycles. Each cycle shall consist of at least 15 minutes at each temperature extreme with a maximum transition time of 5 minutes between each temperature extreme.

4.3.5 Reverse Bias Clamp Inductive Test –

V_{CEO} = Rated Input Voltage

I_C = 5A., f = 25 kHz, E_{out} = 5V

T_C = 25°C, see Figure 4

4.3.6 High Temperature Reverse Bias – Each Hybrid device will be high temperature reversed biased in the circuit shown in Figure 3. The conditions of this test are as follows:

TA = +125°C

Time = 16 hours $^{+8}_{-0}$ hours

Circuit and voltages as shown in Figure 3 for appropriate device.

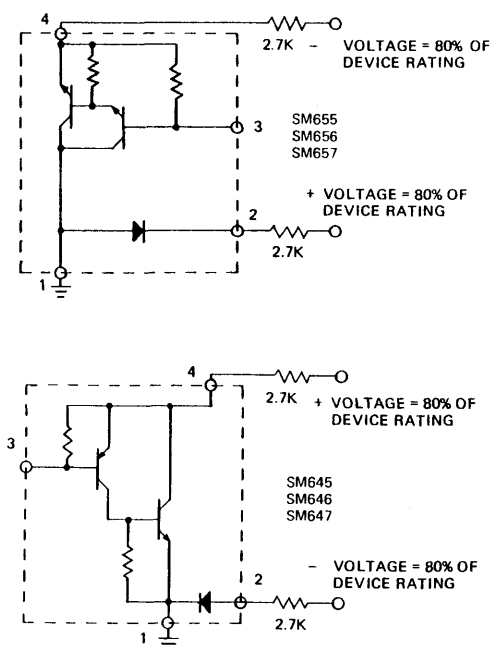


Figure 3. High Temperature Reverse Bias Circuit

4.3.7 The following measurements will be made before and after the high temperature reverse bias test. The unit measurements shall be recorded or the devices will be celled in order to compare and guarantee the delta (Δ) requirements depending on the test level the lot is being prepared to.

Type Number	Test 1.1.6	Maximum Readings Initial & Final	Delta Change	Symbol
SM645/646/647	8	-1.5V	±0.3V	V4-1 (on)
SM655/656/657	8	-1.5V	±0.3V	V4-1 (on)
SM645/646/647	10	1.25V	±0.3V	V2-1 (on)
SM655/656/657	10	-1.25V	±0.3V	V2-1 (on)
SM645/646/647	12	10μA[1]	±1.0μA[1]	I4-1
SM655/656/657	12	-10μA	±1.0μA[1]	I4-1
SM645/646/647	14	10μA	±2.0μA[1]	I1-2
SM655/656/657	14	-10μA	±2.0μA[1]	I1-2

[1] or ± 100% whichever is greater.

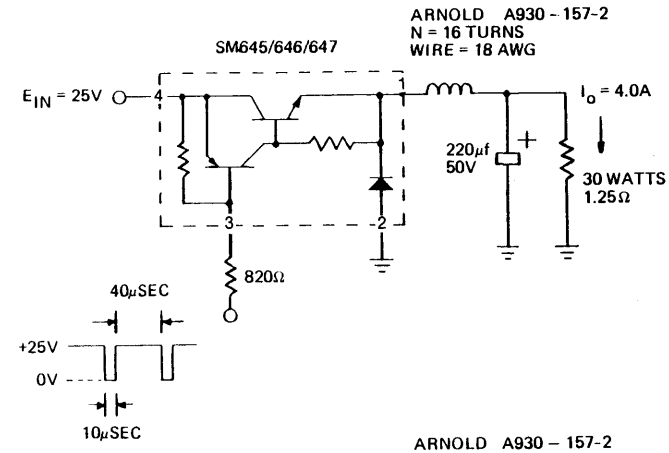
4.3.8 Power Stress – Each Hybrid device shall be burned-in using the circuit shown in Figure 4. The conditions are as follows:

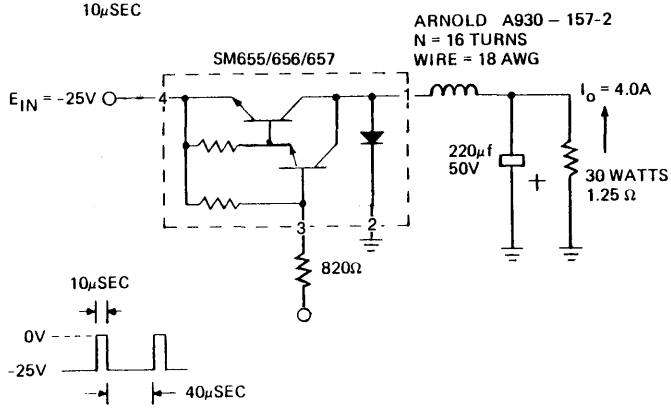
T_C = 140°C

Time = 40 hours minimum

Circuit and conditions as shown in Figure 4.

4.3.9 The readings before and after burn-in shall be as specified in paragraph 4.3.7 above.





	150°C
P_{DIODE} DISSIPATION	2.4W
$V_{CE(SAT)}$ TRANSISTOR DISSIPATION	0.6W
SWITCHING DISSIPATION	1.2W
TOTAL	4.2W

AFTER 10 MIN. OF STEADY STATE CONDITION, MEASURE THE CASE TEMP. ADJUST PULSE WIDTH IF NECESSARY TO ADJUST THE CASE TEMPERATURE TO 140°C.

Figure 4. POWER BURN-IN CIRCUIT

TABLE I. GROUP A INSPECTION

Examination or Test	Symbol	Electrical Spec Test Number	Sample Size (LTPD)	Max. Acc. No. of Failures
Subgroup 1				
Visual and Mechanical	–	–	22 (10)	0
Subgroup 2 25°C Tests				
On-State Voltage	V4-1 on	8	45 (5)	0
On-State Voltage	V4-1 on	9		
Diode Forward Voltage	V2-1 on	10		
Diode Forward Voltage	V2-1 on	11		
Off-State Current	I4-1	12		
Diode Reverse Current	I1-2	14		
Subgroup 3 T_A = +100°C Tests				
Off-State Current	I4-1	13	45 (5)	0
Off-State Current	I1-2	15		
Subgroup 4 25°C Tests				
Current Delay Time	t_{di}	1	45 (5)	0
Current Rise Time	t_{ri}	2		
Voltage Rise Time	t_{rv}	3		
Voltage Fall Time	t_{fv}	5		
Current Fall Time	t_{fi}	6		

TRANSISTOR ARRAYS

Silicon General
LINEAR INTEGRATED CIRCUITS

SG3183/3183A

High Current NPN Transistor Arrays

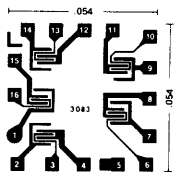
This series of arrays consists of five closely-matched, high current NPN transistors. Although sharing a common monolithic substrate, the transistors are connected such that all terminals are independent, including the substrate bias connector. With current capability to 100 mA per transistor, these arrays are ideally suited for all types of driving applications including relays, lamps, and thyristors. The SG3183 and SG3183A are higher voltage versions of the SG3083.

FEATURES

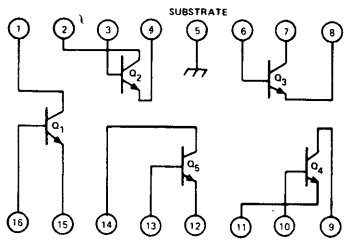
- High voltage capability
- Collector current to 100 mA
- Low saturation voltage
- Closely matched parameters

ABSOLUTE MAXIMUM RATINGS

Power Dissipations:	
Any one transistor	500 mW
Total package	750 mW
Above 25°C derate linearly	6.67 mW/°C
Ambient Temperature Range:	
Operating (N-Package)	−40 to +85°C
Operating (J-Package)	−55 to +125°C
Storage (both packages)	−65 to +150°C
Maximum Collector Current	100 mA
Maximum Base Current	20 mA



SG3083 Chip (See schematic for pad functions)



NOTE: The collector of each transistor is isolated from the substrate by an integral diode which must be reverse biased by connecting the substrate to a voltage more negative than any collector. To prevent undesired coupling between transistors, the substrate connection should be connected to an AC or DC ground.

ELECTRICAL CHARACTERISTICS AT TA = 25°C

PARAMETER SYMBOL CONDITIONS	MIN.	TYP.	MAX.	UNITS
Collector-Substrate Breakdown Voltage, BV_{CSO}, I_C = 100 µA				
SG3183	40	70	–	V
SG3183A	50	70	–	V
Collector-Base Breakdown Voltage, BV_{CBO}, I_C = 100 µA				
SG3183	40	70	–	V
SG3183A	50	70	–	V
Collector-Emitter Breakdown Voltage, BV_{CEO}, I_C = 1 mA				
SG3183	30	40	–	V
SG3183A	40	50	–	V
Emitter-Base Breakdown Voltage, BV_{EBO}, I_E = 100 µA				
All types	5	6.9	–	V
Collector Cutoff Current, I_{CEO}, V_{CE} = 10V	–	–	10	µA
Collector Cutoff Current, I_{CBO}, V_{CB} = 10V	–	–	1	µA
DC Forward Current Transfer Ratio, h_{FE}				
All types V_{CE} = 3V, I_C = 10 mA	50	100	–	
V_{CE} = 5V, I_C = 50 mA	40	75	–	
Collector-Emitter Saturation Voltage, V_{CE} (SAT)				
SG3183 /SG3183A I_C = 50 mA, I_B = 5 mA	–	1.7	3.0	V
Base to Emitter Voltage, V_{BE}, V_{CE} = 3V, I_C = 10 mA	0.65	0.75	0.85	V
For Q_1 and Q_2 Matched Pair				
Input Offset Voltage $\lvert V_{IO}\rvert$ V_{CE} = 3V, I_C = 1 mA	–	1.2	5	mV
Input Offset Current $\lvert I_{IO}\rvert$ V_{CE} = 3V, I_C = 1 mA	–	0.7	2.5	µA

8

Transistor Arrays

These transistor arrays offer V_{BE} typically matched to ±0.5 mV, less than 10% variation in hfe, operation from dc to 300 MHz, high current gain from 10 μA to 10 mA and high voltage capability.

SG3821 (CA3046, 3045) Matched Transistor Array — five general purpose monolithic NPN transistors internally connected to form two independent differential amplifiers, each with its associated current source transistor.

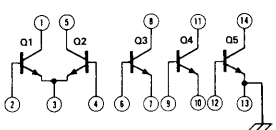
ABSOLUTE MAXIMUM RATINGS

Collector-substrate Voltage	40V (CA Series 20V)	Emitter-base Voltage	5V
Collector-base Voltage	40V (CA Series 20V)	Collector-Current	50mA
Collector-emitter Voltage	25V (CA Series 15V)	Operating Temperature Range	0—125°C (CA Series 0 - 70°C)

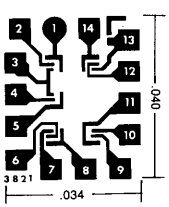
PARAMETERS*	CONDITIONS	3821,	3046/3086	UNITS
Collector-Substrate Breakdown	I_C = 10μA, I_B = 0	40	20	V
Collector-Base Breakdown	I_C = 10μA, I_E = 0	40	20	V
Collector-Emitter Breakdown	I_C = 100μA, I_B = 0	25	15	V
Emitter-Base Breakdown	I_E = 10μA, I_C = 0	5	5	V
Collector-Substrate Leakage	V_{CS} = 20V, I_B = 0	80	80	nA
Collector-Base Leakage	V_{CB} = 20V, I_E = 0	40	40	nA
Collector-Emitter Leakage	V_{CE} = 20V, I_B = 0	500	500	nA
Forward Current-Transfer Ratio	V_{CE} = 5V, I_C = 10μA	80 (typ)	80 (typ)	–
Forward Current-Transfer Ratio	V_{CE} = 5V, I_C = 1mA	50/400	50/400	–
Forward Current-Transfer Ratio	V_{CE} = 5V, I_C = 10mA	80 (typ)	80 (typ)	–
Collector-Emitter Saturation	I_C = 10mA, I_B = 1mA	0.5 (typ)	0.5 (typ)	V
Gain-Bandwidth Product	V_{CE} = 5V, I_C = 3mA	500 (typ)	500 (typ)	MHz
Collector-Substrate Capacitance	V_{CS} = 5V, I_C = 0	2.0 (typ)	2.0 (typ)	pF
Collector-Base Capacitance	V_{CB} = 5V, I_C = 0	0.4 (typ)	0.4 (typ)	pF
Noise Figure	f = 1kc, V_{CE} = 5V, I_C = 100μA, R_S = 1kΩ	4 (typ)	4 (typ)	dB
Input Offset Voltage for any two transistors	V_{CE} = 5V, I_C = 1mA	5	5	mV
Input Offset Current for any two transistors	V_{CE} = 5V, I_C = 1mA	4	2	μA

*Parameters apply for T_A = 25°C and are min/max limits unless otherwise specified.

Note: Substrate pin (⊿) must be connected to the most negative DC potential -- which should also be a good AC ground -- for proper isolation between transistors.



3821/3046/3045/



OTHER CIRCUITS

Wideband Amplifiers/Multipliers

Multipliers

Modulators

Line Receivers

Voltage Comparators

Precision Voltage Reference

Voltage Comparators

The SG111/211/311 are medium speed, high input impedance devices which are especially well suited for use in level detection and low level voltage sensing applications. Operation may be obtained from supply voltages ranging from ±15V down to a single +5V source.

The output, an open collector NPN capable of switching 50V and 50mA, can drive RTL, DTL, TTL, MOS logic, relays or lamps. Both input and output can be isolated from ground and the output can drive loads referred to a positive supply, ground or a negative supply. These devices also offer offset balance, strobe capability and pin configuration of the SG710 Comparator.

- **Differential input voltage range of ±30V**
- **150nA maximum bias current**
- **Consumes 135mW at ±15V**

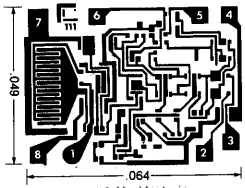
PARAMETERS*	111	211	311	UNITS
Operating Temperature Range	−55 to +125	−25 to +85	0 to +70	°C
Package Types	T, J	T, J		
Supply Voltage	±15			V
Input Offset Voltage $R_S \leq 50k$	3 (4.0)[2]		7.5 (10.0)[2]	mV
Input Offset Current	10 (20)[2]		50 (70)[2]	nA
Input Bias Current	100 (150)		250 (300)	nA
Voltage Gain	200 (typ)		200 (typ)	V/mV
Response Time[1]	200 (typ)		200 (typ)	nS
Saturation Voltage I_{sink} = 50 mA	1.5		1.5	V
V^+ = 4.5V, V^- = 0V, I_{sink} = 8 mA	0.4		0.4	V
Output Leakage Current	10 (500)		50	nA
Differential Input Voltage max	±30		±30	V
Total Supply Voltage, V_{84} max	36		36	V
Input Voltage Range	±14 (typ)		±14 (typ)	V
Positive Supply Current	6.0		7.5	mA
Negative Supply Current	5.0		5.0	mA
Output Voltage, V_{74}	50[3]		40[3]	V

*Parameters apply over supply voltage range and are min./max. limits either at T_A = 25°C (or over operating temperature range if enclosed in parentheses), unless otherwise indicated.

[1] The response time specified is for a 100mV input step with 5mV overdrive.

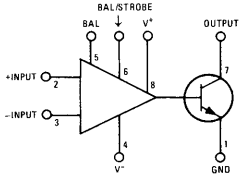
[2] The offset voltages and offset currents given are the maximum values required to drive the output down to 1V or up to 14V with 1mA load.

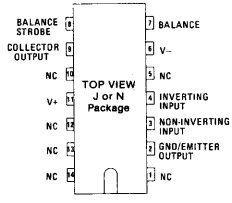
[3] Output voltage levels can be changed for compatibility with DTL and T2L logic levels.

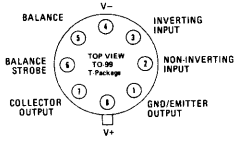


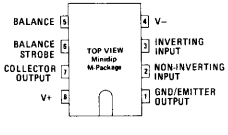
SG111/211/311 *Chip* (See T-package diagram for pad functions)

CONNECTION DIAGRAMS









Silicon General
LINEAR INTEGRATED CIRCUITS

SG1401/2401/3401

Video Amplifiers

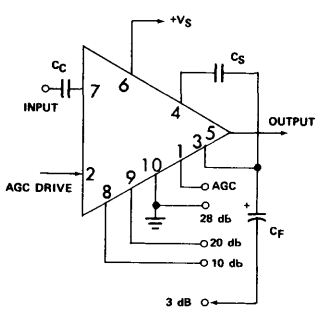
The SG1401/2401/3401 video amplifiers are useful over a frequency range from DC to 200MHz. Internal emitter followers are used to achieve high input and low output impedances, allowing simple capacitor coupling. Biasing and gain-setting resistors are internally diffused, eliminating external resistor networks. The gain may be externally varied through the use of AGC diodes which are included in the circuit.

- **20dB voltage gain at 100MHz**
- **5nsec rise and fall times**
- **Fixed or variable gain**
- **Single power supply voltage**
- **Minimum external components**
- **Symmetrical limiting**

PARAMETERS/CONDITIONS*	1401	2401	3401	UNITS
Operating Temperature Range	−55 to +125	0 to +70	0 to +70	°C
Package Types	T, J	T, J, N		–
Supply Voltage	6/20		6/20	V
Power Consumption, no AGC voltage	110		120	mW
DC Output Voltage	8.7 (typ)		8.7 (typ)	V
Peak-to-Peak Output, Pin 3 (4) to AC gnd	4 (typ)		3 (typ)	V
Voltage Gain, Pin 3 (4)[2] open	2.2/3.2		2.2/3.2	dB
Voltage Gain, Pin 3 (4)[2] coupled to Pin 8 (11)[2]	9/11		9/11	dB
Voltage Gain, Pin 3 (4)[2] coupled to Pin 9 (12)[2]	18/21		18/21	dB
Voltage Gain, Pin 3 (4)[2] to AC gnd	26/31		24/31	dB
Unity Gain Frequency, Pin 3 (4)[2] to AC gnd	200 (typ)		200 (typ)	MHz
Input Resistance, 20 dB gain	2.5 (typ)		2.5 (typ)	kΩ
Output Resistance, 20 dB gain	25 (typ)		50 (typ)	Ω
Input Capacitance, 20 dB gain	5 (typ)		5 (typ)	pF
Maximum Power Gain, 20 dB gain, R_L = 50Ω	30 (typ)		30 (typ)	dB
Temperature Stability, 20 dB gain	±1[1]		±2[1]	dB
AGC Range	20 (min)		22 (typ)	dB
Noise Figure, 20 dB gain, R_S = 1k	8 (min)		6 (typ)	dB

*Parameters apply only for T_A = 25°C, V_S = +12V, and f = 1 MHz, and are min/max limits unless otherwise specified.

[1] Over operating temperature range. [2] Numbers in parentheses refer to dual-in-line package.

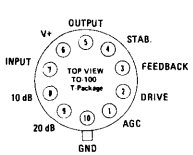


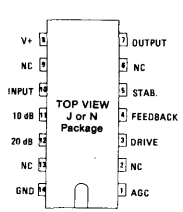
$$C_F = \frac{1}{2\pi f_c R}$$

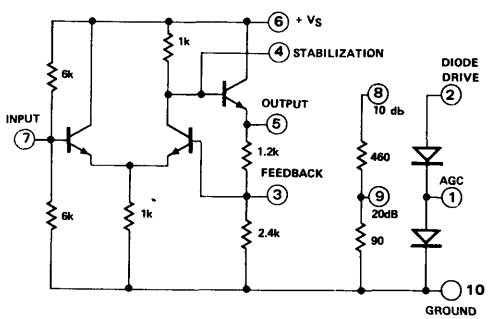
where f_c is low frequency corner and R is the gain setting resistance.

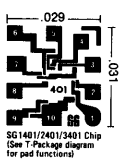
C_S = 0 to 10 pF to minimize high frequency peaking.

CONNECTION DIAGRAMS









See Applications Notes for additional information.

Wideband Amplifier/Multiplier

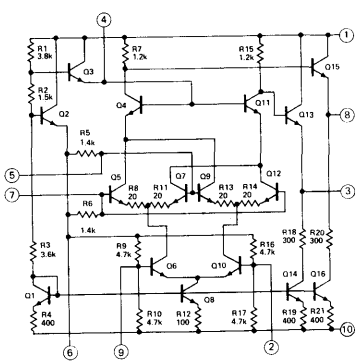
SG1402/2402/3402 are monolithic four quadrant multipliers offering excellent frequency response and provision for use as a variable gain amplifier with both non-inverting and inverting outputs available. In addition to linear amplification, the device is also ideal for balanced modulation, pulse or gated amplification, and coincidence detection.

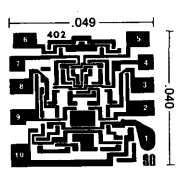
- **Single power supply voltage**
- **Self-contained biasing**
- **25dB voltage gain**
- **Differential or single ended inputs and outputs**
- **Large bandwidth**
- **Low power dissipation**

PARAMETERS, CONDITIONS*	1402	2402	3402	UNITS
Supply Voltage	+18		+18	V
Load Current	15		15	mA
Operating Temperature Range	−55 to +125	0 to +70	0 to +70	°C
Package Types	J, T	J, T, N		–
Maximum Voltage Gain, single ended	23		20	dB
Variable Gain Range, with ext. balance	55		40	dB
Frequency Response, f − 3 dB	40 (min)		50 (typ)	MHz
Input Impedance, Pin 5 or 7 (7 or 10)[1]	1.2 (typ)		1.2 (typ)	KΩ
Input Impedance, Pin 2 or 9 (3 or 12)[1]	1.8 (typ)		1.8	KΩ
Output Impedance, Pin 3 or 8 (4 or 11)[1]	100 (typ)		100 (typ)	Ω
Output Voltage Swing R_L = 100K R_L = 1K	 3 1.3		 3 1.3	Vpp
Quiescent DC Levels Pins 5, 6 and 7 (7, 8 & 10)[1]	3.6 (typ)		3.6 (typ)	V
Pins 2 and 9 (3 & 12)[1]	1.8 (typ)		1.8 (typ)	V
Pins 3 and 8 (4 & 11)[1]	6.5/7.5		7.0 (typ)	V
Output Offset Voltage Minimum Gain Maximum Gain	 100 200		 300 500	mV
DC Output Shift, with max gain change	100		200	mV
Differential Control Voltage, for max gain change	200 (typ)		200 (typ)	mV
Maximum Gain Variation, over temperature	2		3	dB
Equivalent Input Noise (BW = 10MHz, R_S = 50Ω)	25 (typ)		25	μVrms
Power Consumption	85		85	mW

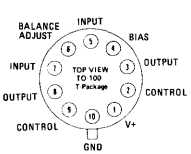
*Parameters are for T_A = 25°C, V^+ = 10V, f = 100KHz and are min./max. limits unless otherwise specified.

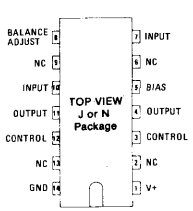
[1]Numbers in parentheses refer to dual-in-line package.



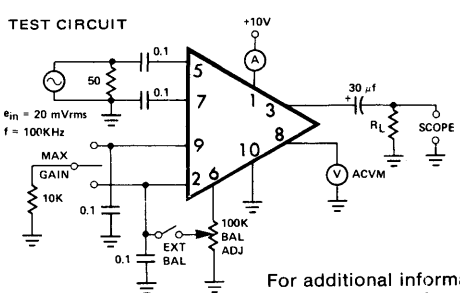


SG1402/2402/3402 Chip (See T-package diagram for pad functions)





CONNECTION DIAGRAMS



See Applications Notes for additional information.

For additional information on this device, refer to Applications Notes.

Line Receivers

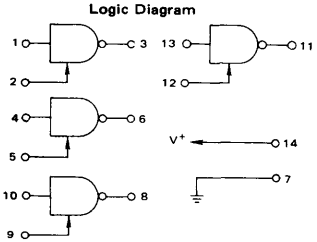
The SG1489A monolithic quad line receiver is designed to interface data terminal equipment with data communications equipment in conformance with the specifications of EIA Standard No. RS-232C.

- Input Resistance – 3.0k to 7.0kΩ
- Input Signal Range – ±30 Volts
- Input Threshold Hysteresis Built In
- Response Control
  - a) Logic Threshold Shifting
  - b) Input Noise Filtering

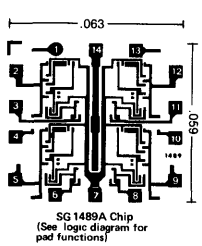
PARAMETERS*		SG1489A	UNITS
Power Supply Voltage (max, T_A = 25°C)		10	V
Input Signal Range (max, T_A = 25°C)		±30	V
Output Load Current (T_A = 25°C)		20	mA
Package Types		J	–
Power Dissipation (Package Limitation, Ceramic Dual In-Line Package)		1000	mW
Derate above T_A = +25°C		6.7	mW/°C
Operating Temperature Range		0 to +75	°C
Storage Temperature Range		–65 to +175	°C
Positive Input Current	(V_{in} = +25 Vdc)	3.6/8.3	mA
	(V_{in} = +3.0 Vdc)	0.43	
Negative Input Current	(V_{in} = –25 Vdc)	–3.6/–8.3	mA
	(V_{in} = –3.0 Vdc)	–0.43	
Input Turn-On Threshold Voltage (T_A = +25°C, $V_{OL} \leq$ 0.45V)		1.75/2.25	V
Input Turn-Off Threshold Voltage (T_A = +25°C, $V_{OH} \geq$ 2.5V, I_L = –0.5 mA)		0.75/1.25	V
Output Voltage High	(V_{in} = 0.75V, I_L = –0.5mA)	2.6/5.0	V
	(Input Open Circuit, I_L = –0.5 mA)	2.6/5.0	
Output Voltage Low	(V_{in} = 3.0V, I_L = 10mA)	0.45	V
Power Supply Current	(V_{in} = +5.0Vdc)	26	mA
Power Consumption	(V_{in} = +5.0Vdc)	130	mW
SWITCHING CHARACTERISTICS (T_A = +25°C)			
Propagation Delay Time	(R_L = 3.9kΩ)	85	nS
Rise Time	(R_L = 3.9kΩ)	175	nS
Propagation Delay Time	(R_L = 390 Ω)	50	nS
Fall Time	(R_L = 390 Ω)	20	nS

*Parameters are min./max. limits with response control pin open, V^+ = +5.0 Vdc ±1%, T_A = 0 to +75°C unless otherwise noted.

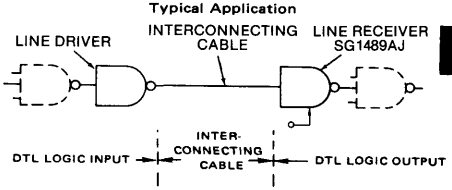
Logic Diagram



CONNECTION DIAGRAM FOR J-PACKAGE



Typical Application



PRECISION 2.5 VOLT REFERENCE

DESCRIPTION

This monolithic integrated circuit is a fully self-contained precision voltage reference generator, internally trimmed for ±1% accuracy. Requiring less than 2 mA in quiescent current, this device can deliver in excess of 10 mA with total load and line induced tolerances of less than 0.5%. In addition to voltage accuracy, internal trimming achieves a temperature coefficient of output voltage of typically 10 ppm/°C. As a result, these references are excellent choices for application to critical instrumentation and D to A converter systems. The SG1503 is specified for operation over the full military temperature range of -55°C to +125°C, while the SG2503 and SG3503 are designed for commercial applications of 0°C to +70°C.

FEATURES

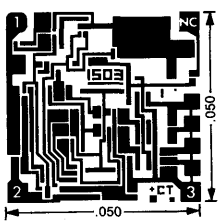
- **Output voltage trimmed to ±1%**
- **Input voltage range of 4.5 to 40V**
- **Temperature coefficient of 10 ppm/°C**
- **Quiescent current typically 1.5 mA**
- **Output current in excess of 10 mA**
- **Interchangeable with MC1503 and AD580**

ABSOLUTE MAXIMUM RATINGS

Input Voltage	4.5 – 40V	Operating Temperature Range	
Power Dissipation	600 mW	SG1503	-55°C to +125°C
Derate Over 25°C	4.8 mW/°C	SG2503/3503	0°C to +70°C
		Storage Temperature Range	-65°C to +150°C

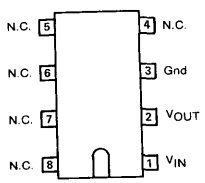
CONNECTION DIAGRAMS

CHIP LAYOUT

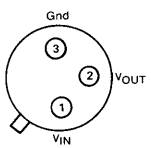


M or Y PACKAGE
MINIDIP

TOP VIEWS



T-PACKAGE
TO-39

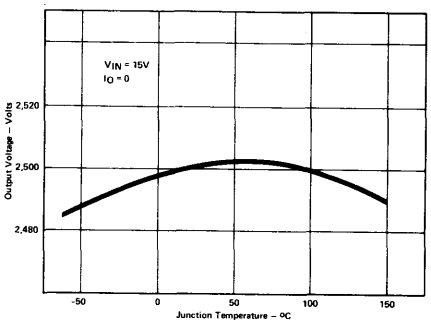


ELECTRICAL CHARACTERISTICS

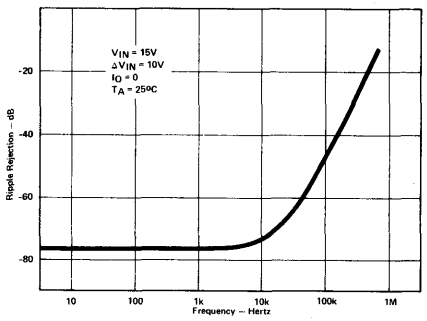
(Input Voltage = 15V, I_L = 0 mA, T_A = Operating Temperature Range unless otherwise stated.)

PARAMETER	TEST CONDITIONS	SG1503/2503			SG3503			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Output Voltage	T_A = 25°C	2.485	2.50	2.515	2.475	2.50	2.525	Volts
Input Voltage Range	T_A = 25°C	4.5	–	40	4.5	–	40	Volts
Input Voltage Range	Over Operating Temperature	4.7	–	40	4.7	–	40	Volts
Line Regulation	V_{IN} = 5 to 15V	–	1	3	–	1	3	mV
Line Regulation	V_{IN} = 15 to 40V	–	3	5	–	3	10	mV
Load Regulation	ΔI_L = 10 mA	–	3	5	–	3	10	mV
Load Regulation	ΔI_L = 10 mA, V_{IN} = 30V	–	4	8	–	4	15	mV
Temperature Regulation	-55° to +125°C	–	15	20	–	–	–	mV
Temperature Regulation	0°C to +70°C	–	2.5	5	–	5	10	mV
Quiescent Current	V_{IN} = 40V	–	1.5	2.0	–	1.5	2.0	mA
Short Circuit Current	T_A = 25° C	15	20	30	15	20	30	mA
Ripple Rejection	f = 120 Hz, T_A = 25°C	–	76	–	–	76	–	dB
Output Noise	B.W. = 10 kHz, T_A = 25°C	–	100	–	–	100	–	μV_{rms}
Stability		–	250	–	–	250	–	$\mu V/kHr$

OUTPUT VOLTAGE vs. TEMPERATURE



RIPPLE REJECTION



9

Multipliers

The SG1595/1495 four quadrant analog multipliers are designed for applications where the output voltage required is a linear product of two input voltages. Both types provide excellent linearity and operation over a wide supply range and input voltage range. Applications include use as multipliers, dividers, squarers, phase detectors, frequency doublers and as balanced modulators.

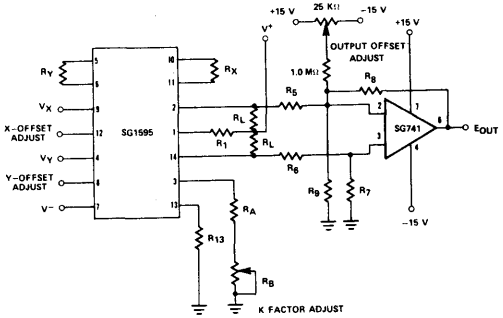
- **Excellent linearity**
- **Adjustable scale factor**
- **Excellent temperature stability**
- **Wide bandwidth**
- **High input voltage range**
- **Wide supply voltage operation**

PARAMETERS/CONDITIONS*	1595	1495	UNITS
Operating Temperature Range	−55 to +125	0 to +70	°C
Package Types	J	J, N	–
Applied Voltage[2]	30	30	V
Differential Input Signal	$V_9 - V_{12} = \pm(6 + I_{13} R_X)$ $V_4 - V_8 = \pm(6 + I_3 R_Y)$		–
Maximum Factor Adjust Current	10	10	mA
Linearity Error in Percent of Full Scale (T_A = 25°C) $-10 < V_X < +10$ ($V_Y = \pm 10V$) $-10 < V_Y < +10$ ($V_X = \pm 10V$)	 1.0 2.0	 2.0 4.0	(% max)
Squaring Mode Error T_A = 25°C T_A = 0°C to +70°C T_A = −55°C to +125°C	 0.5 – 0.75	 0.75 1.0 –	(% typ)
Scale Factor (adjustable) $K = \frac{2 R_L}{I_3 R_X R_Y}$	0.1 (typ)	0.1 (typ)	–
Input Resistance[1]	35 (typ)	20 (typ)	MΩ
Differential Output Resistance[1]	300 (typ)	300 (typ)	KΩ
Input Bias Current	8.0	12	μA
Input Offset Current	1.0	2.0	μA
Common Mode Gain	−50	−40	dB
Output Common Mode Voltage	21 (typ)	21 (typ)	V
Differential Output Voltage Swing	±14 (typ)	±14 (typ)	V
Pos Supply Voltage Rejection Ratio	5 (typ)	5 (typ)	mV/V
Neg Supply Voltage Rejection Ratio	10 (typ)	10 (typ)	mV/V
Neg Supply Current	7.0	7.0	mA
Power Consumption	170	170	mW
Average TC of Input Offset Current	2.0 (typ)	2.0 (typ)	nA/°C
Frequency Response (typ) −3 dB Bandwidth	3.0 (typ)	3.0 (typ)	MHz
3° Relative Phase Shift	750 (typ)	750 (typ)	kHz
1% Absolute Error Due to Input-Output Phase Shift	30 (typ)	30 (typ)	kHz

*Parameters apply over operating temperature range and are min/max limits unless otherwise specified.

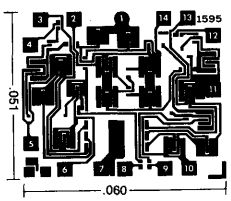
[1] f = 20 Hz [2] Voltage applied between pins 2-1, 14-1, 1-9, 1-12, 1-4, 1-8, 12-7, 9-7, 8-7, 4-7.

Multiply with Op Amp Level Shift

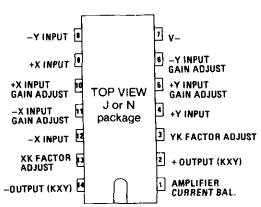


SET UP	RESISTOR* / TOLERANCE	R_1 5%	R_5 1%	R_6 1%	R_7 1%	R_8 1%	R_9 1%	R_{13} 1%	R_A 5%	R_B 20%	R_L 0.5%	R_X 5%	R_Y 5%
1	V^+ = +32 V, V^- = −15 V −10 V ≤ V_X ≤ +10 V −10 V ≤ V_Y ≤ +10 V	9.1	121	100	11	121	15	13.7	12	5.0	11	15	15
2	V^+ = +15 V, V^- = −15 V −5 V ≤ V_X ≤ +5 V −5 V ≤ V_Y ≤ +5 V	3.0	300	100	100	300		13.7	12	5.0	3.4	8.2	8.2
3	V^+ = +15 V, V^- = −15 V −10 V ≤ V_X ≤ +10 V −10 V ≤ V_Y ≤ +10 V	1.2	121	100	11	910	13.7	13.7	12	5.0	1.5	15	15

* All resistors are k ohms.



SG1595/1495 Chip (See D-package diagram for pad functions)



CONNECTION DIAGRAM

Silicon General

LINEAR INTEGRATED CIRCUITS

SG1596/1496

Modulators

The SG1596/1496 are monolithic double-balanced modulator/demodulator devices designed for use where the output voltage is a product of an input voltage (signal) and a switching function (carrier). Typical applications include modulation and demodulation of AM, SSB, DSB, FSK, FM and phase encoded signals. Additional uses include frequency doubling, linear mixing and chopping.

- **Excellent carrier suppression**
- **Fully balanced inputs and output**
- **Low offsets and drift**
- **High common mode rejection**
- **Adjustable gain and signal handling**
- **Useful to 100MHz**

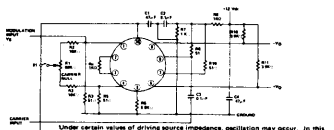
PARAMETERS/CONDITIONS*	1596	1496	UNITS
Operating Temperature Range	−55 to +125	0 to +70	°C
Applied Voltage[1]	30	30	V
Differential Input Signal, $(V_7 - V_8)$	±5.0	±5.0	V
Differential Input Signal, $(V_4 - V_1)$	$\pm(5 + I_5 R_e)$		V
Input Signal, $(V_2 - V_1, V_3 - V_4)$	5.0	5.0	V
Package Types	J, T	J, T, N	——
Carrier Feedthrough			
v_c = 60 mV(rms) sine wave, f_c = 1.0kHz, offset adjusted (typ)	40	40	μVrms
v_c = 60 mV(rms) sine wave, f_c = 10MHz, offset adjusted (typ)	140	140	
v_c = 300 mV_{pp} square wave, f_c = 1.0kHz, offset adjusted (max)	0.2	0.4	
v_c = 300 mV_{pp} square wave, f_c = 1.0kHz, offset not adjusted (max)	100	200	
Carrier Suppression			
f_s = 10kHz, 300 mV(rms), f_c = 500kHz, 60 mV(rms) sine wave offset adjusted (min)	50	40	dB
f_s = 10kHz, 300 mV(rms), f_c = 10MHz, 60 mV(rms) sine wave offset adjusted (typ)	50	50	
Transadmittance Bandwidth			
R_L = 50Ω, Carrier Input Port, v_c = 60 mV(rms) sine wave, f_s = 1.0kHz, 300 mV(rms) sine wave	300 (typ)	300 (typ)	MHz
Signal Input Port, v_s = 300 mV(rms) sine wave[2]	80 (typ)	80 (typ)	
Voltage Gain, Signal Channel v_s = 100 mV(rms), f = 1.0kHz[2]	2.5	2.5	V/V
Input Resistance, Signal Port f = 5.0MHz[2]	200 (typ)	200 (typ)	kΩ
Input Capacitance, Signal Port f = 5.0MHz[2]	2.0 (typ)	2.0 (typ)	pF
Single Ended Output Resistance f = 10MHz	40 (typ)	40 (typ)	kΩ
Single Ended Output Capacitance, f = 10MHz	5.0 (typ)	5.0 (typ)	pF
Input Bias Current $(I_1 + I_4)/2$ or $(I_7 + I_8)/2$	25	30	μA
Input Offset Current $(I_1 - I_4)$ or $(I_7 - I_8)$	5.0	7.0	μA
Average TC of Input Offset Current	2.0 (typ)	2.0 (typ)	nA/°C
Output Offset Current $(I_6 - I_9)$	50	80	μA
Average TC of Output Offset Current	90 (typ)	90 (typ)	nA/°C
Signal Port Common Mode Input Voltage Range f_s = 1.0kHz	5.0 (typ)	5.0 (typ)	V_{p-p}
Signal Port Common Mode Rejection Ratio[2]	−85 (typ)	−85 (typ)	dB
Common Mode Quiescent Output Voltage	8.0 (typ)	8.0 (typ)	V
Differential Output Swing Capability	8.0 (typ)	8.0 (typ)	V_{p-p}
Positive Supply Current $(I_6 + I_9)$	3.0	4.0	μA
Negative Supply Current (I_{10})	4.0	5.0	mA
Power Dissipation	33 (typ)	33 (typ)	mW

*Parameters are for T_A = 25°C and are min/max limits unless otherwise specified.

[1] Voltage applied between pins 6—7, 8—1, 9—7, 9—8, 7—4, 7—1, 8—4, 6—8, 2—5 and 3—5.

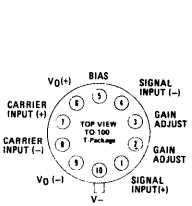
[2] $V_7 - V_8$ = 0.5 Vdc

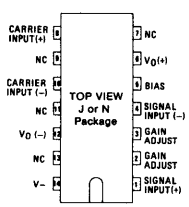
TYPICAL MODULATOR CIRCUIT

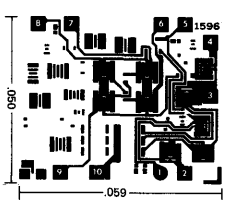


Under certain values of driving source impedance, oscillation may occur. In this event, an RC suppression network should be connected directly to each input using short leads. This will reduce the Q of the source-tuned circuits that cause the oscillation. Note: S1 is closed for "adjusted" measurements.

CONNECTION DIAGRAMS







SG1596/1496 Chip (See J-package diagram for pad functions)

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APPLICATION NOTES

SG1401 Video Amplifier

SG1402 Videoband Amplifier/Multiplier

SG1501A Dual Polarity Tracking Regulator

SG1524 Regulating Pulse Width Modulator
- — Simplifying Converter Design
- — Deadband Control
- — Improving Dynamic Response

SG1524B Regulating Pulse Width Modulator
- — Converting 1524 Designs
- — Versatile Control For Switching Power Supplies

SG1524/1525A/1526/1527A, 1627/1629 Power Supply Circuits

SG1542, 1543, 1544, 3523 Power Supply Supervisory Circuits

SG1549 Current Sense Latch

SG1627/1629 Dual High Current Output Driver

SG1635 Motor Drive IC

SG1731 High Efficiency Motor Drive Systems

SG1731 Feedback Controllers

The SG1401-SG3401 has been designed to provide maximum versatility as a general-purpose, single-ended amplifier. With its broad frequency capability, this circuit will be useful in a wide range of applications provided that the usual considerations for high-frequency circuit designs are observed. The following information is presented toward aiding in the optimization of the many possible configurations of this device.

FIXED GAIN

In the circuit configuration shown in Figure 1, the overall voltage gain is approximated by resistors R1 and the parallel combination of R2 and R3, as

$$Av \approx 1 + \frac{R_1}{R}, \text{ where } R = \frac{R_2 R_3}{R_2 + R_3}$$

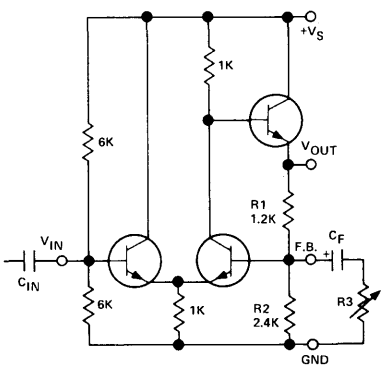

Figure 1.

With no external connections, the voltage gain is determined solely by R1 and R2 and is 1½ or 3 dB. Decreasing the effective value of R2 by capacitively coupling a lower resistor in parallel, raises the gain. Four fixed gain settings are provided internal to the circuit; however, any other setting within the maximum gain of the amplifier is possible with external resistors as shown in Figure 2.

The value of the coupling capacitor, C_F is determined by the low frequency response desired, as its capacitive reactance will add to the value of the resistance it couples. Therefore, the lower cutoff frequency will be

$$f_c \approx \frac{1}{2\pi R_3 C_F}$$

Utilizing the internal 90 or 460 ohm resistors for higher gain settings provides the added advantage of maximum temperature stability since the close tracking of adjacent diffused resistors keeps their ratio constant. Typical temperature variation of this circuit is shown below:

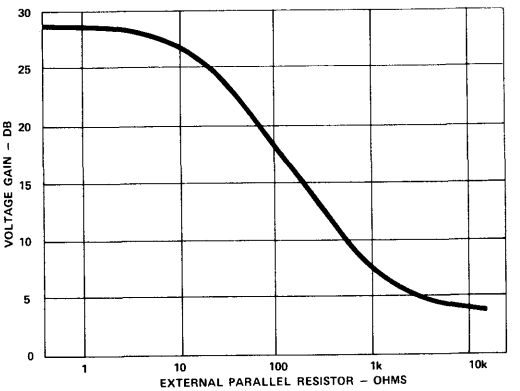

Figure 2. External Gain Control.

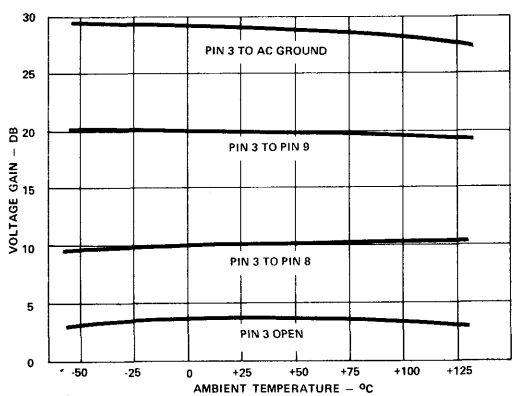

Figure 3. Temperature Stability.

VARIABLE GAIN

Since the dynamic impedance of a forward-biased diode is inversely proportional to the current through it, a convenient gain control can be achieved by using a pair of diodes as a variable impedance. In the circuit of Figure 4, R3 has been replaced by two diodes whose impedances act in parallel due to the decoupling of C_D. If the diodes are driven from a voltage source, a logarithmic relationship between gain and control signal is achieved (see Figure 5); while if a current source is used, the relationship is linear as shown in Figure 6.

There are two limitations on this form of gain control. First, the diodes' capacitance limits their effectiveness to frequencies below 20 MHz and, secondly, the signal voltage across the diodes should be held to less than 50 millivolts RMS to minimize self-modulation of amplifier gain. Additionally, the AGC current should be limited to 3 mA maximum to keep the diodes out of saturation.

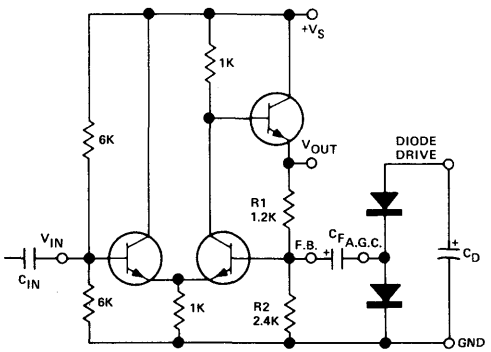

Figure 4.

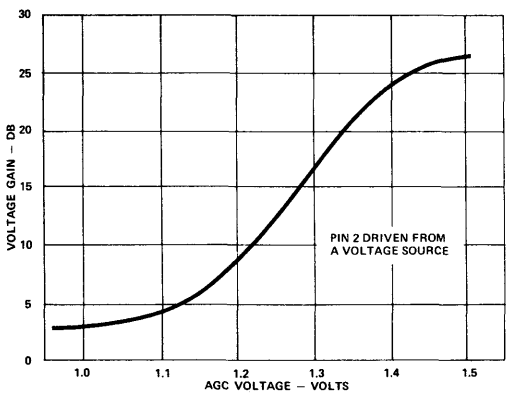

Figure 5. Gain vs. AGC Diode Voltage

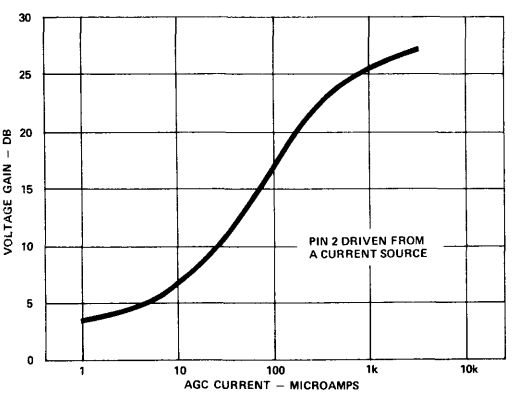

Figure 6. Gain vs. AGC Diode Current.

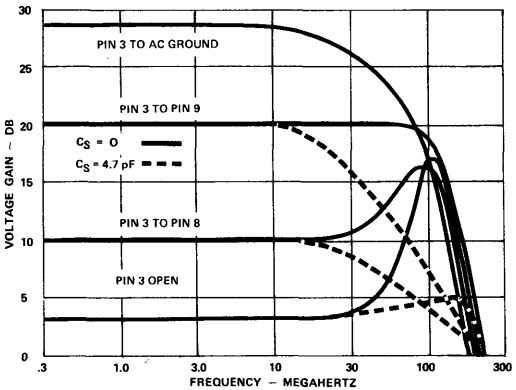

Figure 7. Frequency Response.

HIGH FREQUENCY STABILITY

With the capability of operation at 100 MHz, the SG1401-SG3401 also has some susceptibility to external stray reactances; however, with reasonable care, complete stability may be assured. Some general precautions which should be considered include the following:

(1) Power supply decoupling close to the circuit terminals (a 0.1 mfd capacitor is usually adequate).
(2) Maintain separation of input and output lines.
(3) Minimize load capacitance or insert a series resistor (up to 50 ohms) in the output.
(4) Purposely limit the high frequency response with a stabilizing capacitor C_S between pins 3 and 4.

Since the gain of this circuit is reduced by increasing the amount of feedback, the potential for instability is greatest when the gain is at its minimum value. This characteristic and the stabilizing effects of a 4.7 picofarad capacitor between pins 4 and 3 are illustrated in the frequency response curves presented in Figure 7. The relationship between the value of C_S and the upper cutoff frequency of a 20 dB gain setting is shown in Figure 8 below.

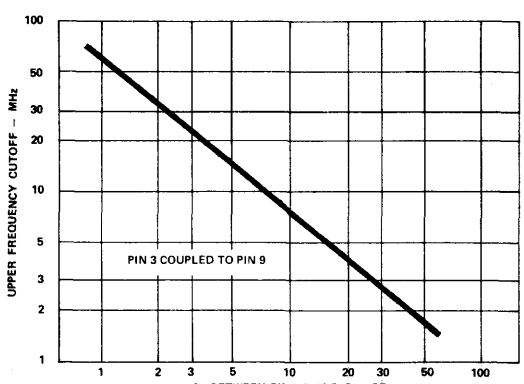

Figure 8. Upper Cutoff Frequency vs. C_S Value.

INTRODUCTION

Rapid advances in the state-of-the-art of processing monolithic linear integrated circuits have made the use of tightly matched components a practical reality. This in turn has opened the doors to a new class of circuit characterized by its utility, versatility, and ease of application. It is now possible to include on a monolithic chip, many of the components which, because of relatively poor tolerances, were formerly required to be external to the circuit. The SG1402, shown schematically in Figure 1, illustrates this capability both by its inclusion of all necessary biasing networks and by the nature of the circuit itself which requires extremely well matched component parameters for successful operation.

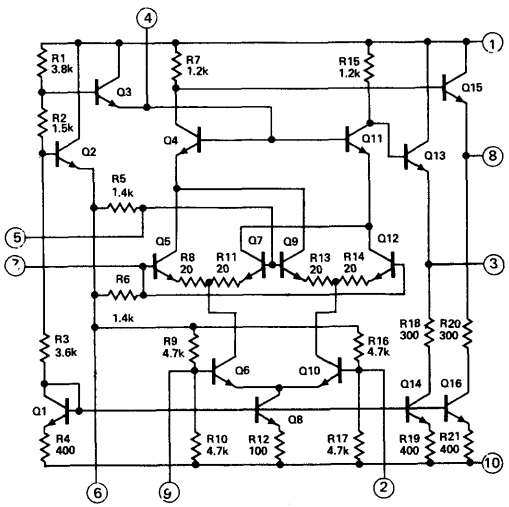

Figure 1. SG1402 Schematic Diagram.

HOW IT WORKS

The heart of the SG1402 is a four quadrant multiplier consisting of two cross-coupled differential amplifiers which are jointly controlled by a third differential amplifier. This part of the circuit is shown in simplified form as Figure 2. The constant current, I_0, is divided by Q6 and Q10 and divided again by each of the upper diff amps such that, for balanced operation, transistors Q5, Q7, Q9, and Q12 each have ¼ I_0 flowing through them. An examination of the way in which the above diff amps are cross-coupled will show that while the collector load resistors receive a portion of their current from each diff amp, the signals will arrive out of phase with respect to each other. This is because the input voltage, v_c, is amplified common emitter – with 180° phase shift – through Q9 and summed at resistor R7 with the signal which has gone common collector-common base – with 0° phase shift – through Q7 and Q5. Therefore, with the circuit perfectly balanced, the two signals completely cancel out and the output has zero signal. This can be shown mathematically as follows:

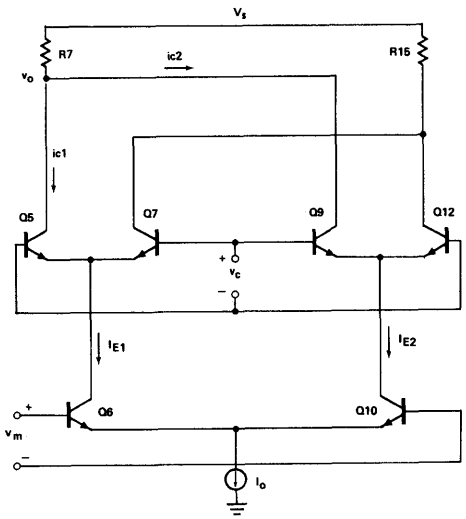

Figure 2. Simplified Schematic of the Multiplier Section of the SG1402.

The collector current in one side of a simple differential amplifier (Q5 and Q7, for example) is:

$$i_{c1} = \frac{I_{E1}}{1 + \exp\left(\frac{q}{kT} v_c\right)}$$

where: I_{E1} = sum of currents in each collector

$\frac{kT}{q}$ = 26 millivolts at 25°C

v_c = differential input voltage

This equation can be differentiated to obtain the transconductance which, for small values of v_c, is:

$$gm = \frac{di_{c1}}{d\,v_c} = \frac{q\,I_{E1}}{4kT}$$

In a similar manner, the transconductance through Q9 is:

$$gm = \frac{di_{c2}}{d\,v_c} = \frac{q\,I_{E2}}{4kT}$$

and the total voltage gain, Av is:

$$Av = R_L \frac{di_{c1}}{d\,v_c} + \frac{di_{c2}}{d\,v_c}$$

$$= \frac{R_L\,q}{4kT}\left(I_{E2} - I_{E1}\right)$$

Since $I_{E1} + I_{E2} = I_0$, it can be seen that when $v_m = 0$, $I_{E1} = I_{E2} = \frac{1}{2} I_0$ and Av = 0. With I_{E1} and I_{E2} being collector currents of another differential amplifier, the total small-signal gain equation may be written:

$$Av = \frac{v_0}{v_c} = \frac{R_L I_0 q}{4\ kT}\left[\frac{1}{1+\exp\left(\frac{q}{kT} v_m\right)} - \frac{1}{1+\exp\left(\frac{q}{-kT} v_m\right)}\right]$$

The circuit gain of the SG1402 is less than that predicted by the above equation due to the local feedback offered by the 20 ohm emitter resistors. The actual relationship between Av and v_m is shown in Figure 3 while Figure 4 graphs the full four-quadrant transfer function between the input voltage, v_c, the control voltage, v_m, and the output voltage. Note that the 20 ohm emitter resistors provide linearity for ±60 millivolts of input voltage while the modulating voltage is only linear for approximately half that value. It should be recognized from Figure 4 that output limiting occurs at a constant input voltage regardless of the modulating voltage. In other words, reducing the gain reduces the maximum peak-to-peak output swing.

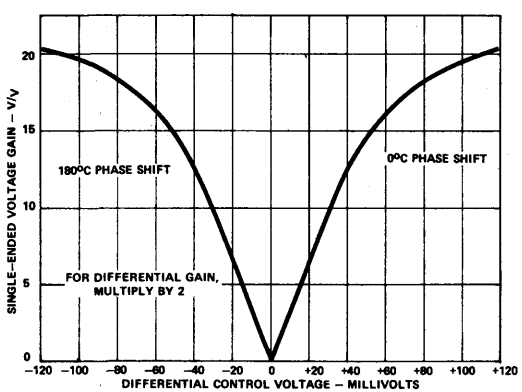

Figure 3. Differential Gain Control.

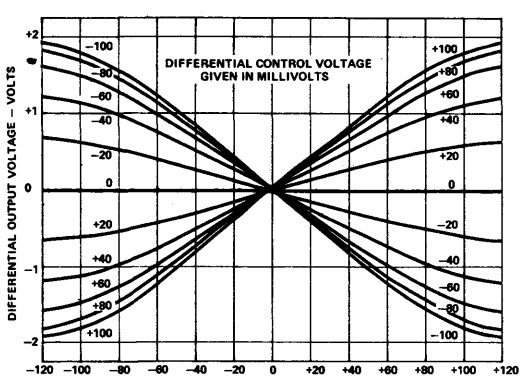

Figure 4. Multiplier Transfer Function.

BIASING CIRCUITRY

Key to the utility of the SG1402 is the inclusion of all the biasing and level shifting circuitry normally required as external components. This is provided by matched current sources and low impedance voltage sources.

Resistors R1, R2, R3 and R4 are directly across the supply voltage and establish a current:

$$I_b = \frac{V_S - V_{BEQ1}}{R1 + R2 + R3 + R4} = 1\ \text{mA at 10 volts}$$

Transistors Q14 and Q16 have the same geometries and emitter resistors as Q1 and therefore, with the same base voltage, they each are also conducting one milliamp and provide the loads for the output emitter followers, Q13 and Q15. This saves chip area as a transistor requires less space than a resistor which would establish the same current.

Transistor Q8 has four times the emitter area and ¼ the emitter resistor as Q1 and thus defines a current level I_0 of 4 milliamps.

The bias voltage levels required at different points in the circuit are all defined by the same resistors which set the current levels but there is no mutual interaction due to the insertion of Q2 and Q3 which act as low-impedance isolators.

Transistors Q4 and Q11 serve only as common-base stages to isolate the load resistor from the collector capacitance of the parallel diff-amp transistors. Thus, frequency response is improved with only slight increase in circuit complexity.

The chip layout of the SG1402 was done to optimize the component matching regardless of mask registration and process variations. From the photomicrograph shown in Figure 5, it can be seen how the symmetrical nature of the circuit was exploited to obtain matched parameters. The chip has an area of 48 by 39 mils.

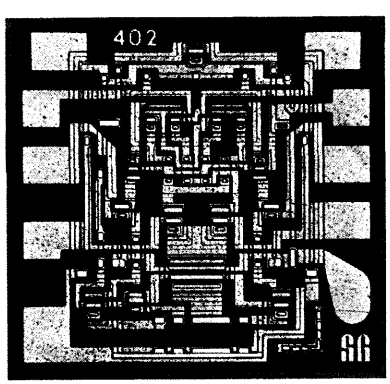

Figure 5. Photomicrograph of SG1402 Chip.

VARIABLE GAIN AMPLIFICATION

The circuit of Figure 6 shows the simplest application of the SG1402 as a single-ended, variable-gain amplifier. The signals at the two outputs are always equal in magnitude and opposite in phase. As the gain control potentiometer is moved from one end to the other, each output will start with a maximum signal, reduce to a minimum when the pot is centered, and increase to maximum again in the opposite phase as the wiper gets to the other end of the potentiometer.

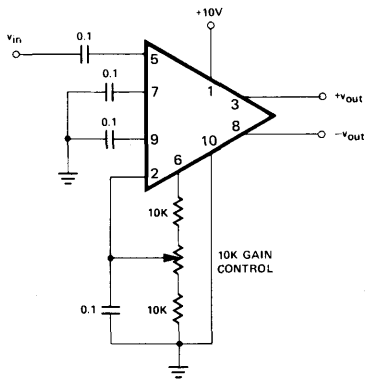

Figure 6. Single-Ended Variable-Gain Amplifier Configuration with Manual Gain Control to Provide Maximum Output of Either Phase.

For applications where a phase change is not desired, the incorporation of a diode as shown in Figure 7 will allow a DC control voltage to vary the input-output transfer function from a gain of +25 dB to an attenuation of −25 dB. This relationship is plotted in the graph of Figure 8.

Since this change in transfer function is accomplished with no net change in either operating currents or bias levels, it is transient-free and extremely fast-reacting. Thus, the circuit of Figure 7 may also be used as a gated amplifier with the control requirements compatible with 0 to 5 volt logic levels. The waveform in Figure 9 shows a 1 MHz signal controlled with a 10 microsecond pulse.

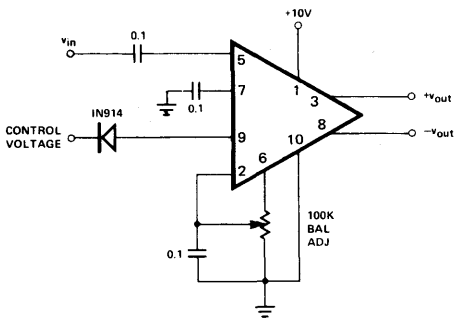

Figure 7. Addition of Diode Provides Gain Control Without Phase Change. Balance May be Eliminated if Maximum Attenuation is not Required.

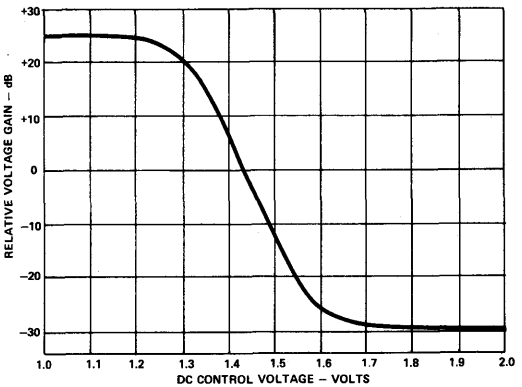

Figure 8. Gain Variation as a Function of Control Voltage with Diode Coupled Input.

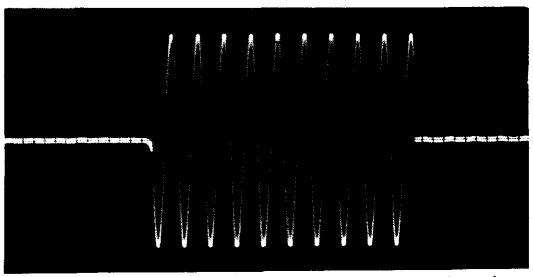

Figure 9. Gate Amplifier or Pulse Modulator Response. Input is 10 mVrms, 1 MHz and Control Voltage is 0 to 5 Volt Square Wave with f = 50 kHz.

MODULATION

The multiplying function of the SG1402 can be used to provide both balanced and amplitude modulation utilizing the basic circuit shown in Figure 10. With the potentiometer adjusted for optimum balance, the carrier signal is canceled out producing a doublesideband waveform at the output. Depending upon the amplitude of the carrier signal, higher frequency harmonics can also be generated; however, if only the lower sideband is used, filtering of the upper sideband will also eliminate all the harmonics. It should be noted that this balanced modulation is achieved without the need for the usual transformers and only capacitive coupling is required. Typical waveforms are shown in Figure 11.

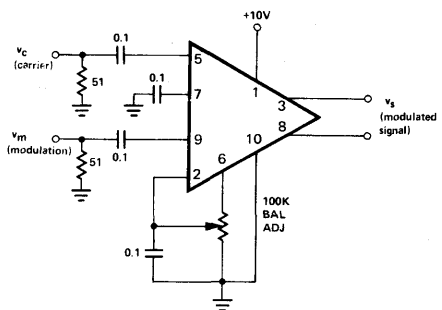

Figure 10. Balanced Modulator.

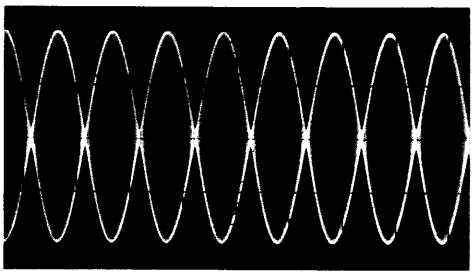

Figure 11. Balanced Modulator Output Waveform. (0.1V/cm, 50 μs/cm, f_c = 1 MHz, f_m = 10 KHz).

If the potentiometer is adjusted so that the circuit is unbalanced, then the carrier is included in the output signal and amplitude modulation as shown in Figure 12 results. The optimum adjustment can most readily be made while observing the output waveform on an oscilloscope. Care should be taken that neither signal overdrive the circuit.

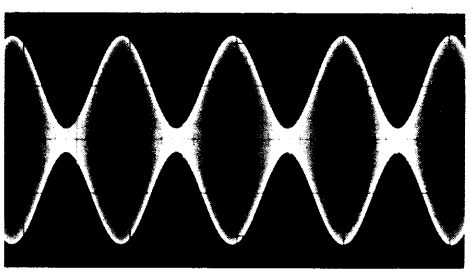

Figure 12. Amplitude Modulator Output Waveform. (0.2V/cm, 50 μs/div, f_c = 1 MHz, f_m = 10 KHz).

By using a signal to modulate itself with the circuit shown in Figure 13, the input is squared and since

$$\cos^2 \omega t = \tfrac{1}{2} [1 + \cos 2 \omega t]$$

the output frequency is twice that of the input. Typical waveforms for this frequency doubler application are shown in Figure 14.

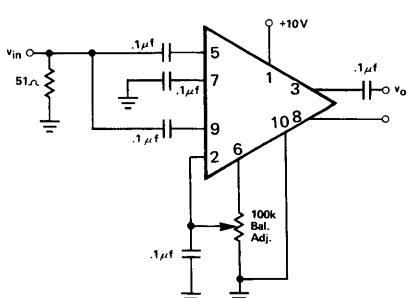

Figure 13. Frequency Doubler.

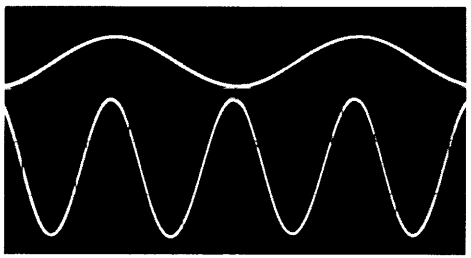

Figure 14. Frequency Doubler Input and Output Waveform. (50mV/cm, 0.2 μs/div, f_1 = 1 MHz, f_2 = 2 MHz).

DEMODULATORS

The same features which make the SG1402 an excellent modulator provide superior performance when the circuit is used as a single or double sideband demodulator. The circuit of Figure 15 illustrates the simplicity of this application. The balance pot is not necessary since the inserted carrier is eliminated by the low-pass filter at the output.

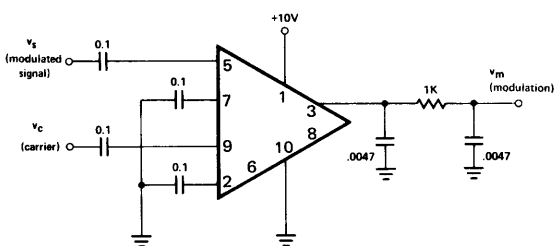

Figure 15. Balanced Demodulator.

The same general approach may be used for amplitude modulation and a block diagram of a simple AM detector is shown in Figure 16. Thus, the SG1402 can be used in receivers which combine SSB and AM to provide complete signal transformation in either mode of operation.

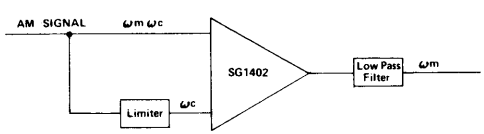

Figure 16. AM Detector Block Diagram.

CONCLUSIONS

With the introduction of the SG1402, Silicon General has provided a powerful tool to the communications engineer and all others working with information processing. Because of its versatility and capability, this device opens the way to a much greater utilization of carrier transmission schemes for data handling in applications ranging from outer space to home kitchens.

CIRCUIT OPERATION

The first IC to combine a positive and negative voltage regulator on a single chip was the SG1501, and this device has since been supplemented with three new tracking regulator designs – the SG1502, the SG1501A, and the SG1568.

All four of these tracking regulators operate in a similar manner which is best visualized through the block diagram shown in Figure 1. This circuit is fundamentally a tracking regulator. That is, the negative voltage is regulated and the positive output tracks the negative. (Note: In the SG1568, the circuit is reversed in that the negative side tracks the regulated positive output; however, the principle is the same.) Negative regulation is accomplished by providing a constant-voltage reference for the negative error amplifier, but the reference input to the positive error amplifier is grounded. This amplifier forces its other input, which is the center-tap between equal resistors, to also be at zero volts, thus requiring the positive output to be equal in magnitude but opposite in polarity to the negative output.

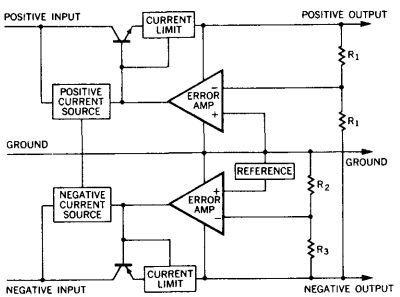

Figure 1. Block Diagram

With this technique, a single adjustment of the negative voltage divider – which changes the negative output level – will also provide exactly the same change to the positive output voltage. This tracking will hold all the way from approximately one volt above the reference voltage to a maximum value of about two volts less than the input supply voltage.

DESIGNER'S CHOICE

With four IC's to choose from some discussion of the significant features of each type is in order. Three of the devices, the SG1501A, the SG1501 and the SG1568 are factory set at ±15V regulators while the fourth, the SG1502, is user-adjusted to provide outputs from ±8V to ±28V.

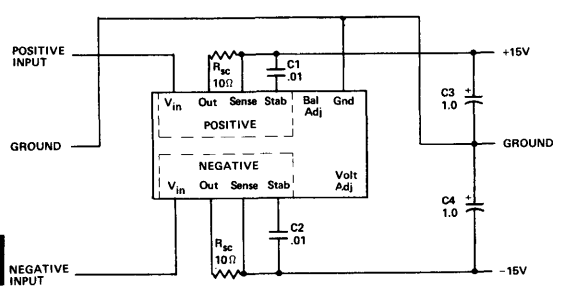

Figure 2. Basic ±15V, 50 mA Regulator

The SG1501 and SG1501A are interchangeable and both can be used by themselves to provide load currents to the maximum defined by package dissipation, or can be combined with external pass transistors for currents in excess of two amps. Both devices feature constant current limiting with the value set by an external resistor. The SG1568 is similar in all respects to the SG1501 except that it is frequency compensated in a slightly different way.

The SG1502 uses the same basic circuit as the SG1501 but has two important differences. First, the voltage setting resistors are external to the device providing greater flexibility in adjusting the output voltage levels to other than ±15V. Secondly, the current limit circuitry has been changed to allow its use in a foldback mode. Foldback current limiting provides for a short circuit current value less than the maximum load current and is a significant feature when the major power dissipation is in external pass transistors rather than the IC.

Self-contained thermal shutdown is the primary improvement offered by the SG1501A although increases in both the maximum input voltage and load current have also been made. With thermal shutdown, temperature sensing circuitry on the chip is designed to turn off the output current when the junction temperature exceeds a safe limit – typically 170°C. The significance of this feature is that the designer now need not design around short-circuit power dissipation limits – the device will take care of itself. Since short-circuit power is typically more than twice as much as maximum operating power, this means a two-times, or better, improvement in load current is possible. It should be noted that even with thermal limiting circuitry, the maximum current must be controlled to allow time for this protection to react.

APPLICATIONS

The simplest way to use the SG1501 and SG1501A is in the basic circuit shown in Figure 2. In this form, the device will handle 50 to 100 mA, depending on the heat sinking (more about this later) and will provide ±15V outputs with typically less than two millivolts of sensitivity to either line or load variations. Because of this excellent line regulation, there is no need for symmetrical input supply voltage levels. The only requirement is that each level be greater than its associated output and that the total voltage between positive and negative supplies be less than 60V (70V for the SG1501A). The minimum input voltage is defined by the regulator dropout characteristics shown in Figure 3.

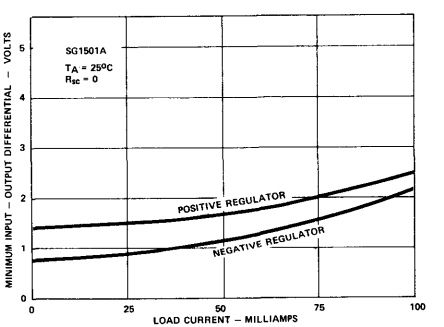

Figure 3. Regulator Dropout Voltage

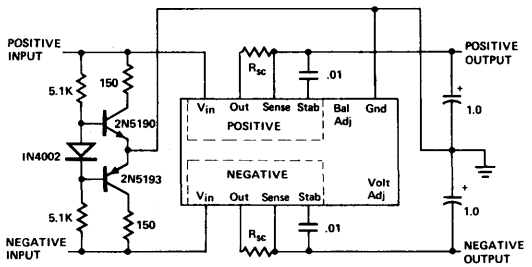

Figure 4. Artificial ground for use with an ungrounded or single level voltage.

When operating from a single voltage source, an ungrounded supply is required. An artificial ground can be provided as shown in Figure 4. In this circuit, the external transistors will conduct as necessary to accommodate unbalanced load requirements and while the outputs will float between the two input levels, they will be held constant with respect to this artificial ground.

CURRENT LIMITING

Current sensing is provided by transistors Q12 and Q13 (see schematic, Figure 5) which are normally held off by an external base-to-emitter resistor, Rsc. When the load current passing through this resistor develops enough voltage, the transistor turns on and diverts drive current away from the series pass transistors. The sense voltage is equal to approximately 0.6V at Tj = 25°C, but it is temperature dependent decreasing to 0.4V at 125°C as shown in Figure 6. Note that it is junction temperature that determines the sense level, and thus increasing the power dissipation within the circuit can lower the value at which limiting will occur. The value of the limiting resistor, Rsc, should be selected by:

$$Rsc = \frac{\text{Sense Voltage at Maximum Tj}}{\text{Allowable Short Circuit Current}}$$

where, for maximum regulation, the allowable short circuit current should be at least 20% more than the maximum expected load current.

Under some conditions, a low-level oscillation may be present on the negative side when the device goes into current limiting. Should this be a problem, it may be eliminated by by-passing Rsc with a capacitor whose value is such that the time constant, Rsc C, is equal to 10 x 10^{-6} second. This capacitor, as well as the output capacitors, C3 and C4, must be low ESR types such as solid tantalum.

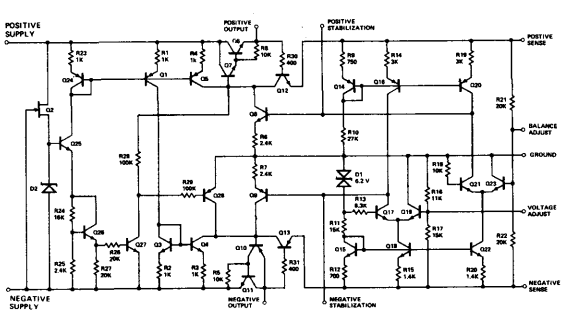

Figure 5. SG1501A Schematic Diagram

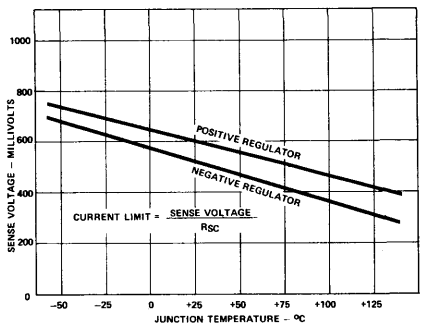

Figure 6. Current Limiting Characteristics

POWER CONSIDERATIONS

Although these dual regulators are designed to handle large load currents and high input voltages, the product of the two can easily exceed the maximum total device dissipation allowed by the package. The functional limitation which should be considered for each application is that for maximum reliability the junction temperature of the chip should not exceed 170°C. This is usually derated to give a maximum design operating Tj of 150°C.

To evaluate the maximum junction temperature possible in a given application, the following three parameters must be known:

1. The power dissipation within the chip
2. The thermal resistance from junction to ambient (or heat sink)
3. The ambient (or heat sink) temperature

The power dissipation within the chip is equal to the sum of the input voltage times the standby current plus the input-output voltage differential times the load current, for each side of the regulator. For example, the total power dissipation for ±20V inputs, ±15V outputs, and 50 mA load currents is:

Pd = 20 (2) + 20 (3) + 5 (50) + 5 (50)
= 100 mW standby + 500 mW load current
= 600 mW

The thermal resistance is the resistance to heat flow from the junction to the ultimate heat sink. For parts mounted in the open, still air, the thermal resistance (θjA) is equal to 185°C/watt for the TO-100 metal can and 125°C/watt for the TO-116 ceramic DIP. Blowing air across the package, or the use of some form of heat radiator can significantly reduce these numbers. For example, the use of IERC's model TXBF-032-025B top hat radiator on the TO-100 package, reduces θjA to 130°C/watt, while their model LIC-214A-2B radiator for the TO-116 will give an θjA of 50°C/watt for that package. Finally, a perfect heat sink reduces θjA to θjC which is 50°C/watt for the TO-100 and 20°C/watt for the TO-116.

With the above information, the maximum power handling capability of the package can be determined as follows:

1. Calculate the maximum allowable junction temperature rise:

   $\Delta Tj = 150^{0}C - T_A$ (max)

2. Calculate the power availability:

   $Pd = \Delta Tj/\theta jA$

3. From this number, subtract the maximum standby dissipation:

   $Psb = (V+ \text{ max})\ (Isb+) + (V- \text{ max})\ (Isb-)$

4. The remainder can be used to determine the maximum load current as a function of input-output voltage differential.

The curves of Figure 7 show these relationships for each package under the assumptions of 25°C ambient, and symmetrical input and output voltages and load currents.

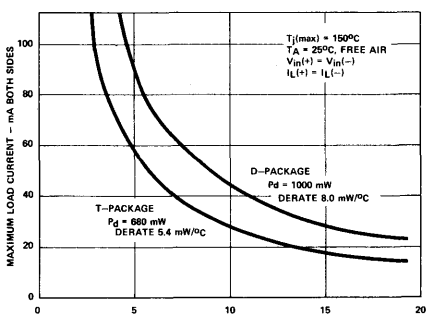

Figure 7. Maximum Current Capability

EXTERNAL POWER TRANSISTORS

Additional current handling capability may be provided through the use of external power transistors in the configuration shown in Figure 8. In this circuit, the 75 ohm base-to-emitter resistors provide a path for the regulator standby current and should not be increased in value. An additional consideration is the use of solid tantalum output capacitors as most common electrolytic types have too high an equivalent series resistance, particularly at high frequencies.

The power transistors are not critical and can be selected on the basis of current and voltage capability, and on mechanical requirements for practical heat sinking. Note that only one transistor need be used if only one side has excessive load current. Although low-frequency devices will minimize the risk of oscillation, unique transistor characteristics may require a small capacitor (0.1 mfd) from base to ground or a larger value (5 mfd) from base to emitter for complete stability.

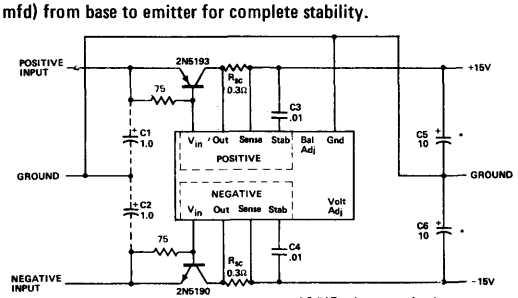

Figure 8. High Current Configuration, One Amp Output

FOLDBACK CURRENT LIMITING

With constant-current limiting as shown in Figure 8, the power dissipation in the pass transistors under short circuit conditions can be substantial. Here, the thermal limiting feature of the SG1501A can't do much good since it senses the IC temperature rather than the external transistors. To eliminate the problem of having to heat sink a short circuit power two to three times normal operating levels, the use of the SG1502 in the circuit of Figure 9 should be considered. The dividers of R5 and R6 pre-bias the current limiting such that when the output is shorted, the maximum current is substantially reduced from its normal operating level. The values for R5 and R6 are most easily determined from an itterative solution of the equations below with the trade-off being that a greater amount of foldback requires a larger voltage drop across Rsc:

$$\text{Max Load Current} \approx \frac{\text{Sense Voltage} + \frac{R5}{R6} Vo}{Rsc}$$

$$\text{Short Circuit Current} \approx \frac{\text{Sense Voltage}}{Rsc}$$

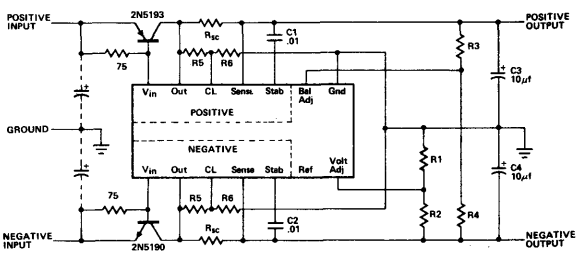

Figure 9. Foldback Current Limiting

VOLTAGE ADJUSTMENTS

With both output voltage levels internally set for 15V, (±200 mV for the SG1501/2501 and ±500 mV for the SG3501) these devices require no additional resistors for many applications. It is possible, however, to externally vary the output voltages from ±10 to ±23V by using external resistors to shunt one or both of the internal resistors which set the negative output level. The positive output will, of course, track the negative value.

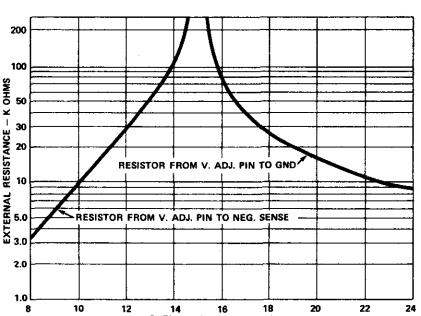

Figure 10. External parallel resistor required for voltages other than ±15V.

The simplest way of changing the output levels is to use a single resistor

in parallel with R17 (see Figure 5) for voltages less than 15V and in parallel with R16 for voltages above 15V. The graph of Figure 10 shows the approximate value to use in either case.

This method of adjusting output levels has one disadvantage, however. Diffused resistors have a positive temperature coefficient and while they can be made to track each other extremely well, with one of them shunted this tracking becomes degraded. A method offering greater temperature stability is the use of a pair of resistors with values low enough to swamp out the internal divider. By shunting R16 with 1.2k, and R17 with a resistor selected by:

$$R17'' = \frac{1.2\,(Vo - 6.2)}{6.2}\ k\Omega$$

where Vo is the desired output voltage, a four-fold improvement in temperature performance is achieved at the expense of the additional divider current. Figure 11 shows that temperature variation which may be expected both with a single shunt resistor and with a divider drawing approximately five milliamps of current. Note that these temperature shifts are caused by changes in chip temperature which could result from variations of either ambient temperature or internal power dissipation.

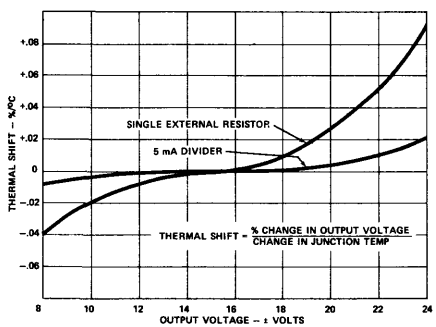

Figure 11. Temperature Coefficient of Output Voltage

In the 14 pin dual-in-line package, a connection is provided to the junction of R21 and R22. An external resistor divider can be used here in the same manner to either balance the two outputs so that they are exactly equal in magnitude or to unbalance them for non-symmetrical output levels.

Although all of these dual regulator types have provisions for adjustment of the output voltage levels, with its user-supplied voltage setting resistors, the SG1502 is the best choice for applications very far from ±15V. The divider resistors (see Figure 9) are selected as follows:

$$\text{Negative Vo} = \frac{6.2\,(R1 + R2)}{R1}$$

$$\text{Positive Vo} = \frac{R3}{R4}\ (\text{Negative Vo})$$

One common application for positive and negative voltages is as a power source for the widely used 710 and 711 IC voltage comparators. Since these devices are designed for +12 and –6V operation, it takes a circuit as shown in Figure 12 to get around the ± 8V minimum output limitation of these regulators. Here, the nominal ±15V output of the SG1501 has been reduced to ±12V by the 2.0k and 1.8k voltage divider. Six volts are then subtracted from the negative output by the IN4735 zener diode. Because the diode is outside the feedback loop, some minor variations in the –6V output may be observed due to its temperature coefficient or dynamic impedance. These variations have negligible effect on the comparators, however, as the negative voltage is used only to bias high impedance current sources.

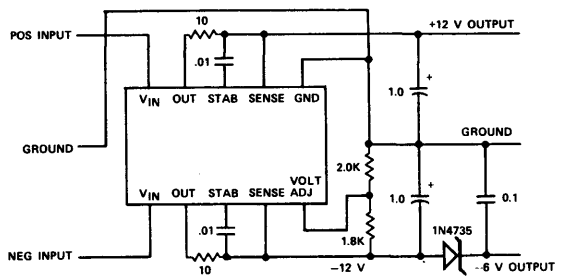

Figure 12. Using the SG1501 to provide +12 and –6V outputs.

Zener diodes can also be put to use in applications requiring high input voltages. In the circuit of Figure 13, the small signal zener diodes reduce the voltage applied to the IC while allowing the easily heat-sinked power transistors to absorb the added power dissipation caused by a large input-output differential.

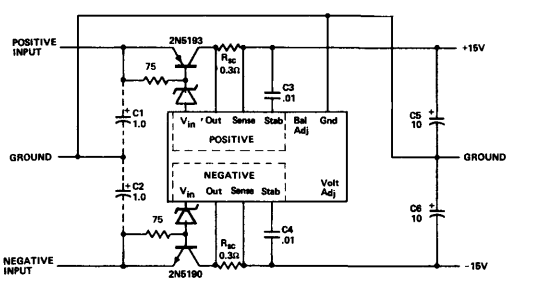

Figure 13. Zener diodes used to prevent high input voltages from appearing across the device.

CONCLUSIONS

With two complete regulators in a single IC, these new regulators offer an improved approach to power distribution. Their high degree of performance and freedom from large numbers of external components make "on-card", or distributed regulation a practical reality. By regulating at the point of use, the system designer has eliminated many knotty problems such as lead inductance, decoupling, line drop through connectors, etc. In addition, since each circuit card or module can now regulate its own voltage, complete interchangeability is more nearly assured and the problems of equipment maintenance are greatly eased.

SIMPLIFYING CONVERTER DESIGN WITH A NEW INTEGRATED REGULATING PULSE WIDTH MODULATOR

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Edited by Stan Dendinger
Manager, Advanced Product Development
SILICON GENERAL, INC.

Abstract

A new monolithic integrated circuit is described which contains all the control circuitry for a regulating power supply converter or switching regulator. Included in this 16-pin dual-in-line package is the voltage reference, error amplifier, oscillator, pulse width modulator, pulse steering flip-flop, dual alternating output switches, and current limiting and shutdown circuitry. This device can be used for switching regulators of either polarity, transformer coupled DC to DC converters, transformer-less voltage doublers and polarity converters, as well as other power control applications.

INTRODUCTION

Implementing a switching power supply has just become significantly easier with the introduction of the SG 1524 series of Regulating Pulse Width Modulator integrated circuits. Long recognized as offering greatly improved efficiencies, the development of switching supplies has been hampered by the complexity of the low-level circuitry required to provide the proper signals for adequate control of the switching transistors. As a result, these supplies have tended to be more costly, larger in size, and with poorer reliability than could be justified by their improved efficiency. Even when threats of higher energy costs and potential brown-outs have made switching supplies mandatory, their complexity has made the engineering design task a most formidable undertaking.

With the introduction of the SG 1524, a major portion of the complex low-level control circuitry has been integrated into a single LSI linear integrated circuit. This monolithic chip, packaged in a 16-pin dual-in-line outline, implements the entire block diagram shown in Figure 1.

It is the integration of all these different functions into a single IC that qualifies the SG 1524 as one of the best examples to date of large scale integration as applied to analog circuits. The remainder of this paper will describe each of the individual blocks in the following diagram in considerable detail and then offer a few basic application suggestions.

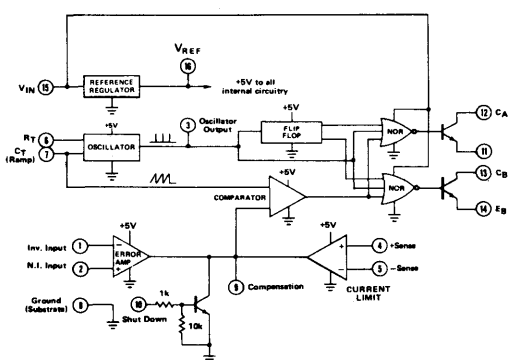


FIGURE 1 – SG1524 BLOCK DIAGRAM

VOLTAGE REFERENCE

The reference circuit of the SG 1524 is shown in Figure 2. This is a complete linear regulator designed to provide a constant 5 volt output with input voltage variations of 8 to 40 volts. It is internally compensated and short circuit protected. It is used both to generate a reference voltage and as the regulated source for all the internal timing and controlling circuitry. This regular may be bypassed for operation from a fixed 5 volt source by connecting pins 15 and 16 together to the input voltage. In this configuration, the maximum input voltage is 6 volts. While discussing input power, it should be mentioned that the entire SG 1524 IC draws less than 10 mA of current, regardless of input voltage.

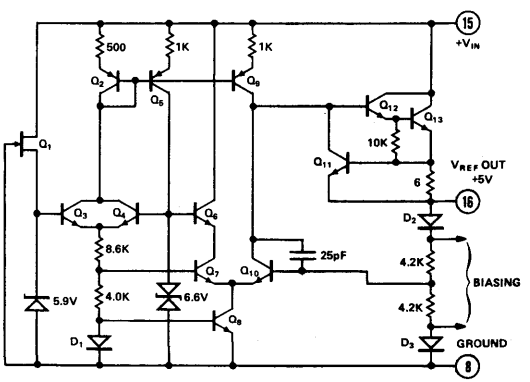


FIGURE 2 – SG1524 REFERENCE CIRCUIT

This reference regulator may be used as a 5 volt source for other circuitry. It will provide up to 20 mA of output current itself and can easily be expanded to higher currents with an external PNP transistor as shown in Figure 3.

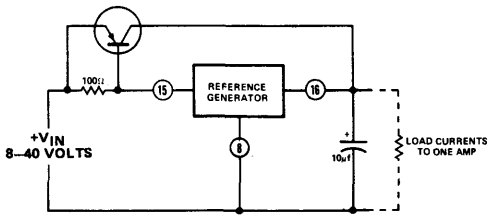


FIGURE 3 – SG1524 EXPANDED CURRENT SOURCE

OSCILLATOR

The oscillator in the SG 1524 uses an external resistor (R_T) to establish a constant charging current into an external capacitor (C_T). This constant-current charging gives a linear ramp voltage which provides an overall linear relationship between error voltage and output pulse width. The SG 1524 oscillator circuits is shown in Figure 4.

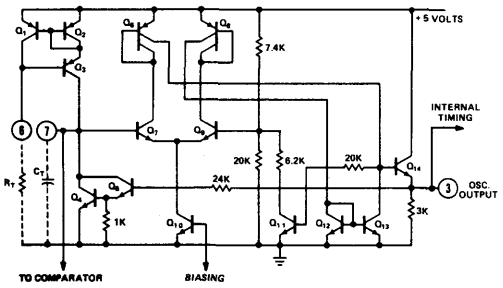


FIGURE 4 – SG1524 OSCILLATOR CIRCUIT

A second output from the oscillator is a narrow clock pulse which occurs each time C_T is discharged. This output pulse is used for several functions as outlined below:

(1) As a blanking pulse to both outputs to insure that there is no possibility of having both outputs on simultaneously during transitions. The width of this blanking pulse can be controlled to some extent by the value selected for C_T.

(2) As a trigger for an internal flip-flop which directs the PWM signal to alternate between the two outputs. Note that for single-ended applications, the two outputs can be connected in parallel and the frequency of the output is the frequency of the oscillator. For push-pull applications, the outputs are separated and the action of the flip-flop provides and output frequency ½ that of the oscillator.

(3) As a convenient place to synchronize an oscilloscope for system de-bugging and maintenance.

(4) As a bi-directional port for external timing synchronization. The output pulse from this oscillator — which is stable to within 2% over variations in both input voltage and temperature — can be used as a master clock for other circuitry, including other SG 1524's. It thus follows that a positive pulse applied to this terminal can synchronize the SG 1524 to an external clock signal.

The waveforms of the two outputs from the oscillator are shown in Figure 5.

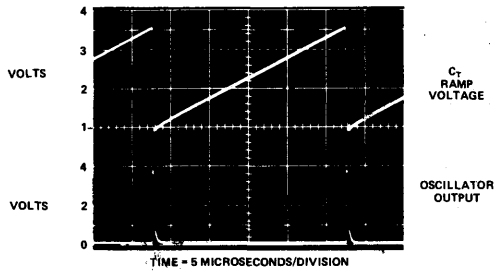


FIGURE 5 – SG1524 OSCILLATOR WAVEFORMS

ERROR AMPLIFIER

The error amplifier circuit, shown in Figure 6, is a simple differential input, transconductance amplifier. Both inputs and the output are available for maximum versatility.

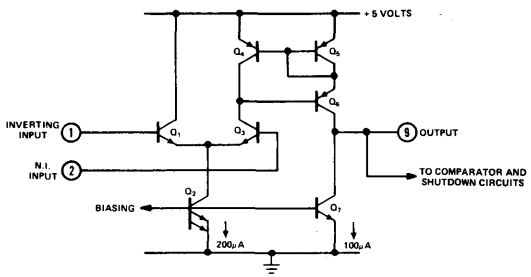


FIGURE 6 – SG1524 ERROR AMPLIFIER SCHEMATIC

The gain of this amplifier is nominally 10,000 (80dB) but can be easily reduced by either feedback or by shunting the output to ground with an external resistor. The overall frequency response of this amplifier which, by the way, is not internally compensated but yet is stable with unity gain feedback, is plotted with various values of external load resistance in Figure 7.

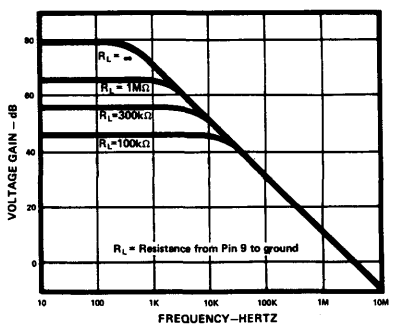


FIGURE 7 – SG1524
ERROR AMP FREQUENCY RESPONSE

Phase shifting to compensate for an output filter pole may readily be accomplished with an external series R-C combination at the output terminal of the amplifier.

Since the error amplifier is powered by the 5-volt reference voltage, the acceptable common-mode input voltage range is restricted to 1.8 to 3.4 volts. This means the reference must be divided down to be compatible with the amplifier input, but yet provides the advantage of being able to be used to regulate negative output voltages. required input dividers are shown in Figure 8.

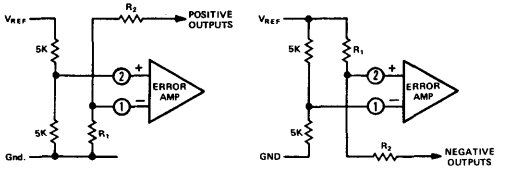


FIGURE 8 – ERROR AMPLIFIER CONNECTIONS

Since this amplifier is a transconductance design, the output is a very high impedance (approximately 5 MΩ) and can source or sink only 100 microamps. This makes the output terminal (Pin 9) a very convenient place to insert any programming signal which is to override the error amplifier. Internal shutdown and current limit circuits are connected here, but any other circuit which can sink 100 μA can pull pull this point to ground, thereby shutting off both outputs.

For example, the soft start circuit of Figure 9 can be used to hold Pin 9 to ground — and thus both outputs off — when power is first applied. As the capacitor charges, the output pulse slowly increases from zero to the point where the feedback loop takes control. The diode then isolates this turn-on circuit from whatever frequency stabilizing network might also be connected to Pin 9.

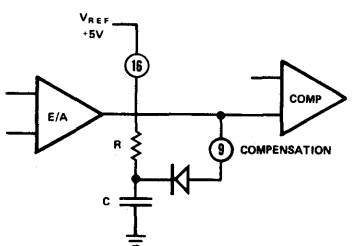


FIGURE 9 – SG1524 SOFT START CIRCUITRY

CURRENT LIMITING

The current limiting circuit, while shown in the block diagram as an op amp, is really only a single transistor amplifier as shown in Figure 10. It is frequency compensated and has a second transistor to provide temperature compensation and a reduction of input threshold to 200 mV. When this threshold is exceeded, the amplifying transistor turns on and, by pulling the output of the error amplifier toward ground, linearly decreases the output pulse width. One consideration in using this circuit is that the sense terminals have a ± 0.3 volt common mode range which requires sensing in the ground line. However, since differential inputs are available, foldback current limiting can be implemented as shown in Figure 11.

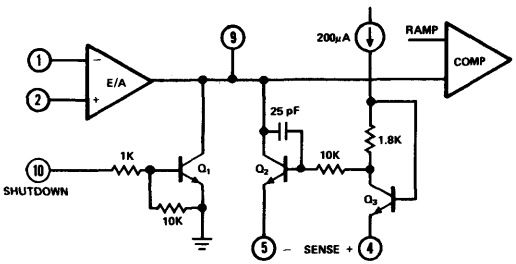


FIGURE 10 – SG1524 CURRENT LIMITING

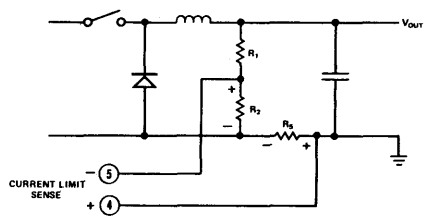


FIGURE 11 – FOLDBACK CURRENT LIMITING

While on the subject of protection circuitry, although overvoltage protection is not built into the SG 1524, it is relatively easy to add by using the internal shutdown circuit in conjunction with a few external components as shown in Figure 12.

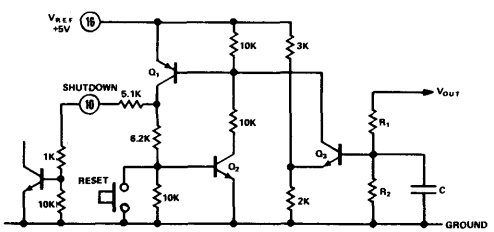


FIGURE 12 – SG1524 OVER VOLTAGE PROTECTION

This circuit will provide a low level sensing and latching function and while it won't protect against a shorted output transistor, it will remove the drive signals with no power dissipation.

OUTPUT STAGES

The outputs of the SG 1524 are two identical NPN transistors with both collectors and emitters uncommitted. These circuits are as shown in Figure 13 and include an antisaturation network for fast response and current limiting set for a maximum output current of approximately 100 mA.

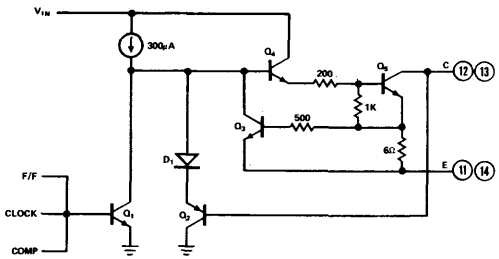


FIGURE 13 – SG1524 OUTPUT STAGE

The availability of both collectors and emitters allows maximum versatility to enable driving either NPN or PNP external transistors; however, it must be remembered that this is only a switch which closes and opens. Power transistor turn-off drive must be developed externally. Some suggestions for output drive circuits are shown in Figure 14.

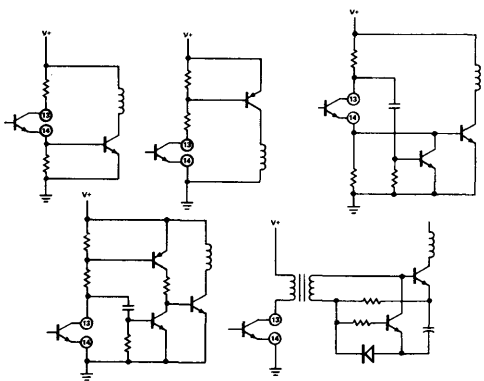


FIGURE 14 – DRIVING EXTERNAL TRANSISTORS

APPLICATIONS

In considering applications for the SG 1524, it appears that there are three general classifications of switching power supply systems. Included in the first are the transformerless voltage multiplier circuits shown in Figure 15. These circuits are primarily used for low level applications but can step up, step down, or change the polarity of an input voltage. The switches shown can be either the output stages of the SG 1524 or external transistors. Note that one extra diode is required to protect the emitter-base junction of switch S_A during the times when both switches are open.

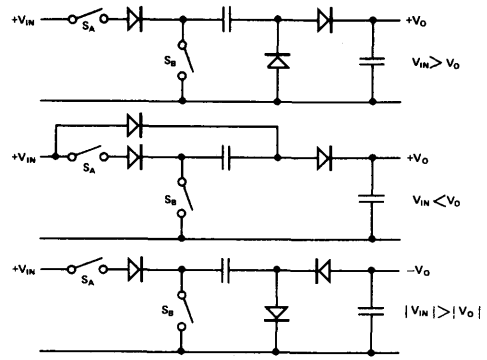


FIGURE 15 – CAPACITOR/DIODE OUTPUT CIRCUITS

For higher current applications, the single-ended inductor circuits of Figure 16 represent another classification. Here the two outputs of the SG 1524 are connected in parallel, but note that this does not give twice the current as the switches are alternating internally. This does not affect external performance, however, and the SG1524 can be used to provide 0-90% duty cycle modulation in any of the configurations shown.

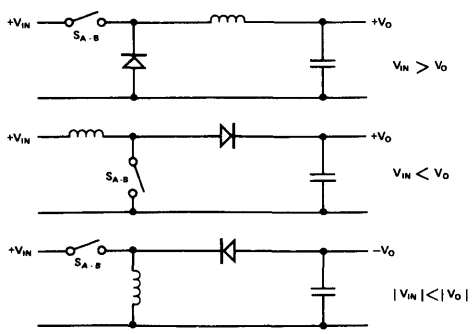


FIGURE 16 – SINGLE-ENDED INDUCTOR CIRCUITS

The third general classification of power supply systems are transformer coupled, two types of which are shwon in Figure 17.

The push-pull circuit represents the conventional DC to DC converter with each switch being controlled for 0 - 45% duty cycle modulation. The second transformer circuit is a single-ended flyback converter, useful at light loads without a separate output inductor.

To illustrate the use of the SG 1524 in each of the above general classifications, the following simple, but practical, circuits are presented:

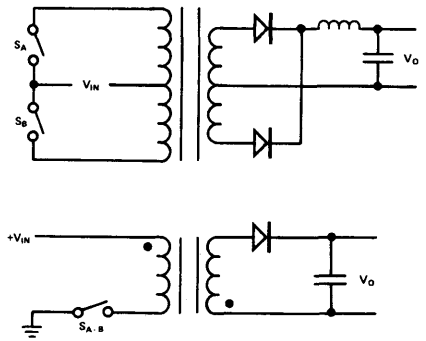


FIGURE 17 – TRANSFORMER COUPLED CIRCUITS

Figure 18 shows the use of the SG 1524 as a low current polarity converter providing a regulated −5 volt output at currents up to 20 mA from a single positive input voltage. The external components required include the divider resistors to interface the reference and output voltages with the error amplifier, a resistor/capacitor to set the operating frequency, and the output diodes and capacitors. The combination of the built-in current limiting of the SG1524 output stages and the capacitor coupling of the output signal provide full protection against short circuits and the current limit amplifier is unused. Since this circuit has no inductor, the output capacitor is more than enough to stabilize the regulating loop and no additional compensation is required.

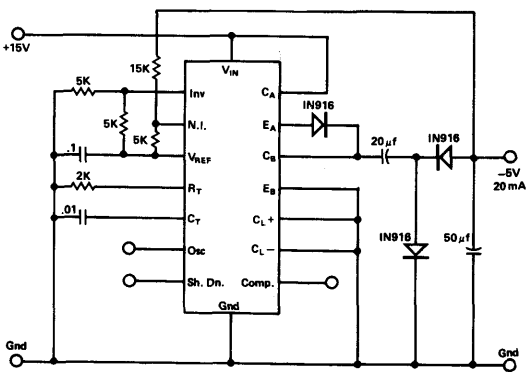


FIGURE 18 – LOW CURRENT POLARITY CONVERTER

Another low-level circuit is the flyback converter shown in Figure 19.

The circuit is designed to develop a regulated ±15 volt supply from a single +5 volt source. Note that the reference terminal is tied to the input, disabling the internal regulator. The error amplifier resistors are also tied to the input line so the output regulation can be no better than the input; however, an external reference could just as easily have been used.

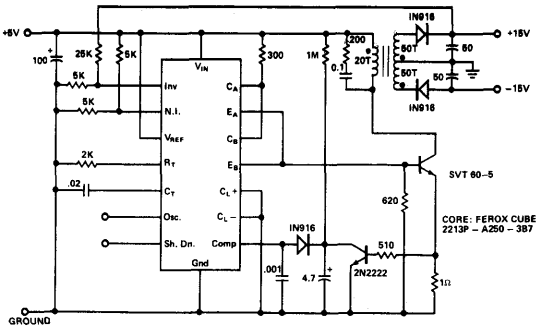


FIGURE 19 – +5 TO ±15 VOLT, FLYBACK CONVERTER

In this application, the two output stages are connected in parallel and used as emitter followers to drive a single external transistor. Since the currents in the secondary of a flyback transformer are out of phase with the primary current, current limiting is very difficult to achieve. In this circuit, protection was provided through the use of a soft-start circuit. If either output is shorted, the transformer will saturate, providing more current through the drive transistor. This current is sensed and used to turn on the 2N2222 which resets the soft-start circuit and turns off the drive signal. If the short remains, the regulator will repetitively try to start up and reset with a time constant set by the soft-start circuit. Removing the short will then allow the regulating loop to re-establish control.

For higher current applications, the single-ended conventional switching regulator of Figure 20 is shown.

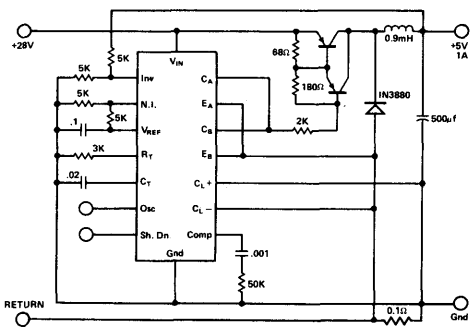


FIGURE 20 – 1 AMP, SINGLE-ENDED SWITCHING REGULATOR

In this case, an external PNP darlington is used to provide a 1-amp current switch. The SG1524 has the two outputs in parallel, connected as a grounded emitter amplifier. The current sense resistor is inserted in the ground line and the voltage across it used for constant current limiting. Note that in addition to the divider resistors and frequency setting R_TC_T, a phase compensation resistor and capacitor is used to stabilize the loop now that an inductor has been added.

A fourth application would have to be a push-pull, DC to DC regulating converter as shown in Figure 21.

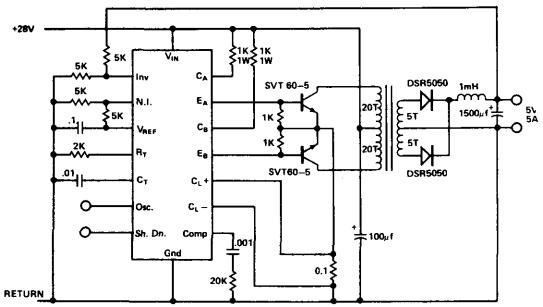


FIGURE 21 – 5V, 25W, DC TO DC CONVERTER

Here the outputs of the SG 1524 are connected as separate emitter followers driving external transistors. Current limiting in this application is done in the primary for several reasons: First, it's easier to live within the ±0.3 volt common mode limits of the current limit amplifier; second, since this is a step-down application, the current — and therefore the power in the sense resistor — is lower; and third, if the output drive were to become non-symmetrical causing the transformer to approach saturation, the resultant current spikes will shorten the pulse width on a pulse-by-pulse basis, providing a first order correction. Note that the oscillator is set to run at 40kHz to obtain a 20 kHz signal at the transformer.

This application as shown does not provide input-output isolation and, of course, that feature is difficult to achieve within a single IC. There are a couple of ways the SG 1524 can be used with isolated power supply systems, however. The first is shown in Figure 22 where the SG 1524 is direct coupled on the secondary side of the output transformer. The outputs from the IC are transformer-coupled back to the primary side to drive the switching transistrors. Of course, a separate start-up power source is needed for the SG 1524 but that shouldn't present much of a problem remembering that the IC draws less than 10 mA of supply current.

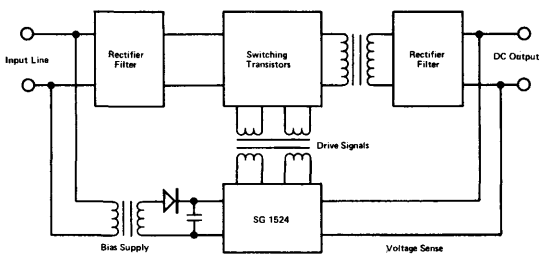


FIGURE 22 – INPUT/OUTPUT ISOLATION

A different method of providing isolation is shown in Figure 23 where the IC is direct coupled on the primary side. Here a separate reference and error amplifier (most easily implemented with a SG 1532 regulator IC) is connected on the secondary and then optically coupled back to the primary side.

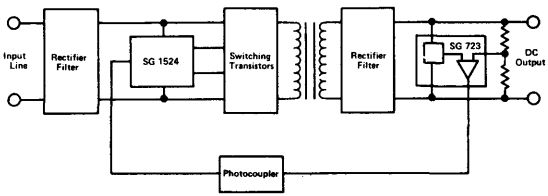


FIGURE 23 – INPUT/OUTPUT ISOLATION

As should be evident from the above, the SG 1524 was designed as the first of what will undoubtedly become a larger family of regulator ICs specifically designed for switching power supplies. As such, versatility was the primary design goal of this device and hopefully this goal has been achieved to the degree that will allow the SG 1524 to find application to a wide range of power control systems.

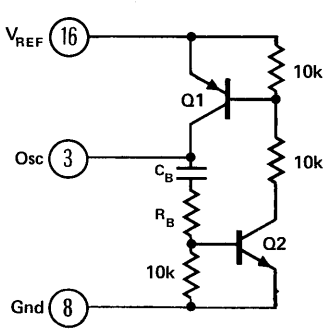
DEADBAND CONTROL WITH THE SG1524 REGULATING PULSE WIDTH MODULATOR CIRCUIT

The SG1524 Regulating P.W.M. integrated circuit provides two outputs which alternate in turning on for push-pull inverter applications. The internal oscillator sends a momentary blanking pulse to both outputs at the end of each period to provide a deadband so that there cannot be a condition when both outputs are on at the same time. The amount of deadband is determined by the width of the blanking pulse appearing on pin 3 and can be controlled by four techniques:

1. For 0.2 to 1.0 microseconds, the deadband is controlled by the timing capacitor, C_T, on pin 7. The relationship between C_T and deadband is shown in Figure 3 on the SG1524 data sheet. Of course, since C_T also helps determine the operating frequency, the range of control is somewhat limited.

2. For 0.5 to 3.0 microseconds, the blanking pulse may be extended by adding a small capacitor from pin 3 to ground. The value of the capacitor must be less than 1000 pf or triggering will become unreliable.

3. For longer and more well-controlled blanking pulses, a simple one-shot latch similar to the circuit shown below should be used:



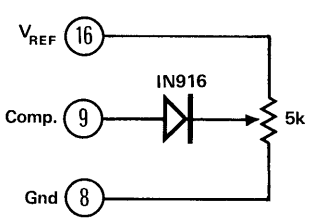
TRANSISTORS — Small-signal general purpose types.
For 5 μsec width, C_B = 200 pf, R_B = 10k

When this circuit is triggered by the oscillator output pulse, it will latch for a period determined by $C_B R_B$ providing a well-defined deadband.

Another use for this circuit is as a buffer when several other circuits are to be synchronized to one master oscillator. This one-shot latch will provide an adequate signal to insure that all the slave circuits are completely reset before allowing the next timing period to begin.

Note that with this circuit, the blanking pulse holds off the oscillator so its width must be subtracted from the overall period when selecting R_T and C_T.

4. Another way of providing greater deadband is just to limit the maximum pulse width. This can be done by using a clamp to limit the output voltage from the error amplifier. A simple way of achieving this clamp is with the circuit below:



This circuit will limit the error amplifier's voltage range since its current source output will only supply 100μA. Additionally, this circuit will not affect the operating frequency.

IMPROVING SWITCHING REGULATOR DYNAMIC RESPONSE

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ABSTRACT

Recent introductions of LSI integrated circuits for P.W.M. control have offered considerable simplification to the job of optimizing the design of switching regulators. In addition to greatly reducing the necessary circuitry, the linear transfer function of these devices eases the task of stabilizing the feedback loop and offers several possibilities for improved response. Experimental methods for evaluating the response characteristics of the P.W.M. switching and output stages can be used to confirm simplifying assumptions of linear operation. With this data, several approaches to equalization networks can be compared for performance optimization.

The past few years have seen a major revolution take place in the field of power supply design. Whether forced upon us by the need for energy conservation or finally made practical thru recent advances in semiconductor technology, switching regulators are now the name of the game in voltage control. Novices soon learn, however, that the implementation of a well-designed switching supply involves a little more skill than that required for a linear regulator.

Although the theory of switching regulation has long been known, there is much practical technology - or art — in designing efficient and reliable systems. This is still true even though recently introduced semiconductor devices have made the job at least a little easier. It is the purpose of this discussion to cover a few of the practical aspects of implementing and stabilizing switching regulators using these newer devices.

INTEGRATED P.W.M. CONTROL CIRCUITS

Recognizing a rapidly growing market, many component suppliers have introduced new devices designed specifically for switching regulator applications. These include faster power transistors with improved S.O.A., low E.S.R. electrolytic capacitors, hybrid power devices which include a matched commutating diode, and monolithic IC control devices such as the SG124[1] which contain all of the P.W.M. control circuitry in a single 16-pin, dual-in-line package.

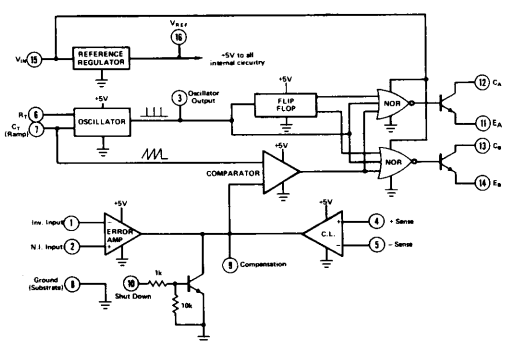


Figure 1. SG1524 Block Diagram

From the block diagram shown in Figure 1, it can be seen that the SG1524 contains the elements necessary to implement either single-ended switching regulators or DC to DC converters of several different configurations. This device includes a voltage reference, error amplifier, constant frequency oscillator, pulse width modulator, pulse steering logic, dual alternating output switches, and current limiting and shutdown circuitry. Since many of the different types of applications for this IC have been discussed earlier[1] it should suffice to review only two of the more common usages as shown in Figures 2 and 3.

The single-sided regulator of Figure 2 is unique because of its simplicity. This circuit combines an SG1524 with an SM625 hybrid to build a 5 volt, 5 amp regulator with all the semi-

conductor devices contained in only two packages. This circuit has an efficiency of over 70% with an input voltage range of 20 to 30 volts, 0.1% line and load regulation, and some added benefits of constant frequency operation and short circuit protection.

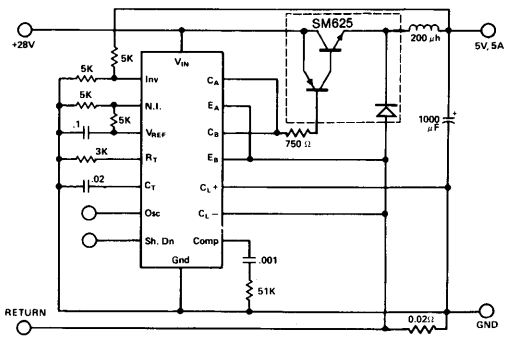


Figure 2. SG1524 Single-Ended Switching Regulator

Figure 3 shows the same 5-volt, 5 amp output requirement met this time with a DC to DC converter. The use of high speed transistors and Shottky rectifiers keep the efficiency more than 80% – significant for a low-voltage output – while maintaining all the other benefits included in the single-ended circuit.

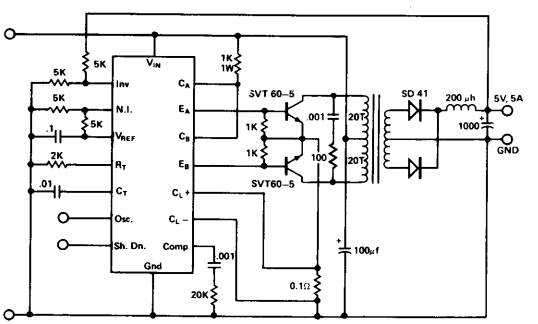


Figure 3. SG1524 Regulating DC-DC Converter

It should be recognized that the above circuits represent very basic applications of an IC control chip. Most practical power supply systems would probably incorporate many other features which may be accomplished by interfacing these IC's with a small amount of external circuitry to add characteristics such as: soft-start, oscillator synchronization, dead-band controls, additional current and/or voltage step-up stages, input-output isolation, remote overvoltage or overload shutdown, and response modifying circuitry. It is this latter subject we wish to explore more fully below.

SWITCHING REGULATOR CONTROL

The basic switching regulator control loop which applies to the most common forms of implementation is illustrated in Figure 4. In analyzing this control loop stability, the obvious immediate problem is the transfer function of the P.W.M. and output stage. A detailed and accurate analysis of the nonlinear characteristics of this stage is an extremely difficult and complex task if one is to account for all the parameters which could possibly be a factor. (2, 3, 4) On the other hand, if this stage could be assumed to have a linear transfer function, analysis becomes a relatively simple application of basic feedback theory.

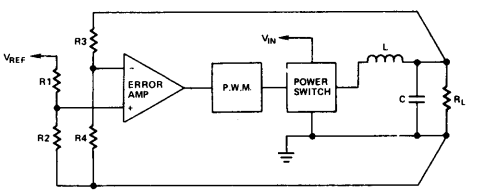


Figure 4. Basic Regulating Control Loop

A significance of the SG1524 is that it uses a design approach which makes a linear assumption accurate enough for most applications. The fact that this device features constant frequency operation, a linear-slope ramp for P.W.M., and fast-response logic and output circuitry all contribute to minimizing the errors associated with a linear assumption. Of course, there are factors external to the IC which could destroy this assumption. Such things as excessive delay in the switching transistors, parasitic ringing or oscillation in the power stages, or nonlinear operation of the magnetics could all cause a resultant nonlinear performance. A first exercise for the designer, then, is to confirm linear operation of the P.W.M. and output stages of his regulator by evaluating his early breadboard models.

OUTPUT STAGE ANALYSIS

The pulse width modulation is accomplished in the SG1524 by comparing the output of the error amplifier with a linear ramp, or saw-tooth signal from the oscillator. Because the comparator has both high gain and high input impedance, and the error amplifier has a high output impedance, this node (pin-9) becomes a very convenient place for inserting a test signal. A voltage source applied as shown in Figure 5 will completely override the error amplifier and essentially open the loop without actually breaking any connections. In addition, the test signal is easily managed because the voltage gain from this point

to the output is relatively low. (A voltage level on pin 9 of from 1 to 4 volts will change the pulse width from zero to maximum which will yield zero to maximum output voltage.)

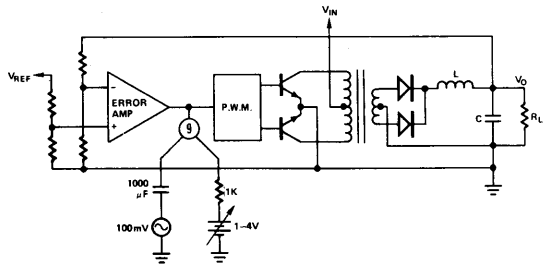


Figure 5. Measuring Output Stage Transfer Function

In experimentally attempting to confirm satisfactory operation of the output stages, the designer hopes to prove that a linear equivalent circuit model is valid for reasonable analysis. One such model as proposed by Middlebrook[5] is shown in Figure 6.. This model describes the overall AC and DC transfer function and input and output impedances in terms of the duty cycle and modulation constant. This model assumes that the effects of operating frequency, switching delays, and parasitic elements are well above the frequencies of interest as defined by the output LC filter.

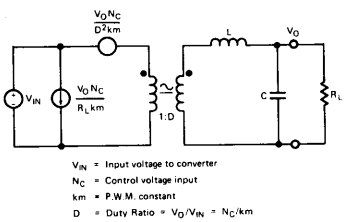


Figure 6. Linear Equivalent Circuit

Values for the inductor and capacitor are normally calculated on the basis of output ripple current and voltage as follows:

For constant frequency operation,

$$L = \frac{V_O(V_{IN} - V_O)}{V_{IN} f(\Delta I_L)}$$

and

$$C = \frac{V_O(V_{IN} - V_O)}{8Lf^2 V_{IN}(\Delta V_O)}$$

where:

V_{IN} = peak input voltage to the inductor
V_O = output voltage across the capacitor
f = switching frequency
ΔI_L = peak-to-peak current variation in the inductor
ΔV_O = peak-to-peak ripple voltage across the capacitor.

Note that the actual ripple voltage at the output of the filter will be ΔV_O, plus ΔI_L times the capacitor E.S.R.

Regardless of the requirements for minimizing the output ripple, an additional requirement on the filter is that its cutoff frequency be well below the switching frequency if our original goal of simple linear analysis is to be met. Specifically, the switching operation introduces a second order lag at one-half the switching frequency and for the output filter to dominate, its cutoff should be at least an order of magnitude below that number, or

$$\frac{1}{2\pi\sqrt{LC}} \leq \frac{f}{20}$$

To verify the performance of the resultant hardware, a Bode plot of the output stage response can be most meaningful. Ideally, a plot as shown in Figure 7 should show a flat response to the filter cutoff and then a linear 12 dB/octave rolloff with a

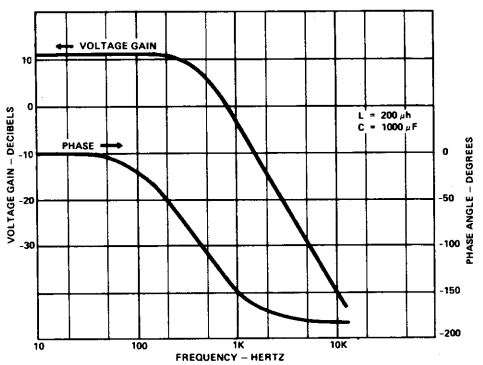


Figure 7. Linear Output Stage Response

180° phase shift. By making these plots with varying input voltage and load current, factors affecting stability such as leakage inductance, capacitor E.S.R., and either saturation or discontinuous operation of the magnetics may be evaluated over the operating conditions of interest. Figure 8 shows typical plots with less than ideal component parameters. With the characteristics of the output stage defined, attention can be turned to the error amplifier to develop an equalizing network which will allow satisfactory closing of the loop.

ERROR AMPLIFIER COMPENSATION

The error amplifier contained within the SG1524 is a transconductance amplifier in that it has a high-impedance, current source output. The gain is a function of the output loading and

can be reduced from a nominal 80 dB by shunt resistance as shown in Figure 9. Note also in Figure 9 that the uncompen-

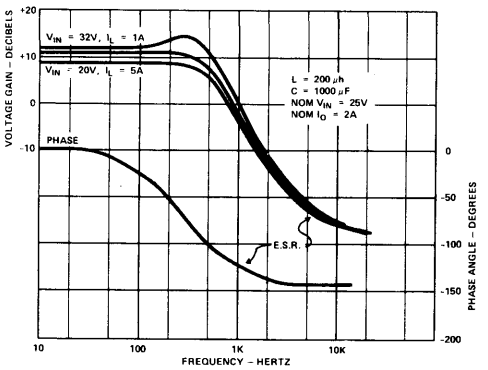


Figure 8. Measured Output Stage Response

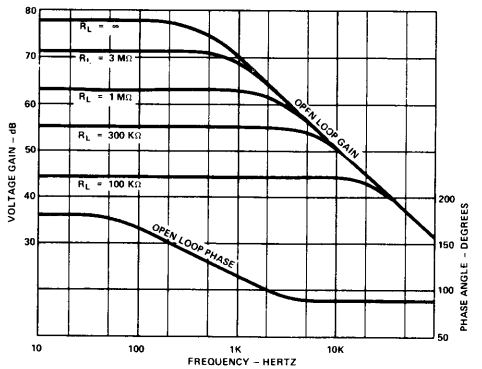


Figure 9. Open-Loop Error Amplifier Response

sated amplifier has a single pole at 300 Hz and 90° of phase shift. The unity gain cross-over frequency is 3 MHz and the large scale slew rate is 0.5 volt per microsecond.

This type of amplifier can be compensated in two ways: The compensation network can go from the output to ground or it can be connected from output back to the inverting input.(6) In the first case, the voltage gain is:

$$A_V = gmZ_C = \frac{8I_CZ_C}{2kT} \approx 0.002Z_C$$

where Z_C is the complex compensation network impedance. If a feedback approach is used, the gain is:

$$A_V = \frac{Z_C}{Z_S}$$

where Z_S is the source impedance driving the input. In cases where relatively low impedances are desired in a feedback network, it may be necessary to buffer the high output impedance of the error amplifier. Figure 10c shows the use of an external emitter follower to provide a low driving impedance for the feedback network.

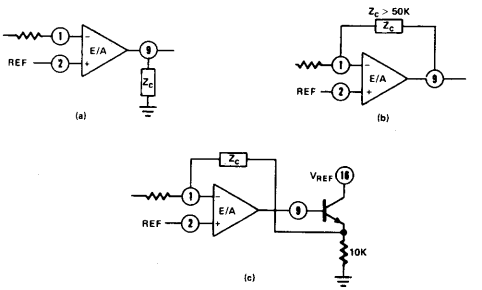


Figure 10. Error Amplifier Compensation Networks

To stabilize the overall regulator feedback loop of Figure 4, it should be apparent that the uncompensated loop contains at least two poles in the output filter and one more in the error amplifier, a situation which typically results in significant gain remaining when the total loop phase equals 360°. One of the simplest compensation schemes is to convert the error amplifier to an integrator by adding a single dominate pole at a frequency so low that the loop gain falls below unity well before the cut-off frequency of the output filter. While this approach yields a stable closed loop gain as shown in Figure 11, the response to

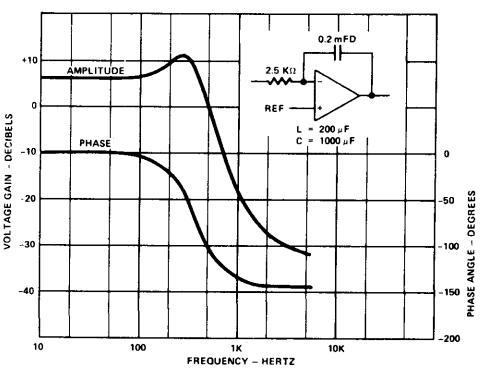
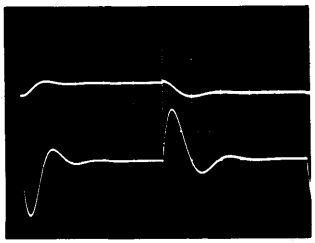


Figure 11. Closed Loop Frequency Response

disturbances is very slow. For example, the waveforms of Figure 12 show the response to a 20%, or one amp, step change in load to the circuit of Figure 3 when compensated with a 0.2 mfd capacitor around the error amplifier.

If instead of slowing down the error amplifier, a zero, or lead network is added to cancel one of the output filter poles, we can keep the total loop phase less than 360° to well beyond the output filter cutoff.



STIMULUS: ONE AMP STEP CHANGE IN I_O
UPPER TRACE: ERROR AMP OUTPUT, 500 mV/DIV
LOWER TRACE: REGULATOR OUTPUT, 200 mV/DIV
TIME BASE: 5 MILLISECONDS/DIV

Figure 12. Integrator Compensation Step Response

Figure 13 shows a circuit for accomplishing this by moving the amplifier pole lower in frequency and adding a zero at the output filter cutoff frequency. Figure 14 shows the effects of this network on the Bode plot of the error amplifier, and Figure 15 indicates the improvement in recovery from the same one-amp load change. Note how the output of the error amplifier overshoots to give a boost to the output.

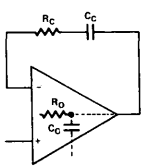


Figure 13. Series RC Phase Compensation

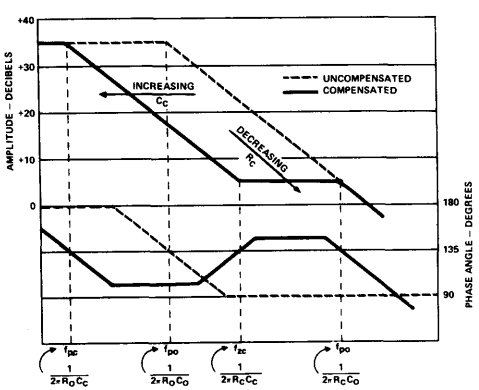
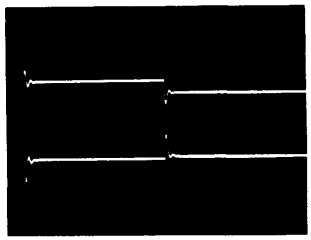


Figure 14. Phase Compensated Bode Plot

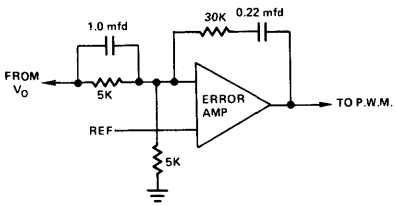
Even faster response can be achieved by providing additional lead networks. For example, another zero may be added by bypassing the sense feedback resistor. As can be seen in Figure 16, this greatly improves loop response but offers the hazard of coupling ripple noise directly into the error amplifier.

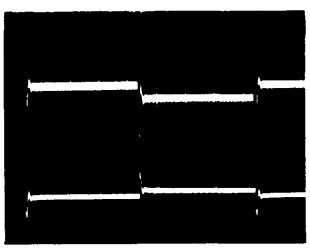


R_C = 30 KΩ, C_C = .022 mfd

STIMULUS: ONE AMP STEP CHANGE IN I_O
UPPER TRACE: ERROR AMP OUTPUT, 500 mV/DIV
LOWER TRACE: REGULATOR OUTPUT, 100 mV/DIV
TIME BASE: 5 MILLISECONDS/DIV

Figure 15. Phase Compensated Step Response





STIMULUS: ONE AMP STEP CHANGE IN I_O
UPPER TRACE: ERROR AMP OUTPUT, 500 mV/DIV
LOWER TRACE: REGULATOR OUTPUT, 50 mV/DIV
TIME BASE: 2 MILLISECONDS/DIV

Figure 16. Double Zero Compensated Step Response

TWO LOOP CONTROL

From the examples presented above, it should be apparent that the integration method of error amplifier compensation provides good stability by making the dominate pole so low in frequency that variations in all other circuit parameters become inconsequential. This technique also provides high accuracy at DC where high gain can be used and is the type of feedback one would want to take directly from the output of a regulator since a user might add additional external capacitance, thereby

changing the output filter characteristics. Another reason for using single-pole compensation is to accommodate the use of a two-stage output filter which can add phase shifts well beyond 180°.

The problem of poor response can then be accommodated by adding a differentiated signal taken from somewhere else in the loop. If the time constants and gain factors are properly selected, the differentiated signal can compensate for the error in the integrated signal taken from the regulated output.

While it may be possible to combine these two signals with passive signal conditioning at the input to the error amplifier, a more straightforward approach is with two separate op amps.(7) shown in Figure 17. Here the error amplifier in the SG1524 has

SUMMARY

Although integrated circuit controllers for switching supplies have removed much of the circuit complexity from this type of regulator, the dynamic analysis of the control loop must still be optimized for each application. This optimization is made easier, however, if a linear approximation of the switching stages can be shown to be valid. The SG1524 controller offers benefits in this regard as it does provide a linear transfer function through its pulse width modulation scheme. Therefore, experimental techniques can be used to simply confirm proper operation of the power switches and output filter.

With a linear output stage, conventional feedback analysis can be used to define the best equalizing network achieving a compromise between stability and fast response. In some cases it may even be desirable to provide separate signal paths for these two parameters but thus, too, can be adapted to the SG1524 controller with a minimum of external circuitry.

Obviously, no recipes for optimum performance have been provided herein. Only a few directions which, it is hoped, will point the way toward the development of specific solutions for specific applications.

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CONVERTING 1524 SWITCHING POWER SUPPLY DESIGNS TO THE SG1524B

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1. INTRODUCTION

Many power control engineers have designed successful switching power supplies around the SG1524 Pulse Width Modulator integrated circuit. This application note explains the differences between this earlier device and the more sophisticated SG1524B. While the functional pinouts are identical for the two devices, there are some distinct operational differences which the user should be aware of when designing new supplies or when updating an existing design. In many cases design changes are minimal (such as adjustment of frequency compensation) or not required at all. At the same time the improvements in control architecture and circuit design of the SG1524B allow the designer to obtain levels of performance in new power supply designs not possible with the older device.

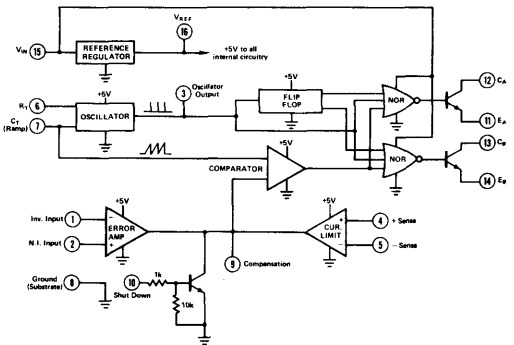

Figure 1 SG1524 BLOCK DIAGRAM

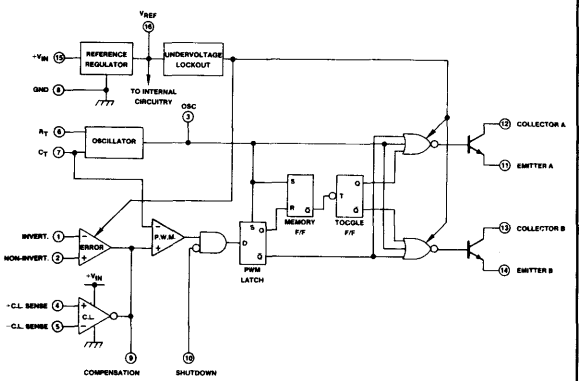

Figure 2 SG 1524B BLOCK DIAGRAM

2. GENERAL COMPARISON

Figures 1 and 2 show respectively the block diagrams of the SG1524 and the SG1524B. Both devices were designed for voltage-mode control, but both can be used to implement current-mode control as well with the addition of an external dual op amp. For further details see the Silicon General Application Note "Current Mode Control with the SG1524B."

The main functional difference between the two circuits is in the action of the shutdown pin. In the SG1524, a voltage at Pin 10 greater than +0.7 volts will turn on an internal transistor which pulls the error amplifier output to ground. In the 1524B, a voltage greater than +1.2 volts at Pin 10 activates a logic gate which inhibits the pulse output of the PWM comparator. The error amplifier output voltage is not affected directly.

Other improvements include the addition of an undervoltage lockout function and fault suppression logic. These provide protection against inadequate supply voltage to the control IC and insure constant-frequency alternating output pulses to the power devices.

INDIVIDUAL SECTION DIFFERENCES

3.1 VOLTAGE REFERENCE

The voltage reference is a low-drift bandgap design which provides a precision +5.0 volt reference for the control loop. Initial accuracy is ±1% for the SG1524B/2524B, and ±2% for the SG3524B. This is a factor of four improvement over the original reference. Line regulation is typically better by a factor of 3:3mV instead of 10mV. Load regulation is better by a factor of 4:5mV rather than 20mV. The temperature coefficient is also lower and more uniform from device to device. All these features translate directly into tighter tolerances on the switcher output voltage.

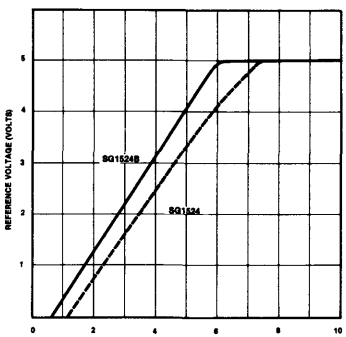

Figure 3.
REFERENCE VOLTAGE VS SUPPLY VOLTAGE

At 25°C the differential drop across the regulator is only 1.2 volts, as opposed to 2.7 volts for the 1524. Figure 3 shows the relationship between V_{IN} and V_{REF} for both devices. As a result the SG1524B is fully functional with a 6.2 volt supply. Under worse case conditions of I_{LOAD} = 20 mA and T_A = −55°C, all devices are guaranteed to function at V_{IN} = 7 volts.

3.2 UNDERVOLTAGE LOCKOUT

This circuit has two sections: a controlled current source which forces the error amp low and the output transistors off, and a bandgap comparator which overrides the lockout source. The current source is fully active when V_{IN} is +1.2 volts. Since the error amp and output driver cannot function until V_{IN} is approximately 3 volts, it is impossible for spurious output pulses to occur when the supply voltage is too low for normal operation.

The bandgap comparator monitors the reference voltage. It enables the SG1524B when the reference rises to +4.3 volts. This arrangement allows operation from a +5 volt ±5% supply by connecting V_{IN} and V_{REF} together.

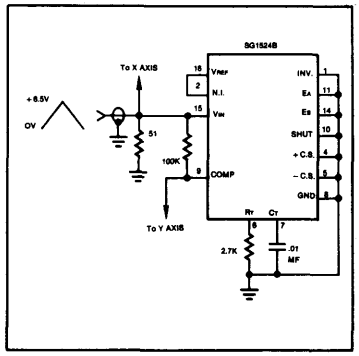

Figure 4
UNDERVOLTAGE LOCKOUT TEST CIRCUIT

The action of the undervoltage lockout can be observed with the test circuit of Figure 4. A 100K pull-up resistor is connected from Compensation to V_{IN}. V_{IN} is swept from 0 to +6.5 volts with a 5Hz triangle waveform from a function generator. An oscilloscope in XY Mode displaying V_{IN} horizontally and Compensation vertically will generate the display shown in Figure 5.

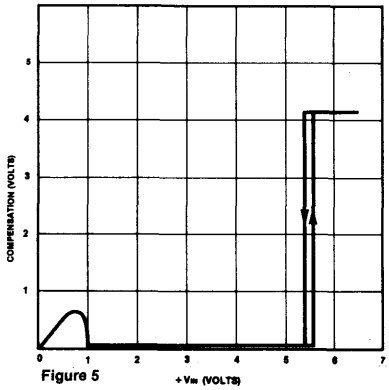

Figure 5
UNDERVOLTAGE LOCKOUT AT THE ERROR AMP

As V_{IN} slowly sweeps from 0 to 1 volt, the lockout current source becomes active and pulls the error amp to ground, guaranteeing 0% duty cycle from the controller. From 1 volt to approximately 5.5 volts the controller is inhibited while the internal circuitry stabilizes. At 5.5 volts the bandgap comparator overrides the lockout current, releasing the output of the error amp. The reverse portion of the voltage sweep is identical, except that approximately 200 mV of hysteresis can be observed at the comparator trip point.

3.3 OSCILLATOR

The oscillator of the SG1524B is programmed for frequency with an external Rt and Ct in the same manner as the SG1524. Both initial accuracy and temperature coefficient have been improved with the "B" version.

There are two methods to synchronize multiple units together.

A. Program a master unit with Rt and Ct for the desired frequency. Connect the Ct terminal (Pin 7) of the master to the Ct terminal of the slave. Connect the OSC terminal (Pin 3) of the master to the OSC terminal of the slave. Leave the slave Rt terminal (Pin 6) open or tied to the reference. This is the recommended approach if the PWM controllers are close together (on the same printed circuit board and within six inches of each other.)

B. Program a master unit for the desired frequency. Select Rt and Ct for the slave units such that they free-run at a frequency 10% slower than the master. Connect all the Oscillator terminals together. This method is recommended if the PWM controllers are not close together, since it avoids routing a high impedance line (Ct) around a noisy environment.

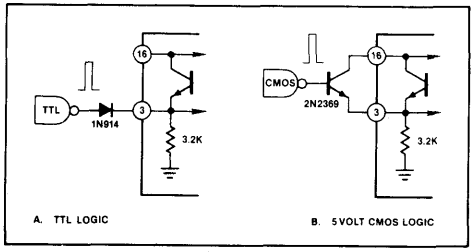

Figure 6
OSCILLATOR SYNC TO AN EXTERNAL CLOCK

To synchronize one or more devices to an external clock frequency, one of the connections shown in Figure 6 should be used. The device(s) to be synchronized should free-run 10% slower than the clock. Pulse width of the external clock should be at least 200nsec, but not longer than the desired deadtime.

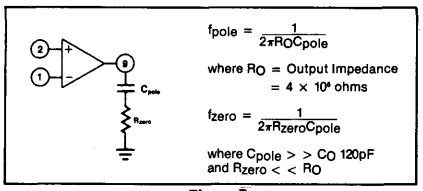

Figure 7
FREQUENCY COMPENSATION OF THE ERROR AMPLIFIER

3.4 ERROR AMPLIFIER

The error amplifier of the SG1524B is, like its predecessor, a transconductance design with an output impedance of approximately 4 megaohms. This allows use of exteral clamp circuitry to obtain soft-start and duty cycle limit, as on the original 1524. Since all the voltage gain takes place at the output pin, open-loop gain/frequency characteristics are easily controlled by shunt reactance from Pin 9 to ground (Figure 7). Also, this type of amplifier has a very predictable 1/T variation of open-loop gain with absolute temperature as shown in Figure 8.

The input common mode range is +2.3 to +5.2 volts, so that existing designs at +2.5 volts will function with no modifications. For new designs the +5 volt reference may be applied directly to the non-inverting input, eliminating the necessity for two divider resistors.

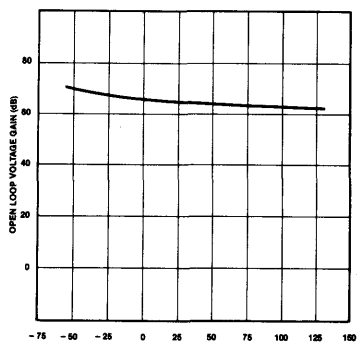

Figure 8
OPEN LOOP GAIN VS. TEMPERATURE

Since the lower common mode limit is +2.3 volts for the 1524B and +1.8 volts for the 1524, neither amplifier should ever be used in the non-inverting unity-gain configuration shown in Figure 9. The error voltage must swing down to +0.5 volts to guarantee 0% duty cycle from the pulse width modulator, and this violates the common mode range specification.

In general, any frequency compensation for the voltage control loop which works with the SG1524 can also be used with the SG1524B with no modification.

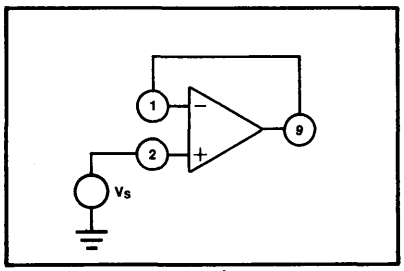

Figure 9
NON-INVERTING UNITY-GAIN CONNECTION
(NOT RECOMMENDED)

3.5 CURRENT LIMIT AMPLIFIER

The current limit amplifier of the SG1524B is one of the most significant areas of change from an applications viewpoint. Like the original circuit, there is a fixed 200mV threshold designed into Pins 4 and 5 to permit direct sensing across a current sampling resistor. Differences in the "B" circuit affect the input bias current, allowable common mode range, and stability in current-limit.

3.5.1 INPUT BIAS CURRENT

In the SG1524, there is a constant 130 μA flowing out of Pin 4, while the current out of Pin 5 is variable from 0 to 100 μA depending on the differential input voltage. Because of this characteristic the current limit sense terminals must be driven from source impedances less than 20 ohms to avoid modulating the current limit threshold. The "B" device features bias currents which are identical at each pin, are independent of current sense voltage, and are a factor of 10 lower. This allows predictable foldback current limiting without wasteful low-resistance divider networks.

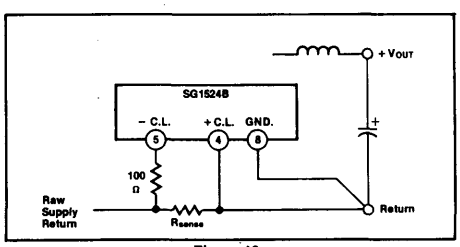

Figure 10
CURRENT SENSING IN THE GROUND LNE

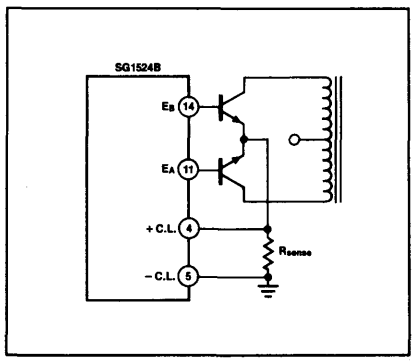

Figure 11
SENSING PRIMARY CURRENT WITH AN EMITTER RESISTOR

3.5.2 COMMON MODE RANGE

The guaranteed common mode range of the current sense inputs is 0 volts to V_{IN} – 2.5 volts. Current sensing in a supply ground line is possible, but the configuration of Fig. 10 should be used to avoid damaging the IC. The 100 ohm resistor is required because of delays through the controller and storage time in any bipolar power device. The SG1524B will reduce the pulsewidth as Pin 5 is driven 200 mV below ground, but in practice it is overdriven due to the aforementioned delays. If Pin 5 is driven below –0.3v at Ta = +125°C the substrate diode will conduct. The 100 ohm resistor will limit the peak substrate current to a safe value without shifting the C.L. threshold.

Current sensing may also be accomplished with a common emitter or source resistor to ground as shown in Figure 11; or it may be placed in the supply output line, as indicated in Figure 12. At –55°C the value of V_{IN} must be at least 2.5 volts greater than the switcher output voltage.

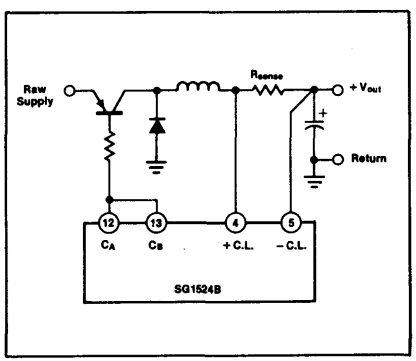

Figure 12
CURRENT SENSING IN THE OUTPUT LINE

3.5.3 FREQUENCY COMPENSATION

The original SG1524 current limit amplifer had a typical open loop gain of 44dB, and was internally compensated to produce a single-pole roll-off above 300 Hz. The SG1524B exhibits 75dB of gain and has no internal compensation. The circuit may be used as a moderate speed comparator, or it may be used as an analog gain block to override the error amplifer.

Because of the higher gain and bandwidth, designers may find that the control loop will oscillate when the supply goes into current limiting. The cure is to add frequency compensation externally to the current limit circuit or to rework the existing voltage loop compensation. See the Silicon General Application Note "A New, Versatile P.W.M. Control Circuit for Switching Power Supplies."

3.6 SHUTDOWN

The shutdown circuit of the "B" is illustrated in Figure 13. It has the following differences compared to the 1524:

A. Logic threshold is +1.2 volts instead of +0.7 volts for compatibility with TTL logic and improved noise immunity.

B. Input current is very low (usually under 100 nA) even at +5 volts input. The pin may be driven directly from TTL logic (all families) or TTL-output comparators.

C. Response time is very fast, between 35 and 100 nanoseconds depending on output transistor loading.

The shutdown pin should never be left floating. If not used, the pin should be grounded. If the shutdown function is used, the pin should be driven from a low impedance source to prevent noise pickup. The internal logic is very fast, and will respond readily to spurious pickup from the normally noisy environment of a switcher.

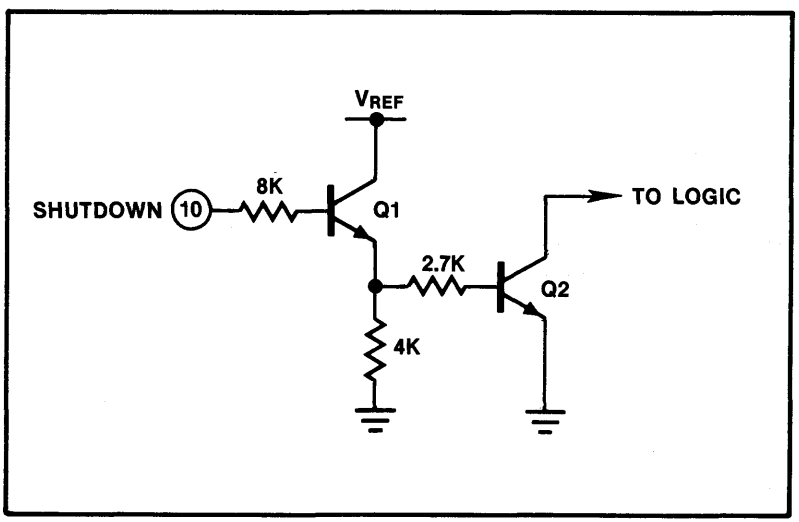

FIGURE 13. SHUTDOWN CIRCUITRY OF THE SG1524B

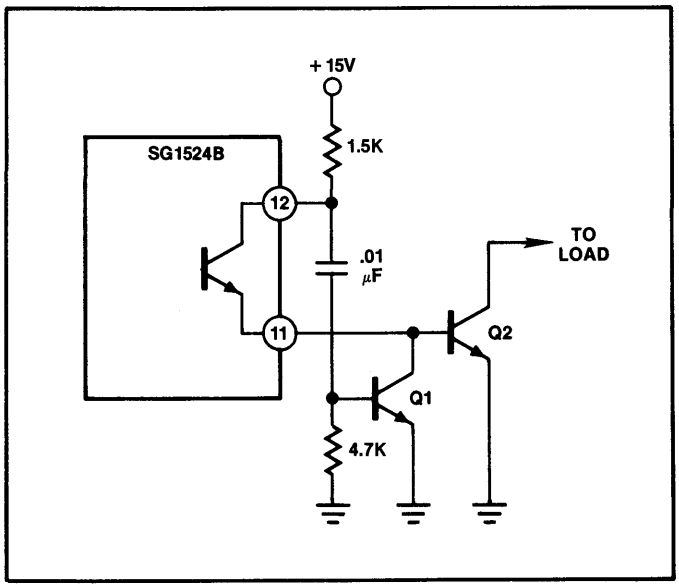

FIGURE 14. DRIVING POWER BI-POLAR TRANSISTORS WITH THE SG1524B

3.7 OUTPUT TRANSISTORS

The output devices have been redesigned to provide 100 mA continuous and typically 200 mA peak, with BV_{CEX} ratings of 60 volts. Saturation voltage is guaranteed both at 10 and 100 mA to ease the interface with external power devices.

3.7.1 BIPOLAR DRIVE

For driving bipolar power devices the circuit in Figure 14 is recommended. The output transistor is used as a phase-splitter to generate the necessary base drive. Figure 15 illustrates forward and reverse base current, and collector current of a PMD 20K 120 volt, 14 amp Darlington using this driver configuration.

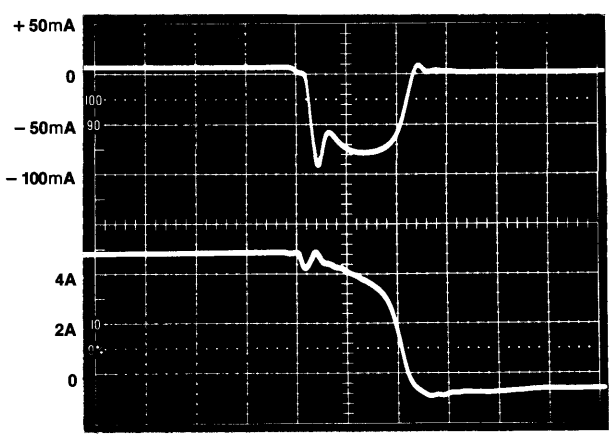

FIGURE 15. BIPOLAR TURN-OFF WAVEFORMS. UPPER TRACE: DARLINGTON BASE CURRENT @ 200 NSEC/DIV. LOWER TRACE: COLLECTOR CURRENT @ 200 NSEC/DIV.

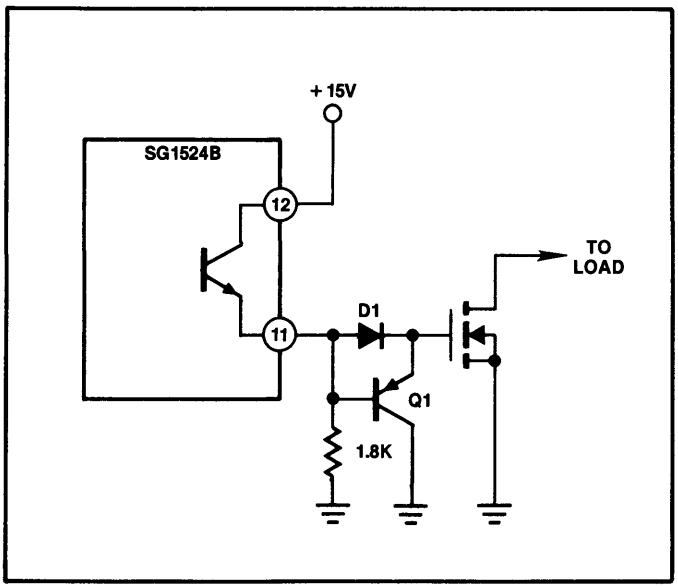

FIGURE 16. DRIVING POWER MOSFETS WITH THE SG1524B

3.7.2 POWER MOSFET DRIVE

Highly capacitive loads such as presented by the gates of power MOSFETs can be readily driven with the circuit in Figure 16. At turn-on, 200mA of charging current is conducted by D1. During turn-off D1 becomes back-biased by the pulldown resistor. Q1 turns on and provides 500mA of discharge current. Figure 17 shows the turn-off gate voltage and drain current of an IRF130 100 volt, 14 amp power MOSFET driven directly with this circuit.

4. CONCLUSION

A designer who is familiar with the SG1524 will find it relatively easy to adapt his designs to use the SG1524B. The immediate benefits are higher levels of power supply performance, worthwhile reductions in total component count, a greater degree of protection for the power devices, and lower overall costs.

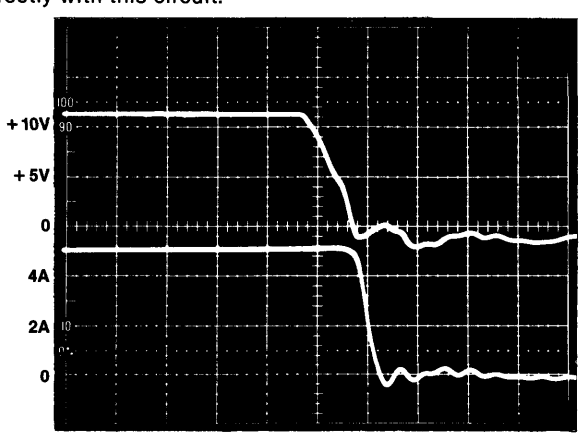

FIGURE 17. MOSFET TURN-OFF WAVEFORMS. UPPER TRACE: GATE VOLTAGE @ 100 NSEC/DIV. LOWER TRACE: DRAIN CURRENT @ 100 NSEC/DIV.

A NEW, VERSATILE P.W.M. CONTROL CIRCUIT FOR SWITCHING POWER SUPPLIES

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ABSTRACT

A new control circuit for pulse-width-modulated switchmode power supplies is described. This device offers improved electrical and functional performance over earlier designs, while retaining the familiar pin-out of the industry-standard SG1524. Innovative circuit design techniques and optimized control architecture result in improved reference accuracy, protection against inadequate supply voltage, elimination of harmful output switching transients, improved current limiting, and higher voltage and current capabilities from the output transistors. A 50 kHz power supply utilizing the new controller is described, and performance characteristics are analyzed.

1. INTRODUCTION

Since the introduction in 1976 of the first monolithic control chip for switchmode power supplies, and its subsequent wide acceptance as the basic building block for high-efficiency regulator designs, the semiconductor industry has found itself in a bit of quandry when attempting to define an improved device.

On the one hand, the initial device, being rather simple and straightforward, had a number of deficiencies when its capabilities were compared with the total requirements of most switchers. As a result, new, more complex controllers were introduced with improved reference accuracy, protection against inadequate or fluctuating supply voltage, improved current limit circuitry, fault suppression logic, and a host of other features.

On the other hand, the new controllers, while enthusiastically accepted first by aerospace designers for sophisticated high-performance supplies and later by major computer and instrumentation manufacturers, lacked the familiar pin-out of the earlier device. As a result it has not been possible until recently to easily upgrade the performance of an existing design by simply plugging in a more intelligent pin-for-pin substitute.

The circuit to be described has been under development at Silicon General for more than two years, and represents an attempt to fit as much function as possible within the constraints of the original device pin-out. Designated the SG1524B, the device block diagram is shown in Figure 1.

2. FUNCTIONAL DESCRIPTION

A precision +5.00V reference trimmed to an initial ±1% accuracy provides a voltage standard for the regulation loop. It also powers most of the internal control circuitry, eliminating adverse effects due to fluctuating supply voltage. A high gain error amplifier compares the reference voltage with the switchmode supply output voltage, and generates a PWM control voltage at Pin 9. This voltage is compared against a periodic linear ramp generated by the oscillator circuit. Oscillator frequency is determined by an external timing resistor and capacitor, R_T and C_T. The comparator output is a fixed-frequency, variable pulsewidth logic signal which passes through routing logic to one of the two high current output transistors if the Shutdown pin is LOW.

A current limit amplifier within the IC overrides the PWM control voltage when the voltage differential at the Current Limit Sense inputs reaches 200 mV. This built-in threshold permits direct sensing across an external current sampling resistor. On-chip undervoltage lockout circuitry protects the power semiconductors in the switchmode supply by guaranteeing orderly start-ups and shutdowns as supply voltage is switched on and off.

Each control section of this new PWM controller has been either redesigned for improved performance, or is a completely new function compared to the original SG1524 design. A detailed description of each section follows to highlight the major improvements.

2.1 Bandgap Reference Regulator

The precision reference uses the predictable base-emitter voltage of NPN transistors to generate the +5V reference voltage, rather than a zener diode[1, 2]. The advantages of this design approach are: lower noise due to elimination of the shot noise associated with an avalanche device, low turn-on drift, better long term stability, and operation from a lower supply voltage. The primary disadvantages are that the bandgap requires more components, and thermal matching of key devices is necessary for realizing low thermal drift.

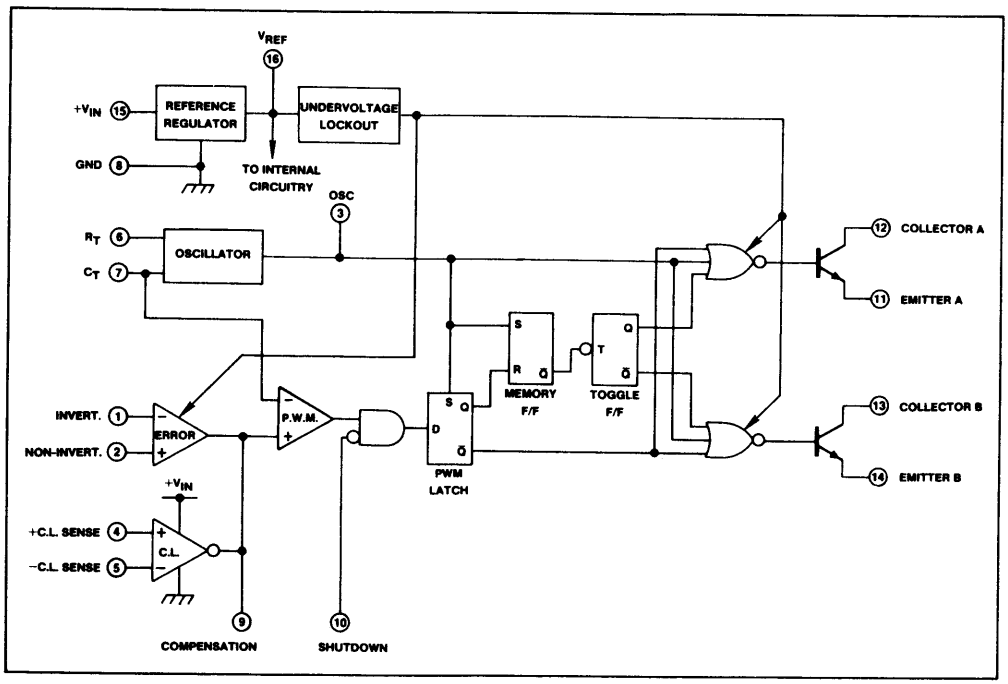

FIGURE 1. BLOCK DIAGRAM OF THE SG1524B PULSE WIDTH MODULATOR.

	ZENER REFERENCE	BANDGAP REFERENCE
Minimum Supply Voltage	8V	7V
Output Noise Voltage	75 μVrms	25 μVrms
Long Term Stability	20 mV/ 1000 hrs	5 mV/ 1000 hrs
Turn-on Drift	5-35 mV	2 mV

TABLE 1. COMPARISON OF ZENER AND BANDGAP REFERENCE TYPICAL PARAMETERS

The ability of the PWM controller to be fully functional with a 7V supply enhances its usefulness in portable instrumentation applications, where six-cell Ni-Cad battery packs are frequently found, and a 1.16V cell voltage is defined as end-of-life before recharge.

2.2 Undervoltage Lockout

The undervoltage lockout circuitry prevents spurious turn-on commands to the external power transistors when the supply voltage to the integrated circuit is too low for proper operation. When the reference voltage is less than +4.5V, the output transistors are forced to an OFF or nonconducting state. Additionally, the output of the error amplifier is clamped to ground. When the supply voltage rises to +7V, the output drivers are enabled and the amplifier output is released. Since compensation capacitance is usually present at Pin 9, this provides a measure of built-in soft start.

During the power-up period of the controller, when the undervoltage lockout is active, bias current is freely supplied to all the internal control circuitry. This insures that all control functions have stabilized in the proper state when the turn-on voltage is reached, and it prevents the possibility of start-up glitches.

The lockout circuitry monitors the reference voltage rather than $+V_{IN}$ to allow the SG1524B to be used with +5V supplies in the same manner as the original SG1524. If the $+V_{IN}$ pin is connected to the V_{REF} pin and +5V ±10% is applied, the control chip will function normally. When the undervoltage sense circuitry monitors the $+V_{IN}$ pin, this type of operation is not possible due to the 2-3V drop across the internal regulator.

To provide jitter-free turn-on and turn-off points, the lockout circuitry has been designed with approximately 500mV of hysteresis. This provides rejection of 120Hz ripple on the $+V_{IN}$ line, and reduces capacitive filtering requirements on the controller supply voltage.

2.3 Error Amplifier

The error amplifier of the SG1524B was designed with three principle goals in mind: a common-mode range extending from +2.5V to $+V_{REF}$, excellent supply voltage and common-mode noise rejection characteristics, and a minimum voltage gain of 60 dB at +125°C. Like its predecessor, it is a transconductance amplifier with a high-impedance output to permit external soft-start circuitry.

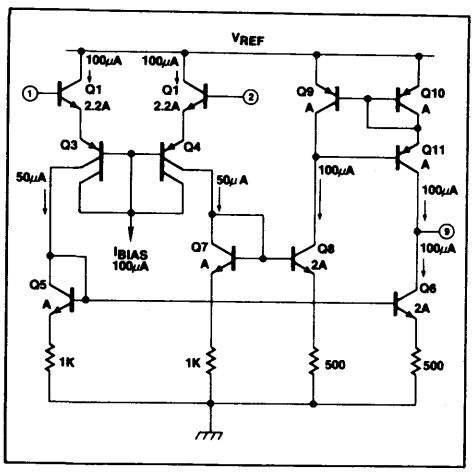

FIGURE 2. SCHEMATIC DIAGRAM OF THE SG1524B ERROR AMPLIFIER.

Input transistors Q1 and Q2 are connected as emitter-followers with their collectors tied to the +5V reference supply. This configuration provides the required common-mode range, even with $+V_{IN}$ connected to V_{REF} for operation from a +5V supply. It also provides current gain to reduce input bias current, and produces a low impedance source to drive level shifters Q3 and Q4. These PNP devices operate at a forced beta of 1.0, and are connected common-base to maximize frequency response. Input stage operating current is set up by the 100 μA bias supply to the common base. Frequency response is further improved by the low impedance collector loads Q5 and Q7. These two devices are diode-connected and form the input sides of two precision 2-to-1 current mirrors, which provide additional current gain. The output current of Q6 provides the pull-down or sink current for the amplifier output. The collector current of Q8 is referenced to the +5V supply rail by the Wilson current mirror consisting of Q9, Q10, and Q11. The collector current of Q11 provides the pull-up or source current for the amplifier output.

It can be seen from the symmetry of the circuit that a differential input voltage is converted to an output current, with a maximum of ±200μA available. The open-loop voltage gain can be shown to be [3]

$$A_V = gm\ R_L = I_S \frac{q}{kT} R_L = .001\ R_L \text{ at } +25°C.$$

Since R_L is the parallel combination of the output impedances of Q6 and Q11, and is typically 4MΩ, an open-loop voltage gain of 72dB is obtained.

The circuit design of the output stage insures that the maximum positive output swing never exceeds +4.3V. This is important when considering loop recovery from momentary overloads which drive the PWM to maximum duty cycle. The peak value of the sawtooth oscillator waveform is +3.4V, and the error amplifier must slew from positive full scale to less than this voltage to reduce the duty cycle from maximum. Some error amplifier designs clamp the output voltage with a 6.3V zener diode, nearly tripling the recovery time from overload.

Since all the voltage gain of the error amplifier takes place at the output pin, the amplifier can be easily frequency compensated at this node with shunt reactance to ground. The uncompensated amplifier exhibits an open loop pole at 350 Hz and a typical unity-gain bandwidth of 2 MHz.

2.4 Current Limit

The current limit amplifier has been redesigned to eliminate the two most common complaints about the original SG1524: limited input voltage range and slow response time. In the original design the ±1V common-mode range restricted current sensing to the supply return line only. In many systems, ground returns cannot be separated, making the current limit function unusable. Also, the internal frequency compensation provided freedom from oscillation at the expense of response time.

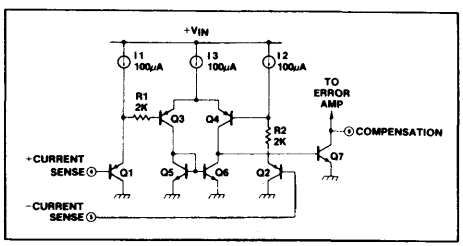

FIGURE 3. HIGH-GAIN CURRENT LIMIT AMPLIFIER.

In the new design, input transistors Q1 and Q2 allow common mode voltages as low as −0.3V over the operating temperature range, allowing sensing in the ground line for configurations that

require it. The upper limit is restrained only by the value of $+V_{IN}$, to which the level-shifter current sources I1 and I2 are referenced.
The voltage drop across R2 creates a 200 mV offset voltage at the amplifier input which provides the current sense threshold. The positive 0.2%/° C temperature coefficient of R2 is balanced by a negative tempco for I2, effectively cancelling effects of temperature on the current sense threshold.

Since both the allowable common-mode and differential voltages are much greater with this design, higher current foldback ratios can be achieved compared to the maximum of 3 or 4 possible with the earlier part. Also, the bias currents are a factor of 10 lower, resulting in more consistent limiting thresholds from unit-to-unit when foldback is employed.
Because there is no internal compensation capacitor, stability in the current limit mode will depend on external components. Due to the controller architecture, in which the output of the current limit amplifier overrides the error amplifier, these external frequency compensation networks may either be shared with the error amplifier or optimized for the current limit amplifier. The two choices are shown in the figures. In either case, the designer now has the freedom to optimize bandwidth for his particular switcher configuration.

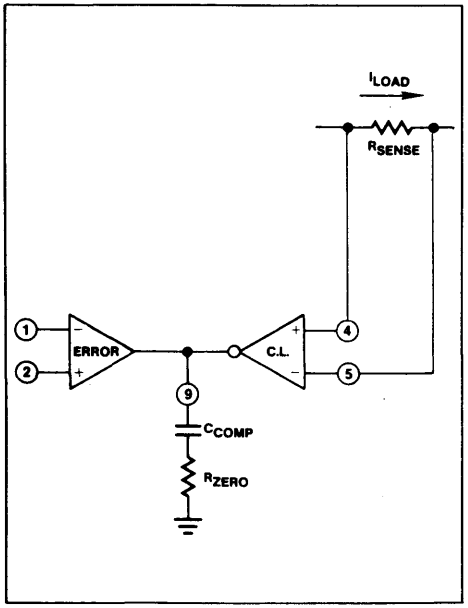

FIGURE 4. CURRENT LIMIT COMPENSATION IN COMMON WITH ERROR AMP.

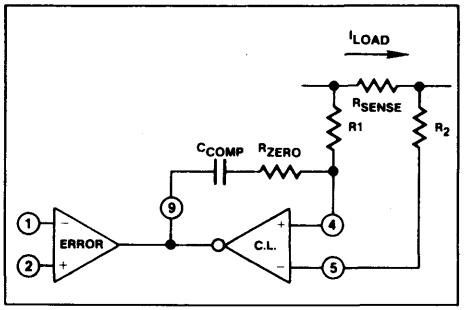

FIGURE 5. CURRENT LIMIT WITH OPTIMIZED FREQUENCY COMPENSATION.

2.5 Oscillator

The sawtooth oscillator circuitry of the SG1524B incorporates the same design improvements recently applied to the SG1524. These result in greatly improved external drive and synchronization capability, together with reduced sawtooth undershoot at high frequencies.
In the original SG1524 design, an external synchronization pulse applied to the OSC pin did not generate a self-sustaining discharge cycle. The extent of the discharge of C_T depended on both the amplitude and duration of the external pulse. As a result, it was possible to generate erratic sawtooth waveforms with partial discharge cycles and pulse-to-pulse modulation of waveform endpoints. The frequent result was audible noise from subharmonics, transformer saturation, and destruction of the power transistors.

In the improved design, an external sync pulse which meets the minimum threshold requirements triggers a positive feedback circuit. This circuit drives the oscillator to end-of-discharge even if the external pulse is very narrow. Due to the feedback, there exists no in-between or quasi-synchronized state; the oscillator switches smoothly between free-running and synchronized modes as the external pulse amplitude is varied through the trigger threshold.
The positive feedback also effectively bootstraps the comparator gain, providing enhanced voltage swing and output current at Pin 3 to drive peripheral circuits. The improved oscillator design, together with a fast, DC-coupled toggle flip-flop, permits operation beyond 500 kHz. However, the limitations associated with single-transistor outputs put a practical upper limit of 400 kHz on the device.

2.6 Full Double-Pulse Suppression Logic

The PWM logic in the SG1524B insures that the output pulses always alternate from side to side, regardless of the action of the shutdown circuit. This is very important in push-pull switcher

configurations, where two pulses in succession on one side of the power transformer primary will cause core saturation and instantaneous failure of the power transistor.

The logic consists of two sections: a PWM latch circuit and a memory flip-flop. The latch allows only one pulse through per oscillator cycle. Once a PWM pulse is terminated, whether due to the normal PWM process or due to SHUTDOWN going high, the pulse cannot start again until the beginning of the next oscillator cycle. Pulse-by-pulse current limiting is easily accomplished now because of the latch feature and the completely digital (and therefore very fast) shutdown circuitry.

The memory flip-flop insures that output pulses always alternate from the output transistors. This is accomplished by generating a clock to the toggle flip-flop only if a PWM pulse was generated during the previous cycle. In the original 1524, the toggle flip-flop changes state with every oscillator pulse, irrespective of what the outputs are doing.

Figures 6 and 7 illustrate the difference in performance between two PWM control ICs, one with only a data latch and the other with the full double-pulse suppression logic described above. The triple-trace photos in each example show an alternating output pulse sequence interrupted by a SHUTDOWN command, followed a short time later by resumption of outputs from Emitters A and B. Oscillator frequency is 40 kHz for each device, so 20 kHz is obtained at the output transistors.

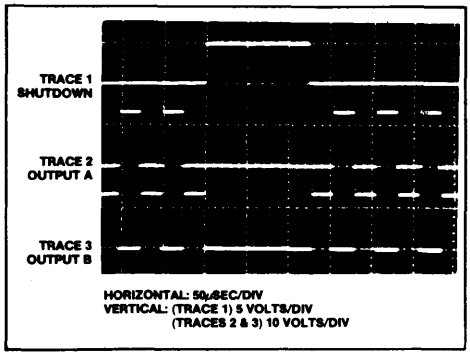

FIGURE 6. OUTPUT SEQUENCE WITHOUT DOUBLE PULSE SUPPRESSION.

In the first case, the PWM pulses are alternating can BABAB when a SHUTDOWN signal inhibits the outputs for five oscillator cycles. When output resumes, the output sequence begins BABAB . . . .Two pulses have occurred in succession from Emitter B.

With the second control IC, the PWM pulses are again alternating BABAB when a SHUTDOWN signal is received, again inhibiting output for five oscillator cycles. When SHUTDOWN is removed, output resumes, but with an ABABA . . . sequence. The potential double-pulse from Emitter B has been eliminated by the internal pulse-steering logic.

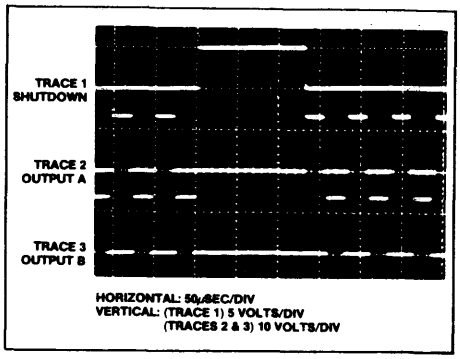

FIGURE 7. OUTPUT SEQUENCE WITH DOUBLE PULSE SUPPRESSION.

This side-by-side pulse-routing problem exists for any PWM control IC with push-pull architecture and a truly digital shutdown function. In the original 1524 design, recovery from shutdown was fairly slow since the error amplifier output was pulled to ground for turn-off. Turn-on was limited by the 100μA output current of the error amp, the internal compensation capacitor in the current limit circuitry, and any external frequency compensation components. This created an inherent soft-start characteristic. With digital shutdown, the error amp voltage is not immediately affected; the first pulse out after shutdown can be the same width as before shutdown, making pulse-routing logic an absolute necessity to guarantee the safety of the power switches.

2.7 Output Transistors

In response to requests for greater output drive capability, the output transistors were redesigned for both higher breakdown voltage and more current.

In a PWM controller with a single-transistor output structure, the load driven is frequently one end of a center-tapped transformer primary winding. Since the maximum collector voltage is 2 x V_{CC}, the absolute maximum rating of 40V for the earlier device restricted the supply voltage to 20V. Consideration given to the effects of transformer leakage reactance would reduce this voltage still further. The SG1524B output transistors carry BV_{CEX} ratings of 60V, high enough for use on a standard +28V supply bus.

Output device geometry was scaled up to allow reliable operation at continuous collector

currents of 100 mA. This represents a factor of two improvement over the earlier device, which was characterized only at 50mA. As a further aid to the designer, the data sheet for the new device specifies maximum saturation voltage at two continuous current levels: 10mA and 100mA. The maximum peak current capability of the output transistors is 200mA for 1μS.

The anti-saturation clamp circuitry around the output transistors found in the earlier PWM controller has been retained in the SG1524B to enhance switching speed. Each output transistor is also guarded against excessive current by protective circuitry which limits the maximum continuous current to 150mA at +25°C.

3. DESIGN EXAMPLE

The functional usefulness of a new device is best demonstrated by study of an actual switcher design. The circuit described illustrates full control of a power supply with a single integrated circuit, resulting in reduction of overall cost and an increase in supply reliability through reduction of component count.

The circuit illustrated in Figure 8 is a push-pull, +28V to +5V converter operating at 50 kHz. The power supply is unique in that the only active component is the SG1524B regulating pulse width modulator; the only other semiconductors required are diodes.

The DC-coupled push-pull configuration was chosen because it is most sensitive to PWM controller anomalies which cause side-to-side imbalance. These include start-up problems such as output from only one driver until the toggle flip-flop begins to be correctly clocked by the oscillator. During normal operation, side-to-side imbalance of volt-second product due to unequal propagation delays in the IC can cause the onset of core saturation. Finally, as outlined earlier, when the digital Shutdown control is activated, double-pulse sequencing can drive the excursion of the transformer core flux past the saturation knee of the BH loop.

Capacitor C3 acts as a high-frequency bypass for the IC supply line, while C6 is the high current reservoir for the power stage. The oscillator is set for 100 kHz with C4 and R5. When divided by two by the action of the internal toggle flip-flop, this becomes 50 kHz at the power transformer. The +5V reference is filtered against high frequency noise pick-up by R2 and C1, and applied to the non-inverting input of the error amp. The inverting input is connected to the power supply output terminals to form the negative feedback loop required for regulation. R3 minimizes the effects of input offset bias current by equalizing the source impedance seen by each error amp input terminal. Closed loop stability is provided by frequency compensation components R4 and C2, using the common technique of cancelling one of the two poles of the LC output filter with a open-loop zero in the error amplifier.[4]

In the power section of the supply, the two output transistors are used to directly drive a center-tapped transformer. A snubber network consisting of C5 and R6 modifies the inductive

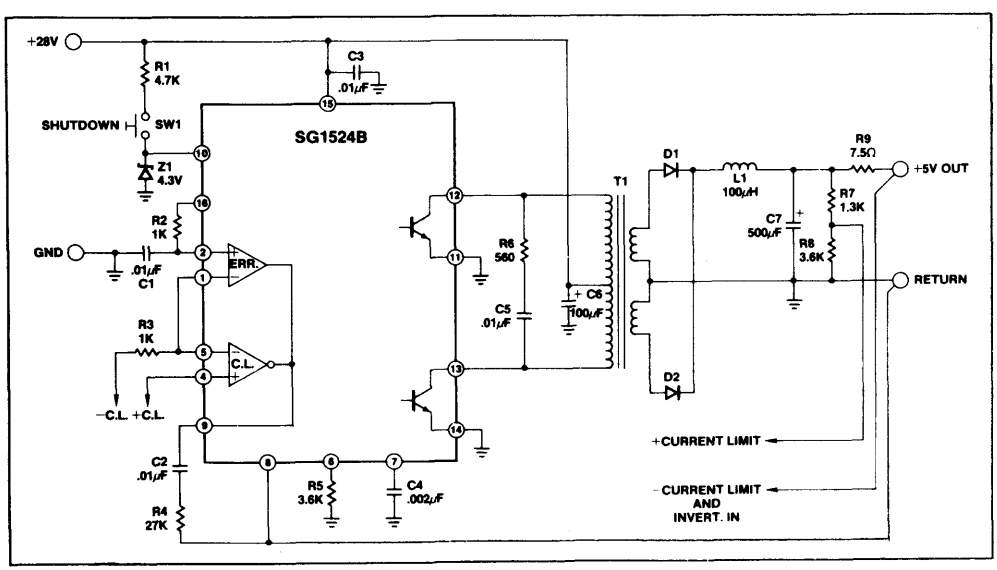

FIGURE 8. A SINGLE IC 50 kHz PUSH-PULL CONVERTER.

load line seen by each transistor. The transformer itself is wound on a small ferrite core; turns ratio is 3:1. Rectifier diodes D1 and D2 are Schottky junction devices to maximize efficiency at +5V output. Filtering is provided by L1, wound on a permalloy powder toroid, and C7.

The improved common mode range of the current limit amp is used to good advantage here; current sensing is done directly in the output line. A foldback ratio of 7.5 to 1 is obtained with the given values of R7, R8, and R9. The divider formed by R7 and R8 applies a back-bias of 1.3 volts, or 6.5 times current limit threshold, when the supply output is at +5.0V. Peak output current before onset of current limiting is 200 mA, and short-circuit current is only 25 mA.

Rapid turn-off of the control circuit is accomplished by closing SW1. R1 and Z1 limit the maximum voltage applied to the Shutdown terminal to less than +5V.

While capable of only limited output power due to thermal limitations of the 16 pin Cerdip package, the supply amply illustrates the controller ability to perform all the major control functions required both during start-up, normal regulation, and overload.

4. CONCLUSION

In the past it was often necessary to incorporate additional components around the 1524 pulse-width modulator to enhance its capabilities, and to guard against various functional anomalies. Economically this was feasible due to the relative cost of the control device compared to the cost of the peripheral components.

With the occurrence of the usual price decline characteristic of most integrated circuits, the economic balance has shifted. Many users now pay more for the necessary support circuitry than for the 1524 itself.

The availability of the SG1524B now gives the designer another option. In many instances costly additional support components can be eliminated and a functionally superior device may be plugged directly into an existing design, with the benefit of simplicity, greater reliability, and reduced overall cost.

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(3) J.E. Solomon, W.R. Davis, P.L. Lee, "A Self-Compensated Monolithic Amplifier with Low Input Current and High Slew Rate", IEEE ISSCC Digest, pp. 14-15, February 1969.

(4) Stan Dendinger, "Digital Current Limiting Techniques for Switching Power Supplies", POWERCONVERSION '80/Munich, pp. 3A. 4-1 through 3A. 4-10.

POWER SUPPLY CIRCUITS HEAD FOR SIMPLICITY BY INTEGRATION

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SUMMARY

The benefits obtained from switching power supplies have become universally recognized by power systems engineers in the past several years. However there has been a simultaneous realization that, too frequently, gains in efficiency and reductions in weight have been accompanied by an escalating component count and a decrease in reliability and predictability of performance. To effectively solve these problems, integrated circuit manufacturers have recently designed new products specifically for switchers. These devices offer the proven advantages of monolithic technology: compactness, accuracy, reproducibility, higher performance through reduction of parasitics, and the economies of mass production.

This paper reviews the circuit simplifications made possible by these specialized devices, as typified by the first practical switching regulator control chip, the SG1524 Pulse Width Modulator, and later by other circuits such as the ZN1066, the TL494A, and the MC3420. A second potential area of power supply simplification is the interface between the control circuit and the high power switching transistors. Two specialized driver circuits, the SG1627 and SG1629, are described which provide high-level turn-on and turn-off signals for efficient switching. Finally some second and third generation pulse width modulator designs will be discussed. These later devices, designated the SG1525/27 series and the SG1526, offer even higher levels of control function integration compared to earlier designs. The SG1526 in particular integrates a number of protective control features which substantially increase the reliability of the power semiconductors in "real world" switching power supplies.

HISTORICAL PERSPECTIVE

A basic pulse width modulated switching power supply requires only four control elements: a precision reference voltage, a ramp oscillator, an error amplifier, and a differential voltage comparator. Each of these elements has been available in integrated circuit form for years, with the well-established benefits of reduced physical size, greater reliability, and increased performance. In light of this background, the development of a single monolithic circuit for switching power supply control appears to be a logical progression.

One of the first devices available to power supply desigers was the SG1524 Pulse Width Modulator from Silicon General. This circuit, shown in Figure 1, contained all of the basic control elements required for a switching regulator. In addition to providing the four basic control elements, the device allowed for push-pull configurations by inclusion of a toggle flip-flop and dual alternately-gated output transistors. Finally, provision was made for some abnormal power supply operating conditions. An analog current limit circuit and a digital shutdown control were included to provide protection against short circuits and other load faults.

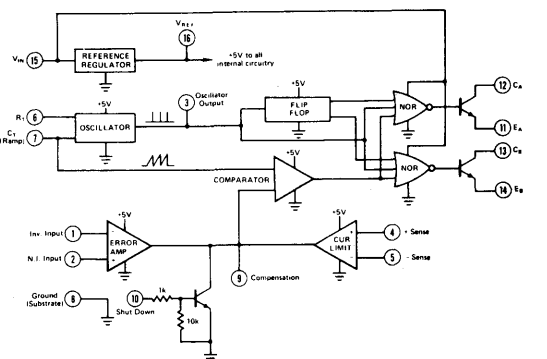


FIGURE 1. SG1524 PULSE WIDTH MODULATOR BLOCK DIAGRAM

Despite this level of complexity, the device was easy to understand and was quite flexible. As a result, since its introduction in 1976, the SG1524 has been very widely accepted within the power supply industry, finding its way into a majority of new designs, including exotic applications in communications satellites and the space shuttle program.

POWER DRIVER INTEGRATION

As experience was gained in applying the SG1524, it became apparent that there was a gap between the output power capabilities of the control integrated circuit and the drive levels required by the power semiconductors. Two areas were identified within most supply configurations where specialized driver functions could be successfully implemented with monolithic technology.

An Integrated Source/Sink Driver

The first design is a dual 500mA totem-pole driver with externally programmable current sourcing. Both inverting and non-inverting logic inputs are available, and may be driven by either an open-collector control circuit or (with a diode) by TTL logic. Connections to the high current output transistors are brought out separately, allowing maximum flexibility when interfacing with standard bipolar transistors, the new VMOS power FETs, and transformers.

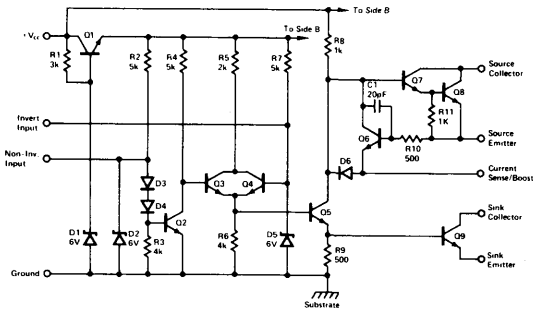


FIGURE 2. PARTIAL SCHEMATIC DIAGRAM SG1627 DRIVER CIRCUIT

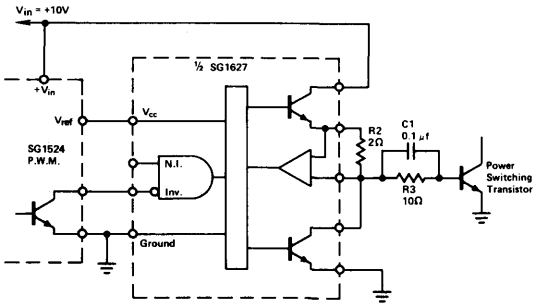


FIGURE 3. DRIVING BIPOLAR JUNCTION TRANSISTORS WITH A TOTEM-POLE SWITCH DRIVER

Power Bipolar Drive is accomplished with the connection shown in Figure 3. R2 controls the magnitude of forward base drive, and is selected to develop a voltage drop of one V_{BE} when the output Darlington pair is sourcing 350mA. At the same time R3 develops a 3.5 volt differential, which is stored by C1. During turn-off, sink transistor Q9 saturates, pulling the output terminal to ground. The emitter-base junction becomes reverse biased from a low impedance source, allowing stored base charge to be rapidly extracted.

Power FET Drive is possible with a minimum of external components. The source/sink capability of the SG1627, together with its fast edge speeds, makes it an ideal driver for power MOSFET devices. Although MOSFETs have negligible DC gate current, input capacitances of 800—1000pF exist in the higher current units. Since this capacitance must be charged and discharged by 10 or 12 volts in 10 to 20 nanoseconds, high peak currents are required. At switching frequencies of 200 kHz, considerable dynamic power dissipation is required of the drive cicuit to obtain the high speed switching benefits of these devices.

In Figure 4, peak currents in the output stage are limited by R_2, while R_1 helps minimize power in the SG1627. With some power FETs, a 100 ohm resistor in series with the gate lead may also be necessary to eliminate device oscillations.

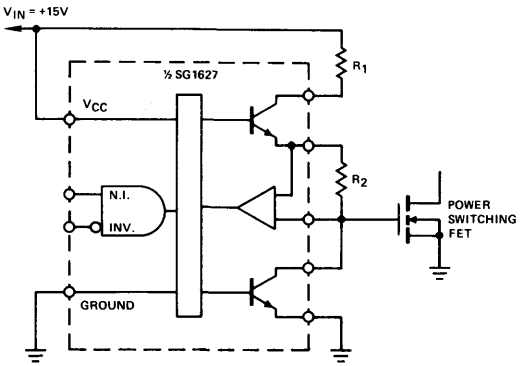


FIGURE 4. A SOURCE/SINK DRIVER PROVIDES THE PEAK CURRENTS REQUIRED BY POWER FET'S AT HIGH SWITCHING FREQUENCIES

Transformer Drive is the third interface area where an integrated power driver can eliminate components. Most bi-phase transformer drive circuits using grounded emitter transistors require additional components to reset the magnetic flux to zero every half cycle. This is necessary to insure that no net DC excitation is applied to the transformer primary over many cycles of operation, thereby avoiding core saturation. These additional components may include extra transformer windings, clamp diodes, and anti-phase driven clamp transistors. A much less complex circuit can be achieved with the SG1627, as shown in Figure 5.

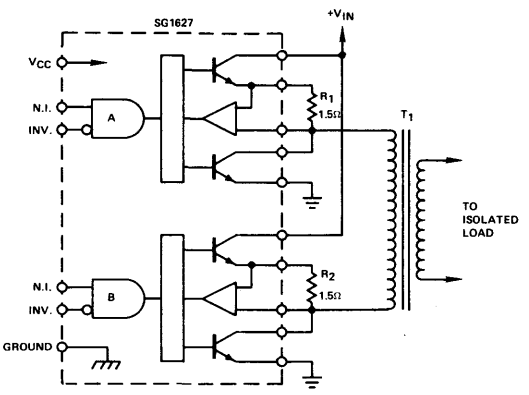


FIGURE 5. THE LOW IMPEDANCE OF THE SG1627 IN BOTH ON AND OFF STATES ALLOWS DIRECT TRANSFORMER DRIVE WITH A MINIMUM OF EXTERNAL COMPONENTS

In this circuit the transformer primary is voltage-driven by the source/sink output structure of the SG1627. Core reset to zero occurs automatically during deadtime, when both ends of the primary winding are switched to ground. Resistors R_1 and R_2 serve as over-current protection for the driver in case of control malfunction or onset of core saturation due to load faults on the secondary. No center tap is required, resulting in elimination of winding balance problems.

An Integrated Floating Switch Driver

The second interface considered was that between the secondary winding of a drive transformer and the base-emitter junction of an NPN power transistor. This configuration is frequently found in off-line converters, where a half or full bridge design is chosen because of the high input supply voltage. In this case the design problem consisted of providing controlled forward base drive to the power device during the positive polarity of the secondary voltage, and a fast negative peak current for rapid switch-off during the negative portion of the cycle. No power other than that provided by the transformer secondary should be required, so that the power device can be floated above ground by several hundred volts.

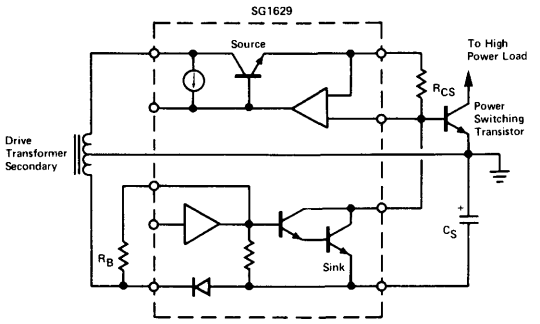


FIGURE 6. SG1629 FLOATING SWITCH DRIVER BLOCK DIAGRAM

The circuit shown is a modification of a discrete design developed by Pete Wood while at TRW Semiconductors[1]. During a positive cycle, base current flows from the drive transformer secondary winding through a source transistor which can be programmed for current limiting. A center tap on the secondary completes the circuit for returning base drive current. At the same time, external storage capacitor C_S is charged to a negative value through the high current rectifier diode in the switch driver. When the secondary voltage is driven to zero, the rectifier diode becomes reverse biased. The resulting positive drive turns on the Darlington sink transistors, which reverse-biases the base-emitter junction of the power device through the storage capacitor. A large negative current spike results, minimizing the turn-off time and power loss in the switching transistor.

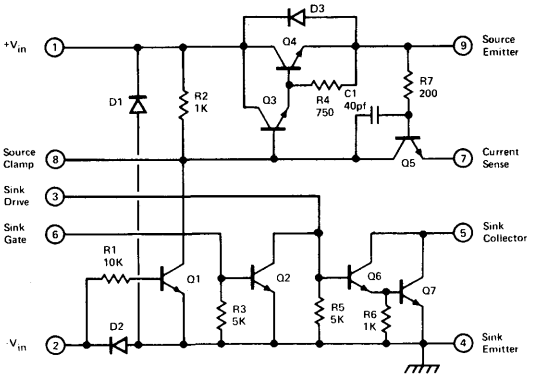


FIGURE 7. SG1629 FLOATING SWITCH DRIVER SCHEMATIC DIAGRAM

As the detailed schematic of the SG1629 indicates, in addition to the high current Darlington source and sink transistors the circuit also contains several gating options for the sink or turn-off section of the driver. Source transistors Q3—Q4 and sink transistors Q6—Q7 are designed fo 2 amp collector currents. Base drive to the source is provided by R_2, while Q5 provides current limiting. On the sink side of the circuit, base drive to Q6—Q7 is normally provided by a resistor connected to Pin 3. Q1 senses the polarity of the input voltage and gates the source transistor off between each drive current pulse. This action allows the external storage capacitor to be charged even at very low duty cycles, since the discharge current during the "off" portion of the drive cycle becomes negligible. The sink gate input is used when the risetime of base turn-on current is important, and transformer inductance is a significant limiting factor. Methods for using this feature are found in the SG1629 application note[2].

Power Driver Summary

Two integrated power driver circuits designed specifically for use in switch-mode power supplies have been reviewed. These devices provide the necessary power gain between a complex low-power control circuit and high voltage, high current switching semiconductors, while offering greater performance in a reduced volume compared to discrete component designs. Monolithic technology will provide even higher levels of voltage and current handling capability in the future as soon as semiconductor packaging technolgy solves the problem of providing large pin-outs in a high power dissipation package.

A SECOND GENERATION PULSE WIDTH MODULATOR CONTROL CIRCUIT

As switch-mode power supplies gained in popularity, a demand was made by power supply design engineers for an integrated circuit that offered all of the functions of a control device and the interface capabilities of a power driver. The SG1525A series of pulse width modulators represents a combination control IC and power driver. The control section is based upon the time-proven architecture of the SG1524, while the output stage of this device combines many of the elements of the previously

discussed 1627 power driver. At the same time, improvements were made within the architecture of the control chip to include even more functions than were originally available on the 1524.

The internal reference regulator on the chip is trimmed to an accuracy of ± 1%, compared to the original ± 4%. Secondly, the chip now contains on-chip shutdown and soft start circuitry. The only external components required are an external timing capacitor. A third area of improvement is in the common mode range of the error amplifier. By designing the error amplifier so the common mode range now includes the 5.1V of the reference, a reference divider network is no longer necessary, thus eliminating two external resistors. The oscillator circuitry has been redesigned to make dead time control easier and multiple device synchronization easier. Finally, the output stage has been redesigned so that, instead of a single transistor which is periodically turned on for pulse width modulation, an output source/sink driver or totem-pole type design is used. Since this particular driver has the characteristic of low impedance in both the on and off states, it becomes much easier now to interface the control circuits with external power transistors including standard bipolar junction devices, the new power FETs, and also drive transformers.

This new family of regulating pulse width modulators is designated the SG1525A/1527A series of devices, and the device block diagram is illustrated in Figure 8.

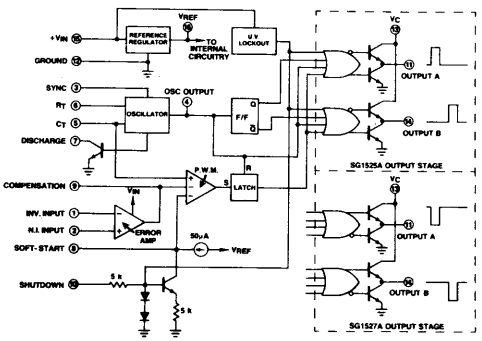


FIGURE 8. BLOCK DIAGRAM OF A "SECOND GENERATION" PULSE WIDTH MODULATOR FAMILY: THE SG1525A/1527A SERIES

The trimmed reference regulator, which has an output voltage of 5.1V, not only acts as the reference terminal for the error amplifier control loop, but it acts as a power source for all the internal circuitry, with the exception of the error amplifier and the output drivers. The oscillator determines the basic operating frequency of the pulse width modulator circuit. An external R_T and C_T are the components that are fixed to set this frequency. Additionally, dead time is controlled by the insertion of a small amount of resistance between the discharge terminal (Pin 7) and the C_T terminal (Pin 5) on the oscillator. The oscillator circuit has two outputs: the ramp waveform, which is applied to the positive input of the pulse width modulation comparator, and a periodic positive-going pulse at the oscillator output pin which acts as the toggle signal for the flip-flop. It is also used as the deadtime control pulse for the output gating logic.

The totem-pole output drivers are designed to easily interface with either single ended or push-pull types of switching power supply configurations. There are two output polarities available with this series of pulse width modulators. In the 1525A series, the output gating is designed with NOR logic, which results in a positive-going output pulse during active time. The 1527A series uses OR logic, so that the active state is a low or ground state. This particular polarity of output is useful in certain types of proportional base drive circuits in which feedback from the power transformer is used to provide base current, thereby compensating for variations in transistor beta.

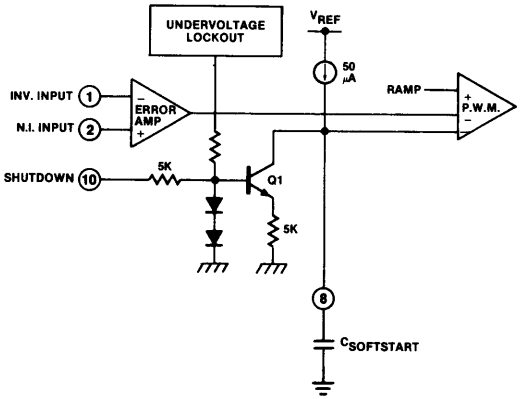


FIGURE 9. SG1525A/1527A SOFTSTART CIRCUIT

Soft Start Circuit

The equivalent of the SG1525A/1527A soft start circuitry is shown in Figure 9. An external capacitor $C_{SOFT\ START}$ provides the timing element for the soft start cycle. This capacitor is charged via a 50 micoramp current source internal to the chip. The P.W.M. comparator has two inverting inputs, and the more negative of the two voltages determines the duty cycle. During undervoltage conditions on the V_{IN} line, current is forced through the two diodes in Q1's base circuit. A voltage of approximately 1 V_{BE} appears across Q1's emitter resistor, resulting in a collector current of approximately 100 µA. Since the charging current available is only 50 µA, the soft start capacitor is held in a discharged state. Because the volatge at pin 8 is 0, the PWM comparator ignores the signal from the error amplifier, and zero duty cycle is obtained. When the controller supply rises to 8 volts the discharge current is turned off, and the voltage on pin 8 rises linearly, resulting in gradually increasing duty cycle. Eventually the capacitor charges up very close to the reference voltage and the duty cycle is controlled by the error amplifier. If the voltage on the shutdown pin is raised above ± 1.5 volts the capacitor is slowly discharged at the same rate it is normally charged.

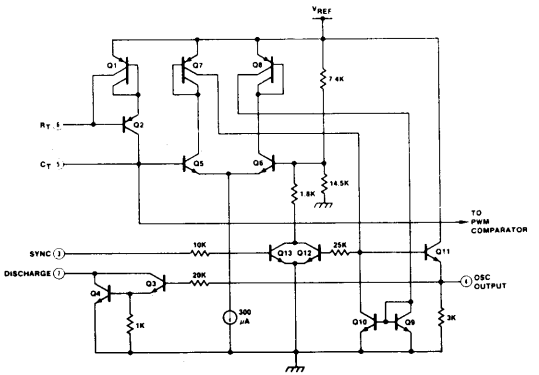


FIGURE 10. SG1525A/1527A OSCILLATOR SCHEMATIC DIAGRAM

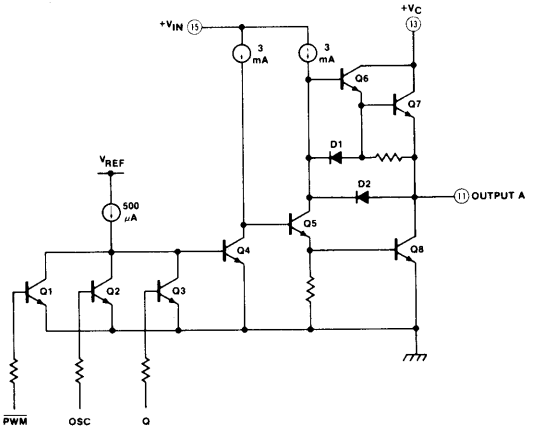


FIGURE 11. SG1525A PULSE WIDTH MODULATOR POWER OUTPUT STAGE

Oscillator Description

The circuit for generation of the timing ramp waveform is shown in Figure 10. The timing capacitor C_T receives a constant charge current from the compound current mirror formed by Q1 and Q2. The R_T terminal voltage is two V_{BE} less than the reference voltage, so that a resistor tied from Pin 6 to ground sets up the charging current for C_T. Transistors Q5 through Q10 form a voltage comparator which constantly compares the voltage at C_T to either a +3.3V or +1V reference, depending on the state of the comparator. The timing capacitor C_T is discharged via the Darlington formed by Q3 and Q4.

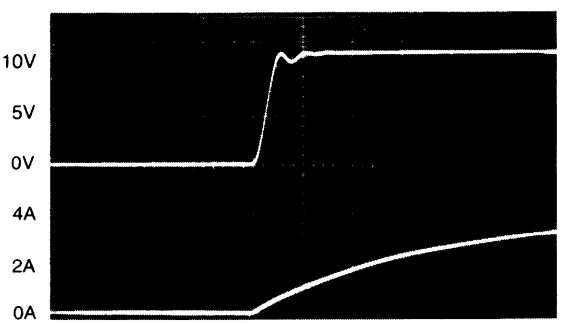
When the voltage on C_T is less than +3.3V, the discharge network does not conduct and C_T receives a constant charge via the current mirror, resulting in a linearly increasing voltage. When the +3.3V trigger level is reached, the comparator changes state and turns on the discharge network. This rapidly removes charge from C_T so that the voltage falls towards +1V, at which time the comparator changes state again and another cycle begins. The discharge time of C_T is used to generate the blanking pulse at the oscillator output pin. The dead time or pulse width at the oscillator output pin may be increased from it's minimum value of approximately 400 to 500 nanoseconds by a resistor between the discharge pin and Pin 5, which lengthens the discharge time of C_T during the second half of the oscillator cycle.

A positive pulse at the sync pin will initiate a discharge cycle in the oscillator. This pin then forms a convenient connection for synchronizing the IC to a frequency supplied by an external system clock.

Output Driver

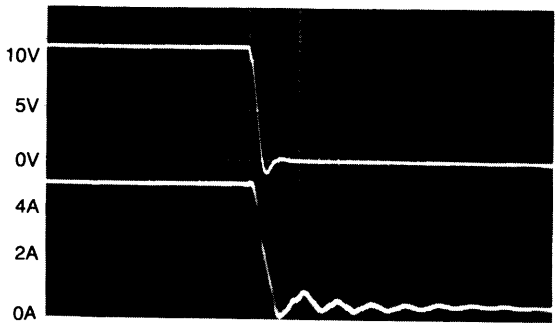
A simplified schematic of the output gating and the power output stage of the 1525A is shown in Figure 11. Transistors Q1, Q2 and Q3, together with a 500 microamp current source, form a logical NOR gate where the pulse width modulation signal from the pulse width modulation comparator, the dead time pulse from the oscillator, and one side of the toggle flip-flop are combined. Q4 is an amplifier with active load which inverts the output signal from the NOR gate. Q5, in turn, acts as the phase-splitter transistor for the push-pull output. When Q5 is on, its emitter current drives the base of Q8, holding the output low. At the same time, the collector of Q5 is also low, thereby back-biasing Q6 and Q7, the output pull-up devices. When Q5 turns off, its collector voltage rises, turning on the output Darlington. At the same time, Q8 turns off and the output terminal is pulled up towards the V_C supply. Diode D1 acts to protect the base emitter junction of the upper Darlington against reverse breakdown. D2 acts to provide extra base drive current to Q8 during turn off. If a capacitive load is present on the output terminal, D2 will turn on and the extra collector current of Q5 will then be routed to Q8 so that Q8 in turn will be turned on harder, thus discharging the output capacitance and enabling the output to fall rapidly to zero.

The source and sink transistors Q7 and Q8 in this driver are designed to provide more than 100mA of current handling capability. In most cases, the full current capability will not be used in a steady state condition to drive an external load but rather the peak current capability can be used to provide rapid charging of external capacitance loads, thereby providing very fast rise and fall times at the output of the driver.



Time Base: 200 NSEC/Division
Upper Trace: Power FET Gate Drive
Lower Trace: Power FET Drain Current

I FIGURE 12. SG1525A/POWER FET TURN-ON WAVE FORMS



Time Base: 200 NSEC/Division
Upper Trace: Power FET Gate Drive
Lower Trace: Power FET Drain Current

FIGURE 13. SG1525A/POWER FET TURN-OFF WAVE FORMS

Figures 12 and 13 illustrate the speed capabilities of the output drivers when driving power MOSFETs, in this case a pair of Siliconix VN64GA devices. The upper traces show the driver output voltage swing for a collector supply of +12 Volts. The lower waveforms are the 0-5 Amp drain currents of the FETs. Switching times of 100 nanoseconds were acheived by driving the gates directly from the totem pole outputs, and by limiting peak currents to 200mA with a 62 ohm resistor at the $+V_C$ terminal. Faster times can be obtained with the higher current SG1627 Power Driver.

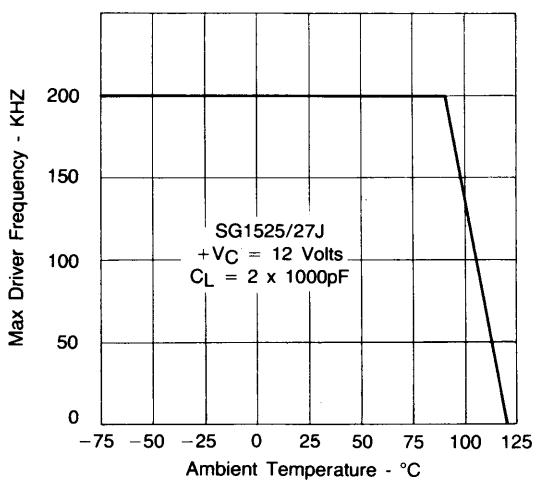


FIGURE 14. SG1525A/1527A POWER FET DRIVE CAPABILITY

The ultimate frequency capabilities of the output drivers as a function of ambient temperature for a given VMOS load is shown in Figure 14. For this graph, a $+V_C$ supply of 12 Volts was assumed. An effective power FET input capacitance of 1000 pF on each driver was also assumed. A thermocouple attached to the ceramic dual-in-line package allowed junction temperature to be calculated based on a worst case Θ_{JC} of 60°C/W and a Θ_{JA} of 100°C/W maximum.

For ambient temperatures below 90°C the maximum frequency allowable is determined by the maximum possible oscillator frequency of 400 kHz. Above 90°C operating frequency and dynamic power dissipation must be reduced to keep the junction temperature from exceeding +150°C. Different supply voltages, capacitive loads, and heat sinking will result in other temperature limits.

It will be noticed in comparing the block diagram of the SG1525A/1527A family to that of the SG1524 that there is no provision made directly for current limiting on the 1525A/1527A. The reason for this is that this chip is designed to interface with a new output supervisory circuit, the AF1543. This device has an extra comparator with adjustable offset which can be used for providing the current limit function in conjunction with the 1525A/1527A. Additionally, this particular chip has the capability for providing under and overvoltage protection for the remainder of the power supply.

A THIRD GENERATION
SWITCHING POWER SUPPLY CONTROL CIRCUIT

- Supply operation to 40 volts
- Reference trimmed to ± 1%
- Sawtooth oscillator with deadband control
- PWM comparator with hysteresis
- Undervoltage lockout
- Programmable soft start
- Wide error amp common mode range
- Wide current limit common mode range
- Two modes of digital current limiting
- Double pulse suppression logic
- Single pulse metering logic
- Symmetry correction capability
- TTL/CMOS compatible logic
- Dual 100mA source/sink output drivers

TABLE 1. DESIRABLE FEATURES OF A HIGH-PERFORMANCE PULSE WIDTH MODULATOR

An ideal circuit for switching power supplies should include not only the elements necessary for normal pulse modulation operation, but also the full range of abnormal operations. Ideally, the circuit should contain as many protective features as possible for the power semiconductors. If a table of parameters were constructed for such device, it would look much like that shown in Table 1. Analysis of the features in the table would show that most of the new features are control related and are therefore ideally suited for inclusion in an integrated circuit, where a great deal of complexity can be easily compressed into a very small area. Just such a device has been designed by Silicon General, and the block diagram of that device is shown in Figure 15.

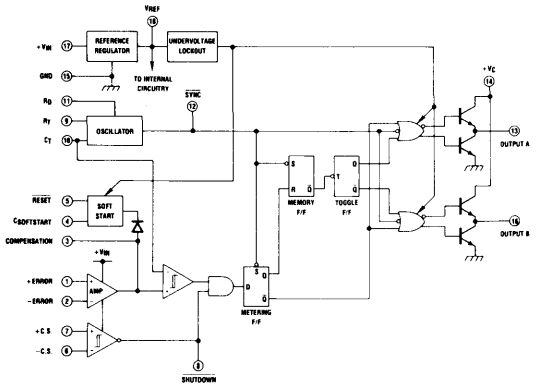


FIGURE 15. SG1526 HIGH PERFORMANCE PULSE WIDTH MODULATOR BLOCK DIAGRAM

As can be seen, the four basic elements of the pulse modulator are present: a reference regulator, error amplifier, sawtooth oscillator, and a pulse width modulation comparator. Of particular interest are some new features in the block diagram: an undervoltage lockout, soft start circuitry, digital current limit comparator and digital signal processing logic between the pulse width modulation comparator and the output power drivers.

The operation of the circuit is as follows: An on-chip regulator trimmed to 1% is both reference voltage for the error amplifier, and also the stabilized power source for all the internal circuitry, with the exception of the error amplifier, the current limit comparator, and the output drivers.

The sawtooth oscillator is programmed for a specific frequency and deadband by values of R_T, C_T and R_D. The resulting ramp waveform is applied to one side of the pulse width modulation comparator, which has been designed with a very small amount of hysteresis to prevent oscillations at the comparison point. The other terminal of the PWM comparator is connected to the output of an error amplifier which has been designed with a common mode range that includes both ground and the 5V reference.

Also associated with the amplifier is on-chip soft start circuitry. This soft start circuitry is controlled not only by an external RESET terminal, but also by the undervoltage lockout circuitry. If the reference voltage should be less than the 5V required for normal linear operation of the control circuitry, the RESET terminal on the soft start is held low by the undervoltage lockout, thus preventing the soft start capacitor from charging. At the same time, the power output drivers of the device are inhibited, thus making it impossible for spurious output pulses to occur during undervoltage conditions.

The digital output of the pulse width modulation comparator is ANDed with the output of the current limit comparator. This provides very fast response to overcurrent conditions. The current limit comparator has a fixed input offset of 100mV plus a slight hysteresis of 20mV to eliminate indecision at the threshold point. The PWM signal from the AND gate is followed by three levels of pulse processing logic. It first passes through a metering flip-flop whose function is to allow only one output pulse per oscillator cycle, thus eliminating oscillations and permitting pulse-by-pulse current limiting. The second element is a memory flip-flop. This flip-flop is part of the double pulse suppression logic and prevents two pulses in succession from one output driver, independent of conditions on the SHUTDOWN terminat, $\overline{\text{RESET}}$ terminal or error amplifier inputs. Also included is a toggle flip-flop which alternately gates first one driver and then the other in the presence of a PWM signal.

The final elements in the block diagram are the source/sink output drivers, with a separate collector supply voltage terminal brought out for additional flexibility.

A simplified version of the undervoltage lockout circuitry is shown in Figure 16. The circuitry consists of a 1.2V bandgap reference and a voltage comparator which are fully operational for reference voltages greater than 2.1V. When the reference voltage is greater than 2.1V, the output transistor is turned on, inhibiting both power output drivers, It also holds the $\overline{\text{RESET}}$ line controlling the soft start circuitry in the low state, thus preventing the soft start capacitor from charging, and guaranteeing zero duty cycle.

Resistive divider R_1 and R_2 is scaled so that when the reference voltage reaches 4.5V the comparator changes state, thus releasing the soft start capacitor and also enabling the power drivers. Approximately 200mV hysteris is built into the comparator so that the transition from lockout to fully on is not accompanied by indecision and jitter.

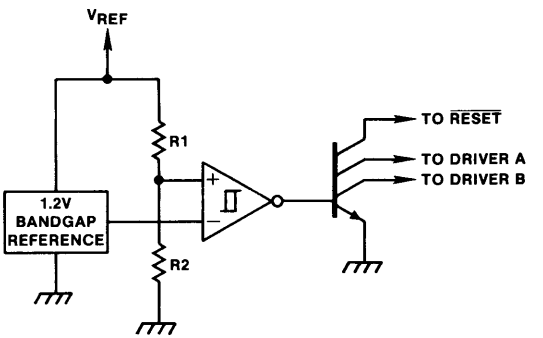


FIGURE 16. THE UNDERVOLTAGE LOCKOUT CIRCUIT CONTAINS A BANDGAP REFERENCE AND COMPARATOR WHICH BECOMES ACTIVE AT $V_{REF} = 3\ V_{BE} \approx 2.1$ VOLTS

Monitoring the reference voltage rather than the input terminal voltage has an additional benefit. With this particular configuration, this chip can operate on +5V by connecting the $+V_{IN}$ terminal to the $V_{REFERENCE}$ terminal and then regulating the input voltage between 4.5 and 5.5 volts. This is a desirable feature where other supply voltages must be generated from a regulated +5V source.

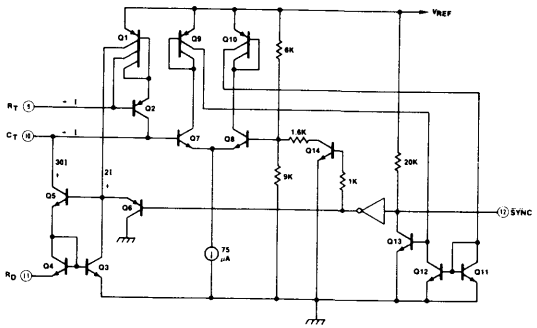
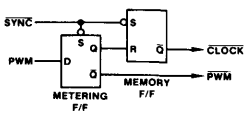


FIGURE 17. THE SG1526 OSCILLATOR PROVIDES DEADBAND CONTROL BY RATIOING THE CHARGING CURRENTS TO C_T

A simplified schematic of the oscillator of the 1526 is shown in Figure 17. A new approach is taken for controlling dead time in the circuit. The principle of operation is similar to the 1524 and 1525 oscillator. A timing capacitor is charged via a constant current programmed by an external resistance R_T. When the capacitor has charged linearly up to a nominal 3.2V, a voltage comparator changes state, thereby turning on a discharge network which reduces the capacitor voltage very rapidly to the +1V level. The distinctive difference between the oscillator in the 1525 and that in the 1526 is that the discharge network is a current source instead of a semi-saturating Darlington. In the 1526, the discharge circuit is formed by a compound current mirror, Q3, Q4 and Q5. The output current of this current mirror is ratioed to the current charging in C_T by a ratio of 30:1. This results in a charge time to discharge time ratio of approximately 29:1 independent of the value of C_T. This ratio can be modified to give longer dead times by insertion of a small amount of resistance from Pin 11 to ground. With this technique, dead times up to 50% or more are easily obtainable. This oscillator configuration has the advantage that the minimum dead time for the oscillator is now fixed at approximately 3% independently of the frequency of the circuit.

The remainder of the oscillator circuit functions similarly to that of the 1525. One notable exception is the TTL compatible buffer gate between the SYNC output pin and the remainder of the circuit. This enables the port to be bi-directional, driven either by open-collector TTL or by open-drain CMOS, or to itself drive other TTL or CMOS logic.



METERING FLIP-FLOP		MEMORY FLIP-FLOP	
DESCRIPTION:	ASYNCHRONOUS DATA LATCH	DESCRIPTION:	SET-RESET FLIP-FLOP
FUNCTION:	ALLOWS ONLY ONE PWM PULSE PER OSCILLATOR PERIOD	FUNCTION:	REMEMBERS WHICH OUTPUT PRODUCED LAST PULSE
BENEFIT:	SUPPRESSES HIGH FREQUENCY OSCILLATIONS	BENEFIT:	INHIBITS DOUBLE PULSING IN PUSH-PULL CONFIGURATION

FIGURE 18. SG1526 PULSE PROCESSING LOGIC

Figure 18 contains a brief explanation of the pulse processing logic in the 1526. The logic consists of two specialized flip-flops: a metering or data latch flip-flop, and a set/reset or memory flip-flop. The metering flip-flop is basically an asynchronous data latch which is enabled by a sync pulse from the oscillator during the beginning of every oscillator cycle. Once the metering flip-flop is enabled, a PWM signal may pass asynchronously through the device. However, once the signal is terminated for any reason, no new pulse can propagate through the data latch until a new sync pulse is received at the beginning of the next oscillator cycle. This feature allows each individual pulse to be terminated either by the action of the current limit comparator or by external circuitry which pulls the $\overline{\text{SHUTDOWN}}$ pin low. This feature allows the $\overline{\text{SHUTDOWN}}$ pin to be a convenient input port for a strobe pulse from symmetry correction circuitry.

The function of the memory flip-flop is to generate the clock pulse for the toggle flip-flop, which alternately gates the two output power drivers. It operates as follows: Let us assume that the flip-flop begins operation in the reset state. When a sync pulse is received from the oscillator, the $\overline{Q}$ terminal is then driven low, generating a clock pulse for the toggle flip-flop, which then changes state. If a PWM signal is generated during this oscillator cycle, then the flip-flop is reset, thus enabling it to generate another clock at the beginning of the next oscillator cycle. If no pulse width modulation signal is generated because the duty cycle has gone to zero or $\overline{\text{SHUTDOWN}}$ has been pulled low, then the memory flip-flop will not be reset, and when the next sync pulse occurs, no clock will be generated. In this way, the output flip-flop is toggled only upon generation of pulse width modulation signals, thus rendering it impossible for two successive pulses to be obtained from one output driver.

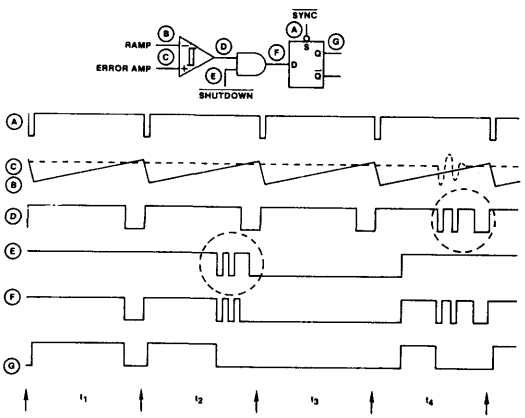


FIGURE 19. TIMING DIAGRAM OF THE PULSE PROCESSING LOGIC OVER FOUR OSCILLATOR CYCLES

The operation of the metering logic in the 1526 is shown in more detail in the timing diagram in Figure 19. The top waveform, Waveform A, shows the $\overline{\text{SYNC}}$ pulse train from the oscillator. This pulse tran defines four timing periods, T_1 through T_4, as shown at the bottom of the timing diagram. Waveform B represents the ramp signal from the master oscillator, while Waveform C represents the analog output signal from the error

amplifier. These two waveforms are differentially compared in the pulse width modulation comparator, whose output is shown as Waveform D. It can be seen that the error amplifier output voltage is just slightly less than the peak of the ramp signal from the oscillator, thus resulting in an output pulse which is approaching nearly full duty cycle. Waveform E is a $\overline{\text{SHUTDOWN}}$ signal from the current limit comparator. Alternately, this line could also show a digital input signal from other control logic. The waveform at line F represents the ANDed output of the PWM comparator and the $\overline{\text{SHUTDOWN}}$ signal. This acts as the date input to the metering logic flip-flop, whose output is shown as Waveform G.

The first time frame, T_1, illustrates a normal period of operation. The error amplifier calls for nearly full duty cycle; the $\overline{\text{SHUTDOWN}}$ pin stays high, and this output signal then passes unaltered through the metering logic flip-flop. During the second time frame, the $\overline{\text{SHUTDOWN}}$ pin is pulled low for several times during the active pulse period. This results in a series of pulses being applied to the data input of the metering logic flip-flop, but as can be shown in Waveform G, once the first pulse is terminated no other pulse can begin until the next oscillator cycle. During time frame T_3, the $\overline{\text{SHUTDOWN}}$ pin is low, thus preventing any PWM signals from reaching the metering flip-flop. In the fourth time frame, the disturbance at the output of the error amplifier causes multiple ramp crossings, which generates multiple PWM signals during one oscillator cycle. These signals reah the data input of the metering flip-flop, but as before, once the first pulse is terminated, the remainder of the pulses cannot propagate through the device to the output drivers.

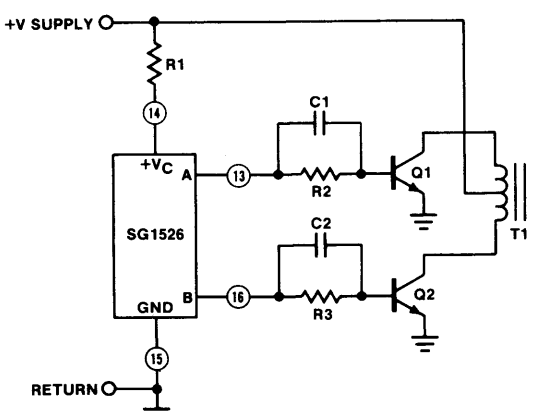


FIGURE 20. BASIC CONNECTIONS FOR A PUSH-PULL GROUNDED-EMITTER CONFIGURATION

The combination of source/sink drivers with a separate collector supply voltage terminal allows the output drivers to be easily interfaced with all the circuit configurations found in most switching power supplies. Figure 20 illustrates the connections for a common emitter push-pull configuration. In this circuit, the collector supply to the output source/sink drivers is tied to the supply voltage through R_1, which limits the voltage swing of each driver output, preventing emitter-base breakdown. During the turn off cycle, an additional spike of reverse base current is generated by the speed-up capacitor C_1 or C_2.

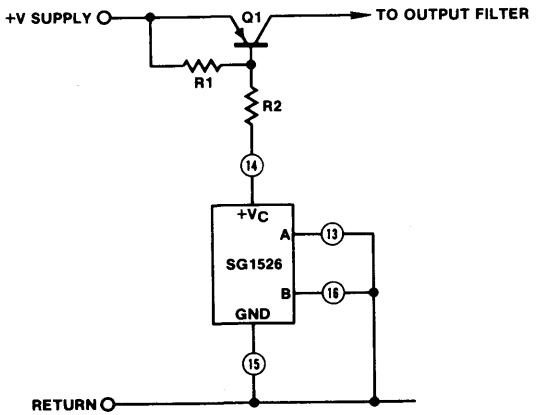


FIGURE 21. FOR SINGLE-ENDED CONFIGURATIONS THE V_C TERMINAL IS ALTERNATELY SWITCHED TO GROUND BY THE DRIVER PULL-UP TRANSISTORS

Buck-type converters are easily interfaced to the totem-pole output devices. For this mode of operation it is necessary only to ground the output terminals A and B, and drive the base of the switching device with the collector supply terminal. In this configuration, the upper Darlington transistors are alternately turned on and pull Pin 14 to ground, thus providing up to 100mA of current drive capability on alternate oscillator cycles.

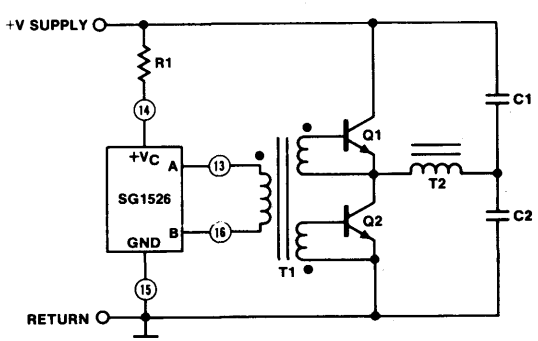


FIGURE 22. LOW POWER TRANSFORMERS ARE DRIVEN DIRECTLY BY THE OUTPUT TERMINALS

The totem-pole outputs can also drive a transformer directly, as illustrated in Figure 22. Since each output driver exhibits a low impedance, no center tap winding is required on the transformer primary. In this example, the transformer drive capability is used to interface the control device with the power transistors in a half bridge configuration.

If an additional current drive capability beyond that available in the 1526 is necessary, it is very easy to interface the output totem-pole drivers with the 1627 dual 500mA driver circuit. This is shown in Figure 23.

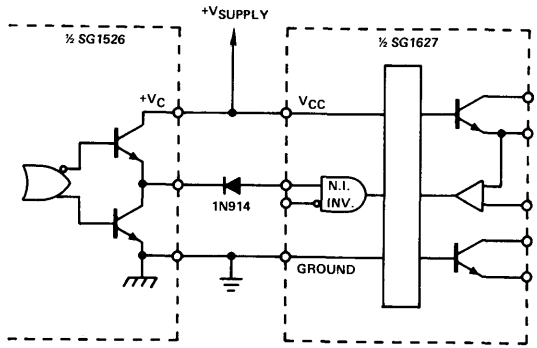


FIGURE 23. THE TOTEM-POLE OUTPUTS OF THE SG1526 CAN BE INTERFACED TO THE SG1627 POWER DRIVER WITH A HIGH-SPEED SWITCHING DIODE

The logic threshold of the 1627 is a nominal +2V, while the sink current in the low state is about 1mA. A fast silicon switching diode such as a 1N914 can be used to provide a sink current path in the low state, while blocking excessive input current to the power driver during the control circuit's high state.

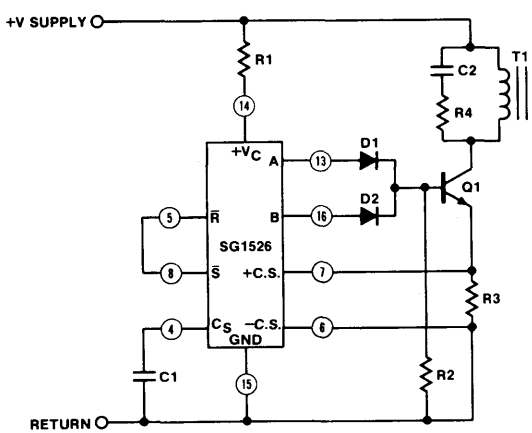


FIGURE 24. USING THE SG1526 IN A FLYBACK CONVERTER WITH CURRENT LIMITING

The ability of one control port of the 1526 to drive another control port enables a good deal of flexibility from the chip. The flyback converter in Figure 24 illustrates this point. Current limiting in a flyback converter is difficult because the overcurrent signal from the current sense resistor is always out of phase with the conduction of the principle power transistor. In this circuit, the output of the current limit comparator in the 1526 is used to re-trigger the soft start circuitry. By choosing the value of the soft start capacitor so that the recovery time of the soft start circuitry is of the order of one or two cycles, it is possible to provide current limiing with a minimal number of external components. This same technique can be used in a push-pull converter where it is desirable for the pulse width modulation signal to be turned off for multiple oscillator cycles rather than for a single cycle. This allows overstressed output semiconductors a cool-off period before returning to normal operation.

CONCLUSION

Several integrated circuits designed specifically for switch-mode power supply control have been described. A brief review has been made of past approaches to the integration of switching power supply control and driver circuitry. A description of a newly available family of control/driver integrated circuits, the SG1525/1527 series, has been given. Finally, a sketch of a future high performance controller circuit, the SG1526, has been drawn.

The future of integrated circuits for switching power supplies clearly involves greater complexity in the control circuitry to account for all possible modes of supply operation. The benefits for the power supply designer will be greater performance and reliability from switchers with reduced component count and greater overall manufacturing economies.

REFERENCES

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2. Robert A. Mammano, "Power Switch Drivers: New IC Interface Building Blocks for Switched-Mode Converters," Powercon 5 Proceedings, May 1978.

OUTPUT SUPERVISORY CIRCUITS: A NEW FAMILY OF POWER SUPPLY CONTROL DEVICES

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Edited by Stan Dendinger
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ABSTRACT

This paper describes a series of new monolithic integrated circuits designed to perform all the functions necessary to monitor and control the outputs of sophisticated power supply systems. Beginning with a simple over-voltage sensing circuit, these devices range through more versatile and accurate single-function units, to all-inclusive devices which contain sensing circuits for both over and under-voltage conditions, current sensing, SCR crowbar firing, logic outputs, and an accurate independent reference generator. A description of the operation each of individual element is given together with several applications which demonstrate their utility.

Introduction

Recent years have seen the introduction of many sophisticated integrated circuits for use in controlling the voltage regulation function of both linear and switching power supply systems. While these circuits have provided a high degree of performance with a side benefit of considerable increases in both reliability and cost savings, they have all addressed the basic function of maintaining the output voltage constant. Most power supply systems, however, require additional circuitry for monitoring satisfactory performance and providing protection in the event of a fault condition. These requirements have led to the development of a new class of power supply element — an Output Supervisory Control Circuit.

Supervisory Control Family Members

The first integrated circuit developed specifically as a power supply monitoring device was Motorola's MC3523 available also as an SG3523 from Silicon General. This device, which is packaged as an 8-pin minidip, was designed to sense an over-voltage condition, provide an adjustable time delay, and then fire a high-current SCR crowbar for power supply shutdown. An improved and interchangable device, the SG3523A, was later introduced to provide more tightly specified performance, greater threshold accuracy, and improved temperature stability. Block diagrams of these two devices are shown in Figure 1.

SG3523 OVER-VOLTAGE SENSING CIRCUIT

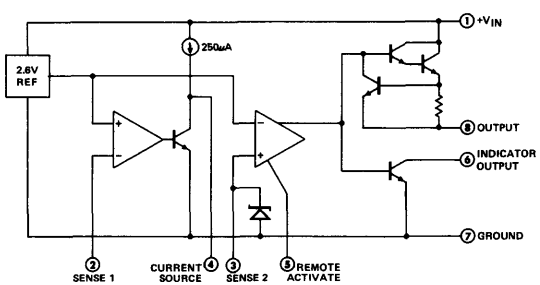

Figure 1. The SG3523 and 3523A contain an independent reference generator, an input comparator designed to initiate a setable time delay, and a second comparator which activates both a crowbar firing current and a low-level indication signal.

It was soon recognized that with the addition of a few more access points to this circuit, significant increases in versatility could be achieved. This led to the

development of the SG1542 device shown in Figure 2. With 14 pins in this DIL package the following additional features could be offered:

1. Access to the reference generator's output so that one could take advantage of it's 1% accuracy and 50 ppm T.C.
2. Uncommitted inputs to the sensing comparator allowing use for either under or over-voltage sensing as well as the ability to set threshold levels below 2.6 volts
3. The addition of a logic level output active when the sensed voltage is within tolerance, aswell as the one which indicates out-of-tolerance.
4. A separate supply terminal for the high-current SCR trigger allowing greater utilization of this output.

SG1542 VOLTAGE SENSING AND PROTECTION CIRCUIT

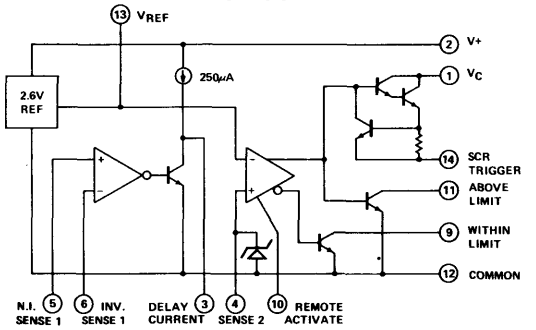

Figure 2. The use of a 14-pin package for the SG1542 provides greater access to the circuit elements and thus greatly expanded versatility.

Finally, it was decided to build an all-encompassing device which would include both over and under-voltage sensing as well as a means for current limiting, all in one integrated circuit. This resulted in the 16-pin SG1543, the main subject of this paper. The circuitry of the SG3523, 3523A, and 1542 is equivalent to the OVP portion of the SG1543 and thus need not be described separately.

Before proceeding with a discussion of the SG1543, however, there is one more member of this family worth mentioning. The SG1544 is identical to the SG1543, but uses an 18-pin DIL package to keep the voltage-sensing comparator inputs uncommitted. This adds the ability to sense voltage levels below the reference voltage to the lengthy list of features offered by the SG1543. Now, on to a more complete description.

The SG1543 Output Supervisory Circuit

To fill the need for this output monitoring and controlling function, the SG1543 output supervisory circuit shown in Figure 3 was developed. This device contains an operational amplifier, a voltage reference circuit, several comparators, and a high-current SCR trigger circuit. The functions performed by this device include over-voltage and under-voltage sensing, current limiting, and provisions for triggering an external SCR crowbar shutdown. All the functions provide open collector outputs for maximum flexibility in interfacing with either the power supply or the system load and, although the SCR trigger is directly connected only to the over-voltage sensing circuit, it may be optionally activated by any of the other outputs or by an external shutdown command. The SCR trigger circuit also includes an optional latch with external reset capability. External capacitors may be used to accurately program the sensing circuits for a minimum time duration of fault before triggering.

SG1543 BLOCK DIAGRAM

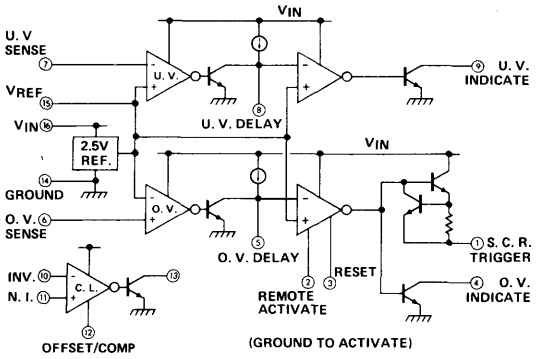

Figure 3. The block diagram of the SG1543 Output Supervisory Circuit includes over-voltage and under-voltage sensing as well as the capability for current limiting and SCR crowbar triggering.

The SG1543 circuit may be powered by either the output voltage to be monitored or a separate bias voltage at any level between 4.5 and 40 volts with a standby current of less that 10mA.

This device is packaged in a standard 16-pin hermetically sealed ceramic package and is available in both commercial and military temperature ranges. Before describing in greater detail the overall functions that this device can perform, it is worth discussing the individual circuits which go into its makeup.

Voltage Reference Circuit

The precision 2.50V reference circuit of the SG1543 is shown in Figure 4. This regulator is based upon the well-known band gap reference circuit which has the capability of providing very stable performance over an input voltage range from as low as 4.5V to as high as 40V. The output is nominally set at 2.50V, but in addition, is trimmed to remove all effects of production manufacturing tolerances from the output voltage. In

PRECISION 2.50 VOLT REFERENCE

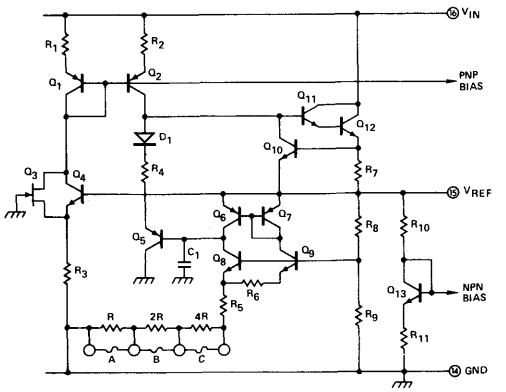

Figure 4. This precision 2.50 volt band-gap reference source is internally trimmed for ±1% accuracy in order to eliminate the need for adjustment potentiometers.

fact, this trimming not only adjusts the output voltage to within 1% of 2.50V, but in the process, as shown in Figure 5, also trims the temperature coefficient of output voltage to better than 50 parts per million per degree C. The trimming is performed at wafer probe by using controlled energy sources to blow fusable metal links which short out incremental values of resistance in the voltage setting network. These resistors are binarily coded so that three values give eight bits of resolution and allow trimming to better than ±12 millivolts. With this accuracy, in all but the most precise applications, the need for adjustment or trimming potentiometers is effectively eliminated.

CHANGE IN TEMPERATURE COEFFICIENT WITH REFERENCE VOLTAGE TRIM

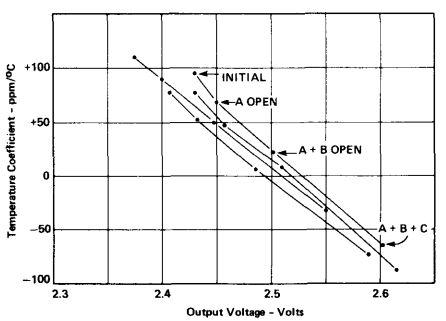

Figure 5. As successive links are opened in the reference voltage trimming network, the output voltage increases and the temperature coefficient becomes less positive.

The output of this reference circuit is current limited for protection and will provide up to 10 milliamps of current for use as a reference for other functions that may be required along with the SG1543. In addition to stable temperature performance, this regulator also maintains its output voltage to within 10mV for all line and load changes. Additional benefits of the band gap reference circuit include low noise performance, instant turn-on, and a high degree of long-term stability.

Comparator Section

Over and under-voltage sensing circuits are identical with only the input polarity changed between them. The under-voltage circuit is shown schematically in Figure 6. This configuration is made up of two comparators in series, each referenced to 2.50 volts, with the delay terminal at their juncture. The first comparator activates a current source upon sensing an out-of-tolerance condition and that current is used to charge an externally selected capacitor to provide a delay. The second comparator then activates the output indicating circuit. The overall time delay from input sense to output indicate, with no external capacitor, is approximately 0.5 microsecond. By adding a capacitor at the delay terminal, the fault must

VOLTAGE SENSING COMPARATORS

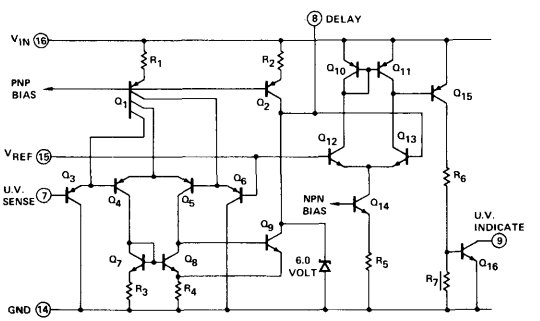

Figure 6. Voltage level sensing is done with a high input impedance comparator with built-in hysteresis. When switched, the input comparator allows a constant current source to trigger the output comparator.

exist for an interval defined by the time it takes the voltage on the capacitor to charge from zero to 2.5V before the output comparator can switch. The charging current for this capacitor is a constant 250 microamps which provides for a delay of approximately 10 milliseconds per microfarad of capacitance. Since the comparator can discharge in excess of 10mA, the capacitor is reset in a fraction of its charge time.

The input comparator has PNP transistor inputs which provide both high input impedance with less than one microamp bias current, and a wide input voltage range which includes ground and goes to within 2V of the positive supply voltage. Because the input PNP operates as an emitter follower, the input impedance to that comparator remains high throughout the input range. To eliminate the tendency to oscillate at threshold, a hysteresis of approximately 25mV is built into the input comparator.

The output indicating transistor, Q18, is designed to sink 10mA of current with a saturation voltage of less than 0.4 volt. Its open collector allows several outputs to be connected together to provide a single indicating signal.

SCR Trigger Section

While the under-voltage sensing circuit has only the 10mA, or low current, open-collector output, the over-voltage section contains additionally, an SCR crowbar triggering circuit good for 200mA. This stage also includes provisions for remote activation of the output as well as a reset terminal. From the schematic shown in Figure 7, it can be seen that the output voltage comparator drives a PNP transistor, Q6, with two collectors, one of which drives the low-current, open collector indicating signal similar to the under-voltage

OVER-VOLTAGE CIRCUIT

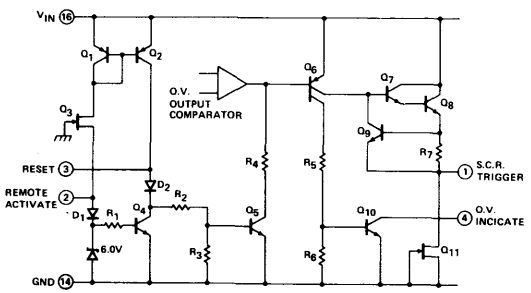

Figure 7. Either the over-voltage output comparator or the remote activation terminal will energize both the SCR trigger and the O.V. indicating transistor. Connecting pins 4 and 2 form a latch.

circuit. The other collector of Q6 drives a darlington amplifier which will provide 200mA to activate an external high current SCR crowbar device. Note that these two outputs are complements of each other; i.e. when pin 4 switches to ground, pin 1 goes positive.

Since in many cases it is desired to activate the crowbar under other than over-voltage conditions, a remote activation circuit is also included. This consists of transistors Q1 through Q5 as shown in Figure 7. The functioning of this circuit is as follows: Q3 provides a controlled current source of approximately 300 microamps to saturate transistor Q4. With Q4 saturated, transistor Q5 is held in the off condition. When the remote activation terminal, pin 2, is grounded, it diverts the current away from the input of Q4, turning it off and turning Q5 on, which activates the output circuitry in the same manner as the over-voltage comparator.

An additional function of this circuit is to provide the capability to latch the outputs on after a fault is sensed, by externally connecting the over-voltage indicating terminal, pin 4, to the remote activation terminal, pin 2. With this configuration, an over-voltage condition which turns on Q10 will pull pin 2 to ground activating the remote activation signal which, in turn, holds the circuit in the on condition until the reset terminal is externally grounded, removing the latch and turning off the output. Thus, the user has the capability to either activate the high current output only as long as a fault condition exists, or to latch it on upon the occurrence of a fault requiring external action by an operator to reset the circuit to its initial condition. Thresholds for both remote activation and reset teminals are approximately 1.2 volts.

Current Sensing Amplifier

The amplifier in the SG1543 designated for current sensing actually has much wider application. It is basically a high-gain, non-compensated operational amplifier with an open collector output; i.e., pull-up on the output must be provided externally. From the schematic shown in Figure 8, it can be seen that this circuit also has a PNP front end which gives it a wide common-mode range extending from slightly below ground to within 2 volts of the supply voltage. With a pull-up resistor of 2kΩ, the open loop voltage gain is greater than 72dB with a unity gain bandwidth beyond 5MHz. When used as a comparator, the response time is less than 200 nanoseconds, and if linear amplification is required, external compensation may be added for stable performance over a wide frequency range or a unique frequency response.

The input to this amplifier is balanced for zero offset voltage but a fixed offset or threshold of up to 200mV

CURRENT–SENSING AMPLIFIER

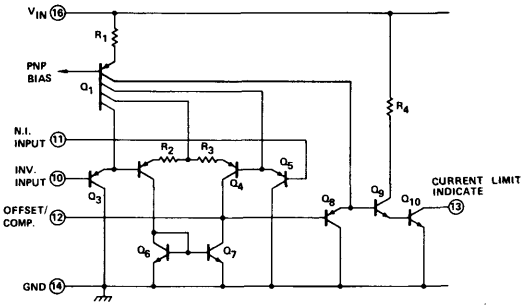

Figure 8. PNP inputs give the current limit amplifier a common-mode input voltage range of from below ground to within 2 volts of the supply voltage.

may be incorporated by adding or subtracting current at the offset/compensation pin 12. For most current sensing applications the required threshold polarity calls for a positive voltage on the inverting input. This can be accomplished with a resistor, RT, to ground as shown in Figure 9.

CURRENT SENSE COMPENSATION

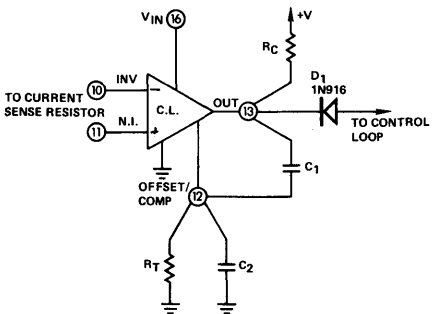

Figure 9. External components can be used with the current sense amplifier to establish an input offset or threshold, define the frequency response, and buffer the output.

Reducing the impedance at pin 12 also lowers the gain of the amplifier somewhat as shown in Figure 8. This fact allows pin 12 to do double-duty as a point to apply frequency compensation as well. Due to the excess phase shift of the internal PNP transistors, this amplifier requires compensation for stable closed-loop, linear applications but this can be accomplished easily with either C1 to the output or C2 to ground as shown in Figures 9 and 10.

C.L. AMPLIFIER FREQUENCY RESPONSE

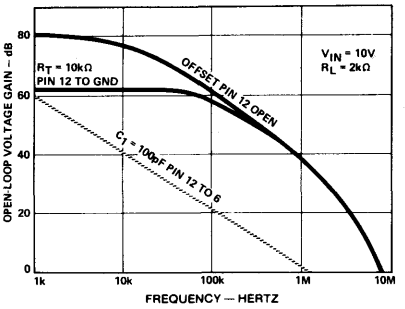

Figure 10. With 80dB gain and 5 MHz bandwidth, the current sense amplifier provides a wide dynamic response, even when modified with external passive components.

Diode D1 and resistor RC are used only if it is necessary to increase the frequency response by operating the output transistor at higher current and/or isolating the load from RC and C1 when the amplifier is off.

Applications

Figure 11 shows a typical application of the SG1543 as used to monitor a single power supply output voltage for both high and low voltage operation as well as current limiting. The data accompanying Figure 11 indicates how the values for the external components are selected. This circuit is driven from an external bias supply which must provide a standby current of 10mA maximum plus the activation current for the SCR trigger. The application in Figure 11 shows a single resistor divider string, R4, R5 and R6, which sets the thresholds for both the under and over-voltage activation levels. The external capacitors CD1 and CD2 are used to provide time delays before activation

SG1543 TYPICAL APPLICATION

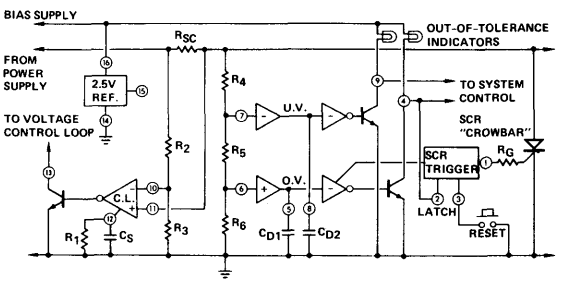

Figure 11. This typical application for the SG1543 provides linear foldback current limiting as well as over and under-voltage protection.

of the output circuitry. The output of the comparators can be used for many different functions; in this case, they are shown driving indicators. They can also provide signals to the system under power to give information that an out-of-tolerance condition exists. Additionally, by the external connection between pin 2 and pin 4, a latch has been provided such that an over-voltage condition will activate and hold that control signal until positive reset action at pin 3 is performed.

In firing an SCR with supply voltages above 5 volts an external resistor, RG, is used on pin 1 to provide power dissipation limiting for the SG1543. While the SG1543 will provide up to 400mA of trigger current, the power limitation of the 16-pin dual-in-line package should be held to less than one watt.

In this application, current limiting is performed by sensing the current in the positive supply line with fold-back provided by the action of R2 and R3. A fixed threshold for the amplifier is set by R1 which is connected between pin 12 and ground.

Although the SG1543 could have been driven from the output voltage to be monitored, it would lose control when that output voltage fell to approximately 3V. This would, of course, preclude the use of the current limit function where short circuit protection must be provided.

The values for the external components used in conjunction with the SG1543 application of Figure 11 are determined as follows:

Current limit input threshold, $Vth \approx \frac{1000}{R1}$

Cs is determined by the current loop dynamics

Peak current to load, $Ip \cong \frac{Vth}{Rsc} + \frac{Vo}{Rsc}\left(\frac{R2}{R2 + R3}\right)$

Short circuit current, $Isc = \frac{Vth}{Rsc}$

Low output voltage limit, $Vo\ (Low) = \frac{2.5\ (R4 + R5 + R6)}{R5 + R6}$

High output voltage limit, $Vo\ (High) = \frac{2.5\ (R4 + R5 + R6)}{R6}$

Voltage sensing delay, $td = 10{,}000\ Cd$

SCR trigger power limiting resistor, $Rg > \frac{Vin - 5}{0.2}$

Current Sensing Options

It is important to remember that all the features of the SG1543 apply equally to either linear or switching power supplies. Figure 12, for example, shows the current sensing amplifier in the SG1543 used to provide foldback current limiting for a linear regulator utilizing the SG723. To answer the question of why one would use the SG1543 for current limiting when that capability is built into the SG723, there are two important benefits: low sensing threshold voltage (whatever is selected vs. a fixed 700mV) and much higher gain for a very sharp transition from voltage to current feedback.

LINEAR FOLDBACK CURRENT LIMITING

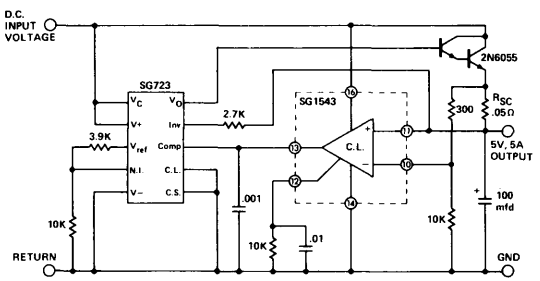

Figure 12. The SG1543 is equally adaptable to either linear or switching supplies. The circuit above shows a substantially improved current limit function for a linear SG723 voltage regulator.

Output current limiting for a switching supply which gets its control from an SG1524 regulating pulse width modulator is shown in Figure 13. Here, foldback is not included but an optical coupler for isolation has been added. It should be noted that all the low-current outputs of the SG1543 are equally well suited for driving optical couplers.

DC CONVERTER WITH ISOLATED CURRENT LIMITING

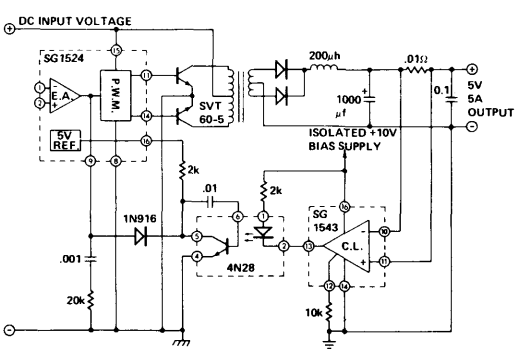

Figure 13. Current limiting for a switching inverter is readily accomplished, even with a requirement for input-output isolation.

This last application suggests another use for the current sense amplifier completely disassociated with current. This is shown in Figure 14 where it is used in conjunction with the very excellent characteristic of the 2.50 volt reference contained within the SG1543 to provide an isolated voltage feedback signal. The SG1543's amplifier provides the gain and the overall loop compensation network, and drives a high-frequency opto-coupler which feeds into the unity-gain configured error amplifier of the SG1524. A designer should recognize that there are many possible variations on this theme, including taking the error signal from the collector of the opto-coupler, feeding it into the output of the SG1524's error amplifier such that this amplifier provides a startup signal. Then the SG1543 may be powered directly from the output eliminating the need for an isolated bias supply.

USING THE CURRENT SENSE AMPLIFIER FOR ISOLATED VOLTAGE FEEDBACK

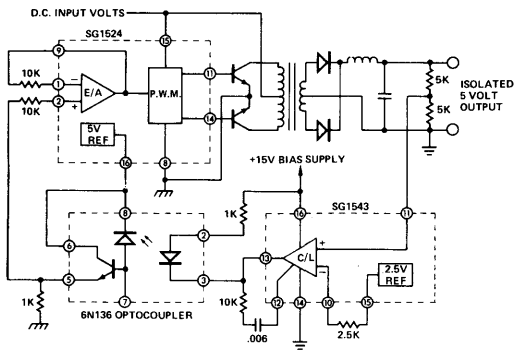

Figure 14. The current sense amplifier can also be used in conjunction with the SG1543's reference to provide a stable, isolated voltage feedback signal.

One final possible use for the current limit amplifier is to provide complete shutdown of the power supply rather than linear voltage reduction upon sensing an over-current condition. This function is shown in Figure 15 where the current limit amplifier is used as a comparator with the output terminal connected to the remote activation terminal for the SCR trigger. In this case, sensing is done in the ground line. There is no offset added to the current limit amplifier but instead a threshold is provided by the action of R1 and R2 from the 2.50V reference signal. When an over-current condition is sensed and maintained for a period of time determined by a capacitor CD on pin 12, then the output transistor will conduct, activating the SCR trigger and shutting down the power supply.

OVERCURRENT SHUTDOWN

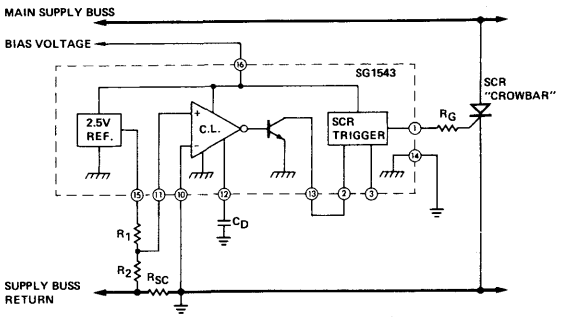

Figure 15. The current sense amplifier may also be used as a high-gain comparator to shut down the supply upon over-current.

Sensing Multiple Output Voltages

Many power supply systems have several output voltages which need to be monitored. This is easily done with the SG1543 because of the capability for remote activation and the availability of the reference voltage for use with external circuitry. A quad comparator like the SG139 which also has open collector outputs can be used to monitor several additional output voltages. As shown in Figure 16, the SG1543 is used to provide both over and under-voltage protection on a main positive supply. The additional comparators within the SG139 can be used to monitor either positive or negative supply voltages depending upon whether one uses the 2.50V signal or ground as the reference potential. The output collectors of each comparator are tied together to the remote activation terminal such that the operation of any single comparator in either the SG1543 or the SG139 will activate the SCR trigger shutdown circuit. Note that

SENSING MULTIPLE SUPPLY VOLTAGES

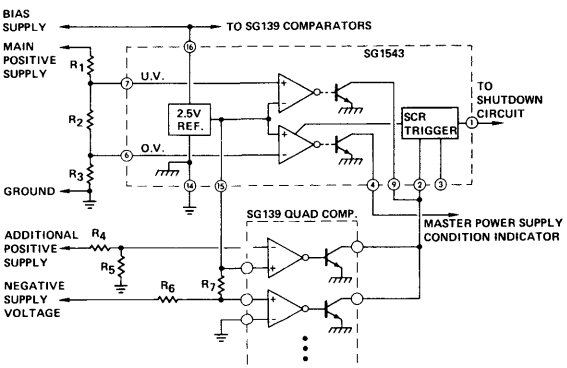

Figure 16. Addition of a simple quad comparator allows multiple voltage sensing of positive or negative levels.

grounding the remote activation terminal also provides an output on the over-voltage indicating circuit; therefore, this output on pin 4 can be used as a master power supply-condition indicator which will provide a low signal if any output voltage that is being monitored is outside its allowable tolerance.

Under-Voltage Sensing

In addition to normal low-output voltage monitoring, the under-voltage sensing circuit has considerable possibilities in monitoring the input voltage to a power supply system. For example, in Figure 17, this circuit is used to measure the input DC voltage to an SG723 regulator and keep the output completely off whenever the input is lower than the minimum required for satisfactory operation of the SG723. This same protective feature, when applied to a switch-mode regulator, is even more important since it keeps the switching transistors off until the oscillator stabilizes.

UNDER VOLTAGE SHUTDOWN

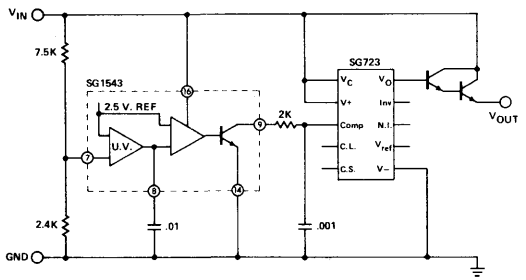

Figure 17. In addition to output monitoring, the under-voltage circuit can be used to inhibit the output if the input voltage is too low for satisfactory performance.

SG1543 INPUT LINE MONITOR

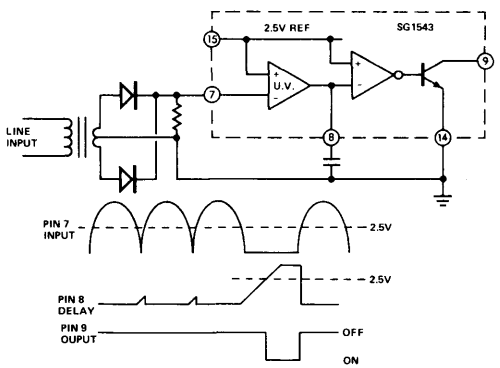

Figure 18. The under-voltage sensing circuit can also be used to monitor the AC input voltage and provide a power failure signal before the power supply output voltage begins to fall.

As shown in Figure 18, the under-voltage circuit can be used to monitor the AC input voltage to a power supply. An isolation transformer and rectifier are used to provide a rectified AC signal to the input of the under-voltage comparator. The signal is compared with the 2.50V reference, activating the first stage of the comparator with each transition toward zero. With proper selection of the delay capacitor, no output is provided unless some number of input pulses are missing at which time the first comparator allows the charging of the capacitor to 2.50 volts which activates the output circuit. In this way, the under-voltage circuit provides an immediate indication of failure, even for one or two cycles. This provides an early warning indication that the power supply output voltage is going to drop while taking advantage of the holdup capability provided by normal electrolytic capacitor storage within the power supply system.

Like other parts of the SG1543, the under-voltage circuit is not limited to its primary function. Figure 19 demonstrates its use as an over-temperature indicator by using the well-defined temperature coefficient of a darlington transistor's VBE as a sensor. Divider R1-R2 establishes a fixed threshold equal to the 2N2723's VBE at the desired temperature limit. Below that limit, the transistor is off and RC back-biases the input to the U.V. sensor. Many other transistors could be used; however, the small case of the 2N2723 makes good thermal coupling relatively easy.

OVER-TEMPERATURE INDICATION

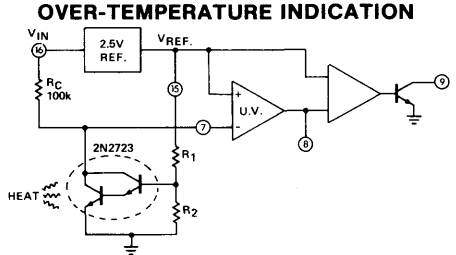

Figure 19. Another use of the under-voltage circuit is to provide an over-temperature indication using the −4mV/°C VBE tempco of the 2N2723 as a sensor.

By providing all of these diagnostic and protective features within one integrated circuit, a new class of control device has been generated to provide overall performance monitoring and control of sophisticated power supply systems. Thus, the SG1543 further enhances the inventory of building block components available to the power supply system designer providing new options in implementing increased performance at lower cost.

PROTECT YOUR SWITCHERS WITH DIGITAL CURRENT LIMITING

A New Current Sense Latch IC Provides Pulse-by-Pulse Current Control

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INTRODUCTION

Another new class of integrated circuits, designed specifically to ease the plight of the switch-mode power supply designer, has just been established with the introduction of the SG1549 Current Sense Latch IC. Although there have been many IC products developed over the past few years to provide simple methods of voltage control for switching supplies, the SG1549 is the first to specifically address and take a fresh approach to the problem of current control. Almost all existing PWM chips have included some type of circuit for current limiting, but these have all used the same techniques as linear regulators; that is, a current sense amplifier generates an error signal linearly proportional to load current which, after reaching an established threshold, takes command away from a voltage control amplifier. Thus, upon overload, the power supply switches from a voltage feedback loop to a separate current feedback path. Each loop must be stabilized separately and, because of the output filter, stable performance along with a reaction fast enough to protect the high-speed switching transistors is difficult to achieve. What is needed for optimum protection is a circuit which operates at the switching frequency and immediately turns off the main current-carrying switching transistors upon current overload. Turn-off must be rapid, without allowing the transistors any appreciable time in their linear operating region, and with no oscillation or multiple-pulsing.

A DIGITAL CURRENT LIMITER

The optimum approach to switch-mode current limiting is to treat each on-cycle as a separate problem. That is, pulse-by-pulse current limiting. This is implemented by a device monitoring current build-up each time the power supply's switching transistor conducts and, upon sensing an over-current condition, immediately turning the transistor off and holding it off for the duration of that normally on period. Such a circuit must have a latch, as once turn-off is achieved, the removal of the over-current signal would otherwise allow the transistor to return to conduction. Including a latch means a provision for reset must also be provided.

All of this and more is offered by the SG1549 Current Sense Latch IC. From the block diagram of this device, shown in Figure 1, it can be seen that the circuit includes a comparator with positive feedback, a means for establishing an input threshold of 100mV, a reset circuit, complementary outputs, and a high voltage level-shifting circuit. This device is designed to be completely compatible with many commonly-used Regulating PWM control IC's such as the SG1524, MC3420, and the TL494. Requiring only 2mA of supply current, the entire circuit can be operated from the reference voltage available with these chips, with reset accomplished by their clock output signals.

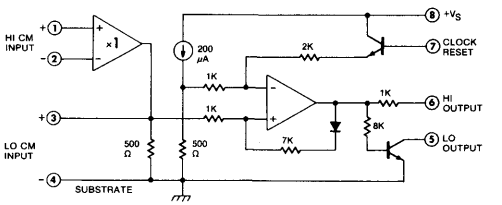

Figure 1. The SG1549 Current Sense Latch IC contains provision for sensing a current threshold over a wide voltage range. Complementary outputs and a latch with reset are also a part of this new protection circuit.

Although obviously designed for use with switch-mode power supplies, the SG1549 has broader application as a general purpose, low-threshold latch. A clock signal is not the only way to provide reset; that function may also be accomplished by any operation which will momentarily pull the reset pin high.

CIRCUIT OPERATION

For a detailed understanding of the operation of this device, refer to the schematic of Figure 2. With a +5 volt supply, a threshold reference is established by a current through R3. This current is mirrored by Q7 to provide a constant 200μA through R11, thereby holding one input to the comparator at 100mV above ground. That same current is mirrored through Q4 to the floating threshold circuit of Q1-Q3, D1 and R1. This portion of the circuit will convert a differential voltage between pins 1 and 2 into an identical voltage across R2. It will do this accurately while allowing the absolute voltage on pins 1 and 2 to range from 2 to 40 volts with respect to ground.

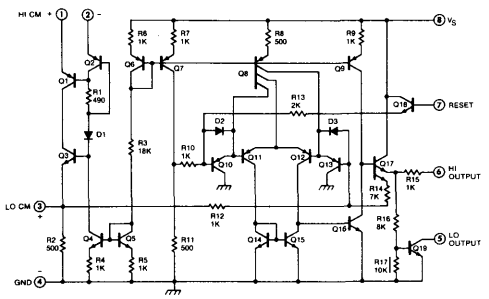

Figure 2. The heart of the SG1549 is a high-speed comparator together with an input threshold level-shifting circuit.

Since the other input to the comparator is tied to pin 3, it can be seen that the comparator will switch when the voltage on pin 3 rises to 100mV, regardless of whether that voltage is applied to pin 3 directly or differentially between pins 1 and 2.

Once the comparator switches, positive feedback provided by Q17 and R14 will hold it latched until a reset signal, effected by raising pin 7 above 2 volts, momentarily increases the threshold, returning the circuit to its initial state.

Transistor Q17 also provides two outputs: a high-going signal on pin 6 which can source 2mA and an open-collector saturating transistor on pin 5 which can sink more than 10mA. With complementary outputs, a variety of shutdown options are offered. Typical delay times for the SG1549 are 180 nSec from the LO CM input and 300 nSec from HI CM to the outputs.

HIGH LINE SENSING

A very straightforward application of the SG1549 is its use for current sensing in the input line of a simple buck converter as shown in Figure 3. This switching regulator is shown implemented with the SG1524 PWM control IC and it can be seen that interfacing between these two chips couldn't be easier. The value for R_{SC} is determined by dividing the 100mV input threshold by the peak current desired. High frequency noise, or switching transients can usually be eliminated by a small capacitor between pins 3 and 4.

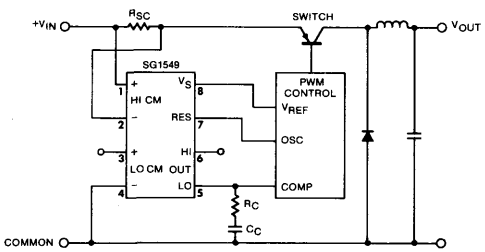

Figure 3. Using the SG1549 to sense input current to a simple buck converter and interface directly to a PWM control IC such as the SG1524.

The current shutdown command can be coupled into the SG1524 by either connecting the HI-OUT, pin 6 to the SG1524's shutdown pin or, as shown here, using the LO-OUT pin to pull the compensation terminal low. In either case, activation of the current sense latch will tend to discharge the compensation capacitor, C_C which may cause slow recovery from pulse limiting. Keeping the value of C_C as small as possible within the requirements of voltage loop stability will minimize this effect; however, slow turn-on from current limit is often desirable and can be optimized by using the LO-OUT signal to discharge a soft-start network instead of coupling directly into the SG1524.

Where minimizing turn-off delay is important, the command from the SG1549 may be taken directly to the output stage of a switching regulator. A practical means of accomplishing this is shown in Figure 4 where the power switch consists of an SM625 15-amp hybrid circuit containing both the power switch and the commutating diode. This switch is driven by using the SG1524 to switch a constant current source formed by the 2N2222 transistor connected with its base to the 5 volt V_{REF} line through a 1k resistor. By connecting the LO-OUT terminal of the SG1549 to the base of the 2N2222, drive current to the output stage can be interrupted without the delays inherent in the SG1524.

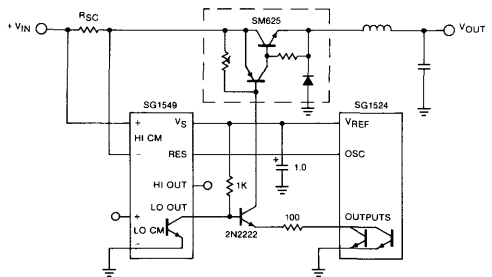

Figure 4. A fully-protected, high performance, single-ended switching regulator is easily implemented with two IC's and a hybrid switch. Current control is direct to the power switch for fastest response.

While the LO CM inputs may be connected directly across a sense resistor, R_{SC}, a small low-pass filter, R1-C1, is often helpful in removing high frequency transients. It must be remembered that the 500 ohm input inpedance to the LO CM terminals will cause the use of R1 to increase the effective threshold; however, this also offers the possibility of an easily adjustable threshold by incorporating a potentiometer at the input to the SG1549.

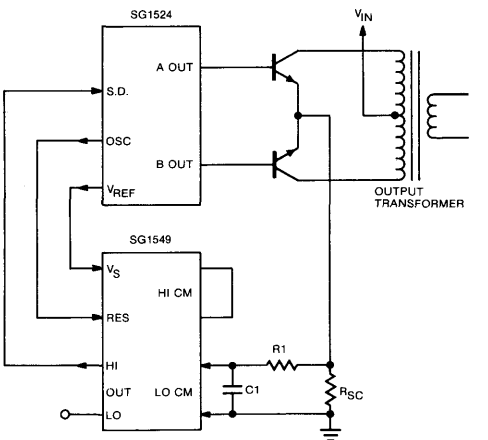

Figure 5. When sensing emitter current, a small input filter is often useful in eliminating transients to the SG1549.

LOW LINE SENSING

In many types of feed-forward or push-pull converters, current protection may be provided by sensing through an emitter resistor referenced to ground on the primary side of an output transformer. The fast-reacting SG1549 can easily sense secondary overload as reflected back to the primary and, additionally, provide protection from unbalanced transformer saturation. When using the LO CM inputs as shown in Figure 5, the HI CM inputs should be shorted together.

Coupling the current shutdown command back to the control circuit may be done in several ways as described above, but, again, the fastest approach is to go directly to the output switches. Figure 6 shows such an approach by adding two external shutdown transistors, Q1 and Q4. In this circuit, these transistors perform double-duty by the use of C2, R3 and R4 to generate a positive pulse when the main power switches, Q2 and Q3, are commanded off by the SG1524. Turn-off signals from either the PWM or the SG1549 are summed together through diodes D2 and D3 to Q1 and Q4.

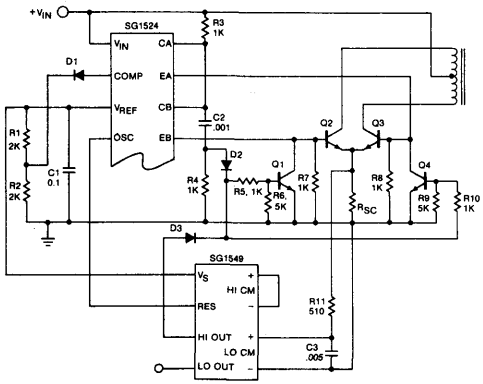

Figure 6. Fastest turn-off response is achieved by taking the output of the SG1549 direct to the power switches through turn-off transistors, Q1 and Q4.

One problem often experienced with using pulse-by-pulse current limiting with a push-pull inverter is half-cycling caused by limiting on one period without full recovery in time for the next. A maximum duty-cycle clamp, formed by R1, R2 and D1 in Figure 6, minimizes this effect by holding the error amplifier out of saturation when the feedback voltage begins to fall.

Another convenient way to tie the output of the SG1549 into the PWM control in higher power applications is by using the SG1627 Dual Interface Driver and connecting the LO-OUT terminal directly to the two non-inverting inputs of the SG1627 as shown in Figure 7. The N.I. inputs of the SG1627 will force the outputs off regardless of the commands on the inverting inputs, and do so within 100 nanoseconds.

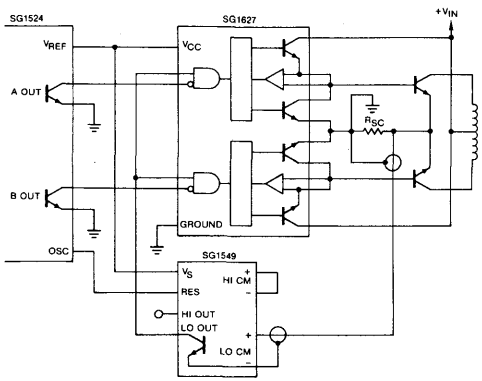

Figure 7. An SG1627 provides both power gain for the voltage control signal as well as a high-speed interface for the SG1549's current protection.

And finally, keep in mind that the LO-OUT terminal of the SG1549 will easily drive most high-speed optical couplers should some type of isolation between current sense and shutdown control be required.

POWER SWITCH DRIVERS: NEW IC INTERFACE BUILDING BLOCKS FOR SWITCHED-MODE CONVERTERS

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Abstract

This paper describes the characteristics and performance of two new integrated circuit products designed to interface between the control circuitry for switch mode converters and their high power output stages. The first device develops the high level turn-on and turn-off commands directly from the outputs of a low power P.W.M. control circuit while the second is designed as a floating switch to control a high current switching transistor directly from the secondary of a drive transformer.

INTRODUCTION

Recent years have seen significant developments by component suppliers which have resulted in the ready availability of many high performance power transistors and sophisticated control integrated circuits for switching power supply design. There existed a gap, however, between the control circuit and the power switching transistors where a considerable amount of circuitry was required to adequately condition and amplify the control signal in such a way as to provide the proper turn-on and turn-off commands to the power switch. This gap has now been filled with two new integrated power switch drivers, the SG1627 Dual Output Driver and the SG1629 High Current Floating Switch Driver.

SG1627 DUAL OUTPUT DRIVER

The SG1627 was designed to directly interface between low level control circuitry and the high current handling devices required in switching power supplies. As shown in Figure 1, this is a dual circuit containing both channels that are required for a push-pull system. It accepts the P.W.M. signals from a control circuit such as the SG1524 and provides the conditioning necessary to develop both turn-on and turn-off commands at currents up to 500mA. Its outputs can be used to directly control an external power transistor or to interface with driver transformers for additional power amplification. Another feature of this circuit is the optional ability to provide a constant drive current.

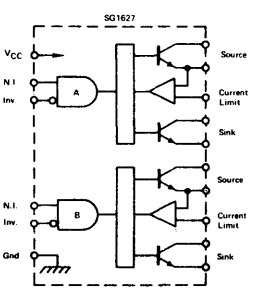


FIGURE 1 – THE SG1627 DUAL OUTPUT DRIVER IS PACKAGED IN A 16-PIN CERDIP D.I.L. PACKAGE.

CIRCUIT DESCRIPTION

Figure 2 shows the schematic for one-half of an SG1627 dual output driver. It must be remembered that there are two identical circuits in each 16 pin dual-in-line package. The inputs to this circuit are switch closures to ground with both inverting and non-inverting logic configurations available. The input threshold level of both logic inputs is 2V, and the logic is

powered by an internal voltage regulator so that input characteristics are unaffected by power supply voltage which can range from 5 to 30 volts.

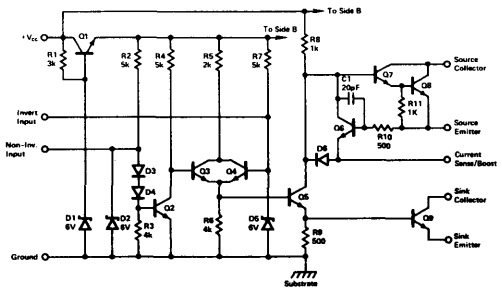


FIGURE 2 – SCHEMATIC DIAGRAM FOR ONE-HALF OF THE SG1627

The output sections of the SG1627 contain both source and sink transistors, each capable of 500mA, 30V operation. In addition, the source transistor has the capability of constant current operation by using an external sense resistor between the source emitter and the current sense terminals. The source transistor is in a darlington configuration which can easily deliver currents to 500mA under all operating conditions but at the cost, however, of a higher saturation voltage. The sink transistor is designed for very low saturation voltage: approximately 0.5 volts at 500mA. It does, however, need greater base drive to meet those high currents. This can be provided either by raising the supply voltage above 5V, or by adding a boost drive current through D6. The saturation characteristics of both source and sink are shown in Figures 3 and 4.

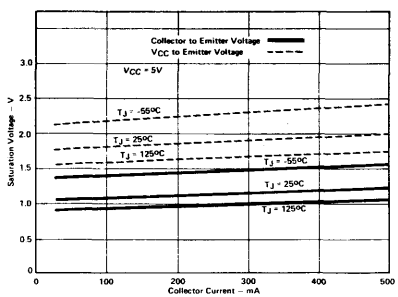


FIGURE 3 – SATURATION CHARACTERISTICS OF THE SG1627 SOURCE TRANSISTOR

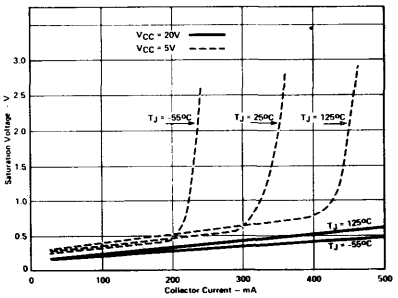


FIGURE 4 – SATURATION CHARACTERISTICS OF THE SG1627 SINK TRANSISTOR

THE TOTEM-POLE OUTPUT CONFIGURATION

One of the simplest uses of the SG1627 is illustrated in Figure 5 where the output is configured to provide a constant 300mA turn-on command to an external switching transistor together with a high peak turn-off current. Note that the logic on the SG1627 is being driven directly from the 5V reference terminal of an SG1524 P.W.M. control I.C. The logic inputs are directly connected to the open collector output transistors of the SG1524 with no additional interfacing components. The output current of the SG1627 comes from the input voltage, which in this case is approximately 10V, but the use of R2 provides a constant source drive regardless of input voltage variations.

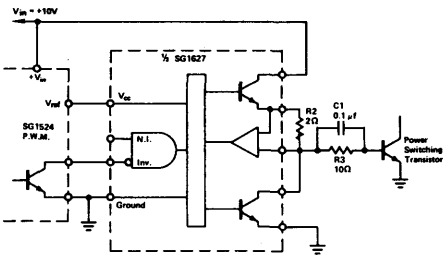


FIGURE 5 – IN A 300mA OUTPUT "TOTEM POLE" CONFIGURATION, THE SG1627 INTERFACES DIRECTLY WITH THE SG1524 REGULATING P.W.M. CONTROL CIRCUIT.

Resistor R3 is used to build up a voltage drop across capacitor C1. At turn-off, the energy stored in C1 provides both a negative voltage to the base of the power switching transistor and the boost drive current necessary to saturate the sink transistor during peak discharge currents of approximately 500mA. With this magnitude of reverse base current (Ib2), transistor turn-off is greatly accelerated.

There are two considerations to remember in this configuration. The first is that the maximum output voltage will be less than the value of Vcc because the source transistor operates as an

emitter follower. With Vcc = 5 volts in this case, the peak output voltage is approximately 3 volts. The other consideration is power dissipation in the source transistor when using it in the constant current mode since it will absorb any excess voltage after current limiting.

The performance of this application is illustrated in Figure 6 which shows the base current into the external switching transistor. One can see both the constant drive current of about 300mA and the rapid, peak negative turn-off current in excess of 500mA. Note that the delays through the SG1627 are less than 50 nanoseconds making a very fast responding circuit.

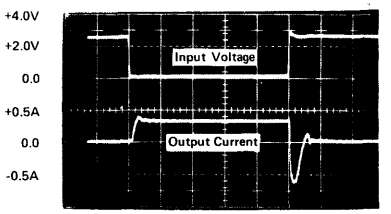


FIGURE 6 – OUTPUT CURRENT TRANSFER FUNCTION

An alternate configuration shown in Figure 7 pictures the SG1627 with a higher value of supply voltage. This offers at least two advantages; first of all, it allows the output voltage swing to rise considerably higher remembering that the source as an emitter follower can rise to approximately 2V below the input supply voltage. The other benefit is in providing greater drive current for the sink transistor allowing 500mA saturation without the need for additional boost current. Because of the large supply voltage across the source transistor, power dissipation can be a problem. This probably means a reduced source current if current limiting is required, although the use of resistor R1 to absorb some of the voltage drop will reduce the power dissipation within the SG1627.

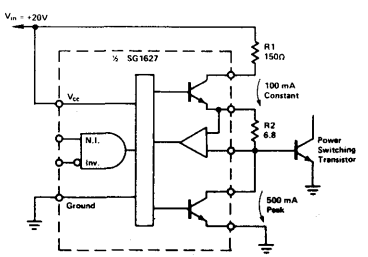


FIGURE 7 – HIGHER INPUT VOLTAGES CAN BE USED TO PROVIDE DRIVE FOR HIGHER SINK-TRANSISTOR CURRENTS

Recognizing the potential for package power limitations, it is important to consider the use of the SG1627 with various types of power boosting circuitry. Maximum flexibility for the use of external current boosting transistors is maintained by the uncommitted availability of both the collector and emitter terminals of both the source and sink transistors. Figure 8, for example, shows the use of an external PNP transistor to boost the source current to 1 amp. The use of the PNP transistor in this configuration still allows current sensing to be used for constant current operation. If constant current operation is not required, an NPN emitter follower booster could also be used. The use of a single boost transistor as shown in Figure 8 makes a powerful drive circuit as one can now drive one amp of turn-on current into a switching power transistor and still have 500mA of turn-off current through the sink transistor.

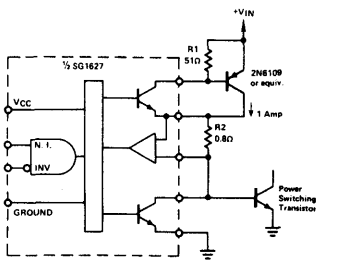


FIGURE 8 – INCREASED SOURCE CURRENT WITH THE USE OF AN EXTERNAL BOOST TRANSISTOR

DUAL PHASE OUTPUTS

The SG1627 does not need to be committed to totem pole operation. The source and sink transistors can be separated and used independently for dual opposite-phased outputs. Figure 9 shows the operation with both source and sink transistor emitters grounded and each used as a common emitter amplifier driving an external load resistor. Figure 9 also shows the use of an external resistor R1 to provide additional drive current boost to the sink transistor. This will allow the sink transistor to provide full 500mA operation with only a 5 volt supply. The response characteristics of this type of configuration are shown in Figure 10, which pictures the response of both source and sink with 24 ohm load resistors to inputs at both the inverting and the non-inverting logic inputs. Note again the minimum delay of both outputs; less than 100 nanoseconds from input to output on both source and sink.

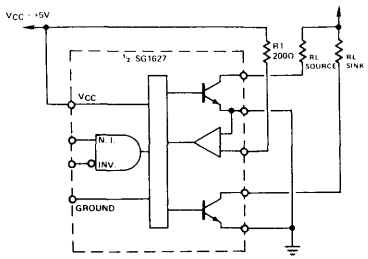


FIGURE 9 – SEPARATE DUAL-PHASE OUTPUTS WITH ADDITIONAL DRIVE CURRENT FOR 500mA SINK TRANSISTOR OPERATION

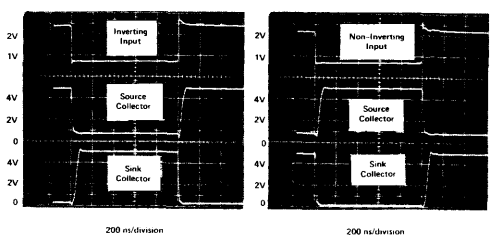


FIGURE 10 – SOURCE AND SINK RESPONSE CHARACTERISTICS

This use of the source and sink as separate outputs provides significant benefit for driving a transformer, as illustrated in Figure 11. In this example, the primary winding of the transformer is driven by the source transistor with its emitter grounded. Constant current operation is shown with the inclusion of the sense resistor, R2, but voltage switching could as easily be accomplished by merely shorting together the sense terminals. To provide greater efficiency in the magnetic design, a reset winding is added and shown being driven by the sink transistor. This ensures that the magnetic flux is reset to zero between each pulse. Of course, the sink transistor opens up every time the source transistor drives the primary winding.

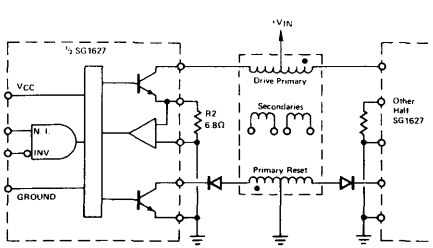


FIGURE 11 – DRIVING AN OUTPUT TRANSFORMER WITH THE SG1627

An additional illustration of the versatility of the SG1627 is shown in Figure 12, where the non-inverting logic input is used to provide a positive guarantee that both sides of a push-pull inverter cannot be on at the same time. This circuit is shown using the inverting input as the primary drive path, which will force the source transistor to be on when the control circuit transistor is conducting. The non-inverting input is then diode-coupled to the opposite side of the inverter and senses saturation of the external power switch. If the collector of the opposite transistor is low, holding the non-inverting input low, then regardless of what happens at the inverting input terminal, the output source on that side cannot be turned on. The sink will remain on, holding the output low until a rising collector voltage on the opposite side removes the non-inverting input at which time the command signal will then come through the SG1627 and turn on the correct side. This circuit is particularly useful as a protection against cross-conduction of the output transistors during transient conditions at power-on or overload.

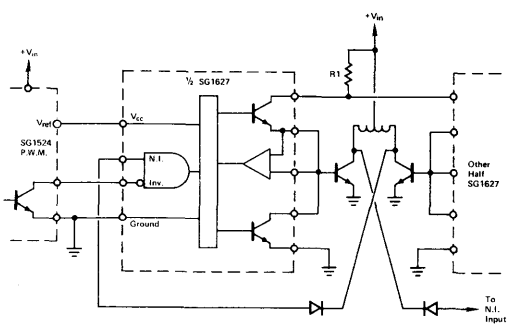


FIGURE 12 – SIMULTANEOUS CONDUCTION OF THE TWO OUTPUT TRANSISTORS IS PREVENTED BY GATING WITH THE NON-INVERTING INPUTS.

The above examples have been chosen to illustrate the versatility and performance of this new device designed to interface between a low level pulse width modulating control circuit and the high power switching transistors used in all modern-day switching power supply designs.

THE SG1629 HIGH CURRENT FLOATING SWITCH DRIVER

A second interface circuit to be discussed in this paper is the SG1629 illustrated in Figure 13. This device has been designed to provide an interface between a drive transformer secondary winding and a high power switching transistor, and again provide the proper signal conditioning to adequately deliver both turn-on and turn-off current into the base of that switching transistor. More importantly, its design is such that it requires no external power connection but develops all the power for

both turn-on and turn-off from the drive transformer and an external storage capacitor. With this capability, the SG1629 can be used in floating operation for bridge inverters at voltages in excess of 300V with respect to ground. This circuit also contains the capability for constant current drive operation with a similar type of current sensing circuit and an external current sensing resistor.

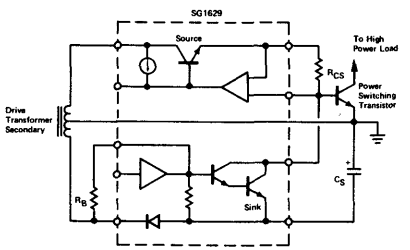


FIGURE 13 – THE SG1629 HIGH-CURRENT, FLOATING SWITCH DRIVER

CIRCUIT OPERATION

The SG1629 functions with a center-tapped drive transformer secondary winding such that when a turn-on command is present and current is flowing in the upper half of the secondary winding through the source transistor and into the base of the power switching transistor, a current is also flowing in the lower portion of the transformer secondary through the high current rectifier to charge the external capacitor C_S to a negative voltage. When the drive command terminates, this negative voltage is used to turn on the sink transistor which then pulls a negative Ib2 current from the base of the switching power transistor down to the negative voltage on the capacitor providing again a high peak turn-off current to speed the response and minimize the power losses in the switching transistor. For maximum versatility, this circuit also contains several gating options.

In Figure 14, the schematic of the SG1629 shows two power darlington transistor structures, each capable of handling an excess of 2 amps of current: Q3/Q4 as the source, and Q6/Q7 forming the sink. Transistor Q5 provides current sensing with feedback to provide constant current operation. The source transistor is turned on by conduction of drive current through resistor R2. The drive current for the source transistor is gated on and off through the action of Q1 which senses the input voltage and provides a turn-off of the source transistor between each drive current pulse.

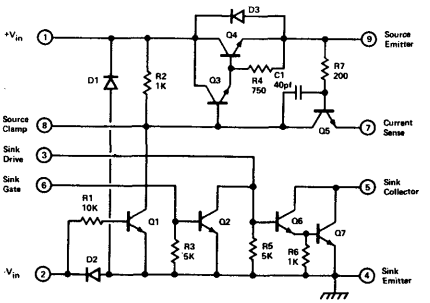


FIGURE 14 – THE SCHEMATIC OF THE SG1629. TRANSISTORS Q4 AND Q7 ARE DESIGNED FOR TWO-AMP OPERATION.

The darlington sink transistor has its input brought out as a separate sink drive terminal which gives the user several driving options. In addition, the sink driving current can be gated by the use of Q2, which has its own input terminal. The diodes D1 and D2 are high current rectifiers which provide the charging current for the external capacitor attached to the sink emitter terminal. The action of transistor Q1 to gate the source transistor insures that there is negligible discharge current (less than 10mA) from the external capacitor during the off periods of the circuit. This allows the capacitor to be charged with very narrow drive pulses separated by relatively long off periods.

The SG1629 is packaged in both a multi-pin TO-66 power package and an 8-pin minidip. Having no sensitive, low-current circuitry, this device can be operated with a maximum junction temperature of 175°C which, coupled with a low Θ5C thermal resistance of 5°C/W, gives the TO-66 package a 3 Watt capability in free air and 10 Watts or more with some heat sinking. Because of the versatility of this device, it was felt that there may be applications for lower power requirements and thus the SG1629 will also be available in an 8-pin ceramic minidip package which, of course, has a power dissipation of only 800mW. With one pin less in the 8-pin minidip package, the sink gating function is sacrificed.

SG1629 APPLICATIONS

The use of the SG1629 can best be demonstrated in an application as shown in Figure 15 where two SG1629's are used to provide the drive signals for the power transistors in a 5 amp one-half bridge switching supply. The drive transformer is shown with 10 volt drive signals on the primary winding which, with a 2:1 transformer turns ratio, provides a 5V peak signal on each half of the secondary. When the drive command is present on one secondary, it is translated into a constant current through the source transistor by the use of the sense resistor,

Rcs, which, in this case, provides a constant 700mA into the base of the external NPN transistor. At the same time, the 20 microfarad external capacitor is being charged with a current through the rectifier in the SG1629 and the lower half of the secondary winding. While this is occurring, the opposite phase signal is being applied to the lower SG1629 circuit which serves to further enhance the charge on its external capacitor while maintaining the power switch in the off state.

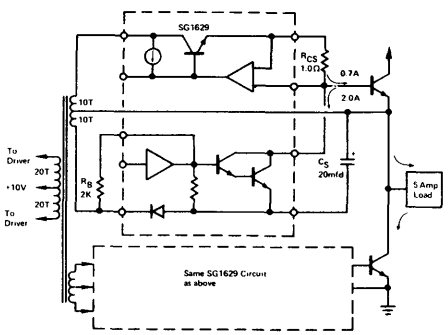
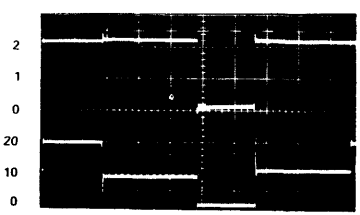


FIGURE 15 – USE OF THE SG1629 IN A 5-AMP, HALF-BRIDGE CONVERTER

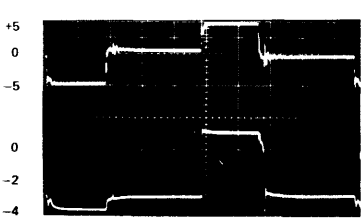
When the drive command terminates, the voltage at both ends of the secondary winding goes to zero. Since there is approximately -4V at the emitter of the sink transistor while its base is being driven through the external drive resistor, RB, to zero volts, the sink transistor then immediately turns on and pulls a high current Ib2 pulse out of the external transistor and through the capacitor. This current, of course, only flows as long as it is available from the stored charge within the base of the external transistor as the source has been gated off. After that charge is depleted, the sink transistor remains on insuring a negative reverse voltage at the base of the switch transistor.

The performance of the SG1629 can be illustrated by the waveform photographs in Figures 16 through 18. In Figure 16, the command signal from one channel of the control circuitry and the waveform of the drive transformer primary voltage are shown. The voltage on the secondary winding, referenced to the centertap and the power transistor emitter, is pictured in Figure 17. Also shown in this photograph is the input voltage at the base of the external NPN transistor. Note that at the very first portion of this waveform, when the opposite side is on, there is an additional negative charge supplied to the capacitor so that we have a maximum reverse base-to-emitter voltage of close to -4V. During the off time, the action of the sink transistor maintains a negative voltage bias of approximately -3V on the base of the power transistor. When the drive command is given to turn on, the base voltage goes positive to the 0.7 or so volts necessary to turn it on and at turn-off, goes negative again. The important action is shown in Figure 18 which pictures the actual base current of the power transistor with a scale of one amp per division. Both the constant turn-on Ib1 of about ¾ amp and the peak Ib2 of close to -2 amps can be seen along with the collector voltage waveform with a 5 amp resistive load. Remembering that the time base of all these waveform photographs is 5 microseconds per division, one can see approximately one microsecond delay between the turn-off signal at the base and the actual turn-off of the collector of the output transistor. Although this turn-off response is primarily a function of the transistor design, it is safe to say that any power switching transistor should perform faster with this form of base drive.



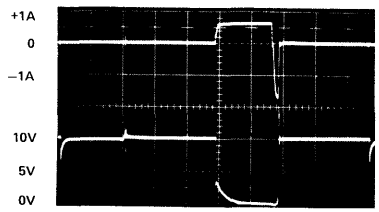
Time Base: 5 μSec/Division
Upper Trace: P.W.M. Control Signal
Lower Trace: Drive Transformer Primary

FIGURE 16 – INPUT CONTROL TO THE DRIVE TRANSFORMER



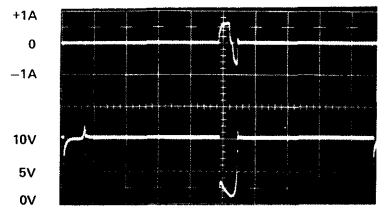
Time Base: 5 μSec/Division
Upper Trace: Drive Transformer Secondary
Lower Trace: Power Transistor Base Voltage

FIGURE 17 – THE BASE VOLTAGE DELIVERED TO THE EXTERNAL POWER SWITCHING TRANSISTOR BY THE SG1629



Time Base: 5 μSec/Division
Upper Trace: Transistor Base Current
Lower Trace: Collector Voltage with $R_L = 2\Omega$

FIGURE 18 – BASE CURRENT AND COLLECTOR VOLTAGE OF THE EXTERNAL SWITCHING TRANSISTOR



Time Base: 5 μSec/Division
Upper Trace: Transistor Base Current
Lower Trace: Collector Voltage with $R_L = 2\Omega$

FIGURE 19 – OPERATION WITH NARROW PULSE WIDTHS

Note that one can also see in the collector waveform a soft knee at turn-on where the power transistor is not saturated instantaneously. This is partially because of the turn-on characteristics of the transistor and partially because of the finite rise time of base current through the driving circuitry. This rise time is primarily a function of the leakage inductance of the drive transformer which opposes a sudden change in current from zero to maximum value. It is an exercise in transformer design to configure the transformer to minimize to the greatest extent possible the leakage inductance. This can be done with a minimum number of turns and a maximum coupling between turns. In the illustration, a ferrite pot core of approximately ¾" in diameter was used to configure the drive transformer. More will be said about turn-on rise time later, but first let's discuss one additional characteristic of concern in the turn-off circuitry: The operation with very narrow pulse command.

Since the charge on the external capacitor is developed during the turn-on command, narrow pulse widths accomplish the transfer of a minimum amount of energy. As the drive command pulse widths get narrower, there is a point where the voltage on the external capacitor begins to fall off. With the circuit components as shown earlier, this loss of Ib2 occurs at approximately 2 microsecond pulse widths. Figure 19 shows the base current and collector voltage waveforms at narrow pulse widths where the Ib2 has diminished from 2 amps down to approximately ¾ of an amp. Further reductions in pulse width bring the Ib2 current ultimately to zero. This characteristic is, of course, a function of the time constants in the total circuit and some compromise or optimization can be achieved by appropriate selection of capacitor values and secondary drive voltages.

The above circuit incorporated constant current drive which is an advantage if the load current happens to be relatively constant but in many applications this is not the case. The SG1629 may also be used to provide a base drive proportional to load demand by adding an anti-saturation clamp diode as shown in Figure 20. With the current sense terminals shorted, there are two V_{BE} voltage drops between the clamp and source emitter terminals. Therefore, the clamp diode D1 will hold the collector on voltage to approximately one diode drop above the base. This will keep the switching transistor right at the threshold of saturation, regardless of load current variations.

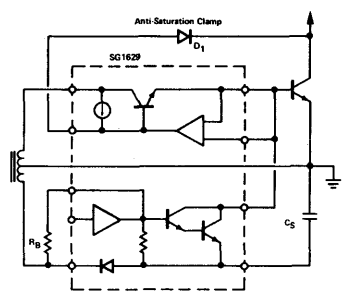


FIGURE 20 – USE OF THE SG1629 IN A LOAD-DEPENDENT DRIVE CONFIGURATION

IMPROVING TURN-ON RESPONSE

In applications where maximizing base current rise time is important and secondary transformer inductance is a significant consideration, the use of the gating functions in the SG1629 can provide significant benefits. Figure 21 shows the addition of an external transistor Q1 to drive the sink transistor's gate circuit. To explain the operation of this circuit, note that the sink transistor's base drive is now being generated with RB connected to the common or center tap of the drive transformer secondary instead of the negative input terminal. This is essentially zero volts and since the emitter of the sink transistor

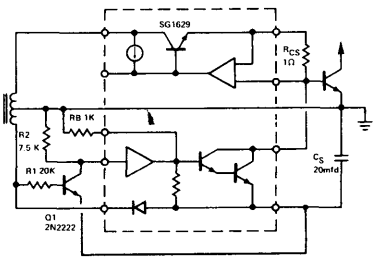


FIGURE 21 – IMPROVING BASE CURRENT TURN-ON RISE TIME

is attached to the capacitor which has a negative voltage on it, the sink transistor would normally be on continuously. Transistor Q1 is selected as a relatively slow non-gold-doped transistor which has a finite storage time. Its action is to turn the sink transistor off during the drive command signals, but to delay that off signal for some increment in time. Note that before the commencement of a drive command, the sink transistor is on by the action of RB. Transistor Q1 is also saturated by its base resistor being connected to the end of the transformer which is also at zero volts prior to the command signal.

When the drive command is initiated, current begins to build up in the secondary circuit and the first flow of current is through the source transistor, through the current limiting resistor, down through the sink transistor which is still conducting, and back to the negative terminal on the transformer secondary. The switching transistor is still back-biased while this occurs. Because the input to transistor Q1 is now at a negative voltage, it turns off, but since it has a finite storage time, that time is used to delay the rise of the input to the sink gate. Additional delay can be added with a small capacitor at the sink gate input terminal. When the input to the sink gate goes high, its output goes low, forcing the sink transistor to turn off. Since the source current is already flowing, turn-off of the sink diverts that current to the base of the output transistor producing an Ib1 rise time of less than 100 nanoseconds.

When the action is reversed at turn-off, there is negligible increase in delay between the turn-off signal and the actual turn-on of the sink transistor. This is because Q1 is the only device with a long storage time and it is turning on so storage is not a factor.

Another method of speeding up the rise time of current into the base is the use of some reactive components to differentiate the drive current signal. A simple approach is a capacitor by-pass around the current sense resistor, Rcs, providing an initial boost in turn-on current.

GETTING IT ALL TOGETHER

The overall simplifications which Silicon General has offered to the design of switch mode power converters can best be illustrated by Figure 22 which shows the total command signal flow from the feedback error information to the output of a high current half-bridge regulating inverter. The SG1524 was designed to provide all of a switching regulator's P.W.M. control signals with the only external components required being the divider resistors to interface with the error amplifier, the overall loop compensation network, and the resistor and capacitor to set the operating frequency. The SG1524 drives the SG1627 directly which, in turn, provides the signal conditioning to develop the drive and reset commands to an interstage drive transformer. The secondary windings of that drive transformer are directly coupled into a pair of SG1629 floating drivers which are then used to command the external 5 amp switching transistors which form the high power output stage of the power supply.

These circuits have all been designed to offer a maximum degree of flexibility while incorporating what would otherwise be a substantial amount of discrete circuitry.

Thus, all these new IC's greatly ease the design and manufacturing problems typically inherent in switching power supplies and, at the same time, provide greater repeatability and reliability at significantly reduced costs.

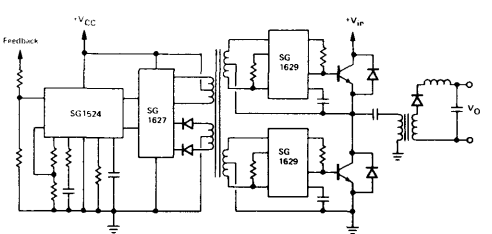


FIGURE 22 – THREE IC TYPES FORM A MAJOR PORTION OF THE CONTROL ELECTRONICS FOR A SWITCH-MODE HALF-BRIDGE CONVERTER.

Use motor-drive IC to solve tricky design problems

An IC driver's logic-control features and high output capability suggest elegant ways to handle a variety of difficult-to-drive loads.

Jim Williams, Consultant,
and **Stan Dendinger,** Silicon General Corp

You can use the SG3635 driver IC in a wide range of applications, ranging from a switched-mode motor-speed controller to a data-communications line driver. The device's input configuration simplifies interfacing between low-level circuitry (eg, a μP or logic blocks) and the high-power load. And its output stage (see **box,** "Anatomy of a driver IC"), capable of driving 40V, 2A loads with peaks as high as 5A (including reactive loads), provides sinking and sourcing capability as well as commutation diodes.

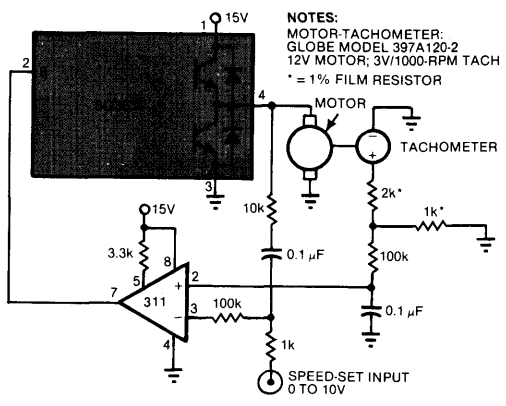


Fig 1—Used in a closed-loop configuration, *the SG3635 self-clocking driver IC controls motor speed in proportion to 0 to 10V input. The comparator weighs the tachometer's output against the input setting, then commands the SG3635 to either speed up or slow down the motor.*

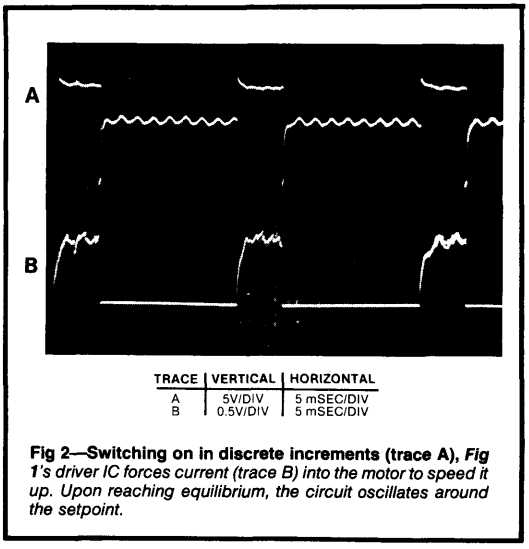


Fig 2—Switching on in discrete increments (trace A), *Fig 1's driver IC forces current (trace B) into the motor to speed it up. Upon reaching equilibrium, the circuit oscillates around the setpoint.*

Fig 1 shows one application of the device in a self-clocking switched-mode speed-control loop. The mechanically coupled tachometer detects the motor's speed; its output, scaled and filtered by the RC network, drives the 311 comparator, which compares the output with the speed-setting input and biases the SG3635 to complete the loop.

When the motor slows down, the SG3635's output switches on (**Fig 2,** trace A), forcing current into the motor (trace B) until the comparator's inputs balance. Under these conditions, the circuit oscillates in a controlled manner around the setpoint. The 10-kΩ, 0.1-μF pair provides positive ac feedback to ensure clean transitions.

Control motor speed with minimum parts count

The 3.3-kΩ resistor from the comparator's offset pin to the 15V supply provides enough offset to prevent motor turn-on with a 0V speed setting. In this application the driver only sources current: The sink transistor is never enabled. You could turn the sink device on to dynamically brake the motor, but the motor's back EMF would cause considerable power dissipation. The back EMF appears after the initial inductive spike (clamped by the internal commutation diode), which appears when the IC's output switches LOW.

What about motor-reversing capability? **Fig 3**'s single-supply circuit uses two SG3635s in a bridge configuration. The flip flop generates the necessary complementary instructions to the ICs' Enable inputs. In this example, the SG3635s' Pulse inputs are grounded; you could instead pulse-width-modulate

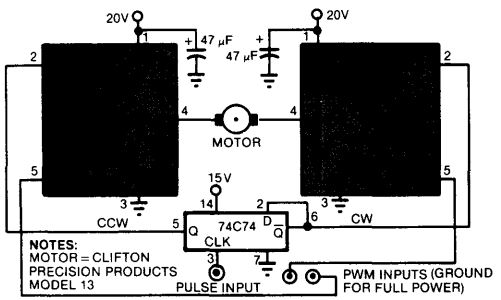


Fig 3—This push/pull bridge configuration *allows two driver ICs to provide bidirectional motor drive. A command to the flip flop's clock input causes instantaneous reversal. Ground the SG3635's Pulse inputs for full speed; apply a pulse-width-modulated input to control the speed.*

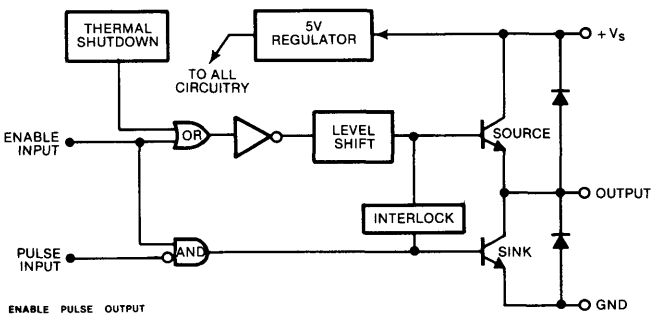
Anatomy of a driver IC

The nearby **figure (a)** shows the SG3635 driver IC's internal organization. The main consideration in the IC's design is to make logic-level/power-load interfacing as straightforward as possible. The logic-compatible Enable and Pulse inputs operate according to the truth table shown: Accepting drive from 74C Series circuits operating at 10V or more, they're compatible with all TTL forms except 54L. You can allow the inputs to float to the HIGH state, but you must force them to ground to produce a ZERO.

Negative supply voltages are permissible at the ground pin, but you must restrict the chip's total rail-to-rail voltage to 40V. The internal regulator stabilizes the IC against supply variations; the level-shift and interlock features provide proper drive levels and prevent simultaneous output-device conduction. The output sinks or sources 2A continuously (5A pk) with ±40V output swing; the commutating diodes handle 5A pk. Finally, the thermal-shutdown circuit disables the upper output device if chip temperature exceeds 160°C.

Why the interlock circuitry? It's important to prevent simultaneous conduction of a source/sink pair's devices **(b)**. This condition usually arises during switching, when the respective devices are interchanging OFF and ON states. During this interval, substantial

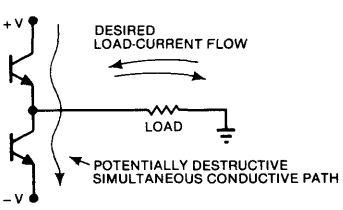
(a)



ENABLE	PULSE	OUTPUT
1	1	OFF
0	1	HIGH
1	0	LOW
0	0	HIGH

Providing logic-to-power-drive translation, *the SG3635* **(a)** *contains both low- and high-level circuitry. The interlock circuit—an important feature—allows only one power device to conduct at a time, thus avoiding transitional power-supply short circuits* **(b)**. *An IC without the interlock can produce large current pulses* **(c)** *during switching. A test circuit* **(d)** *verifies the IC's interlock circuitry;* **(e)** *shows no common current flows in the output devices during switching.*

(b)



IC's high-current output yields fast motor reversal

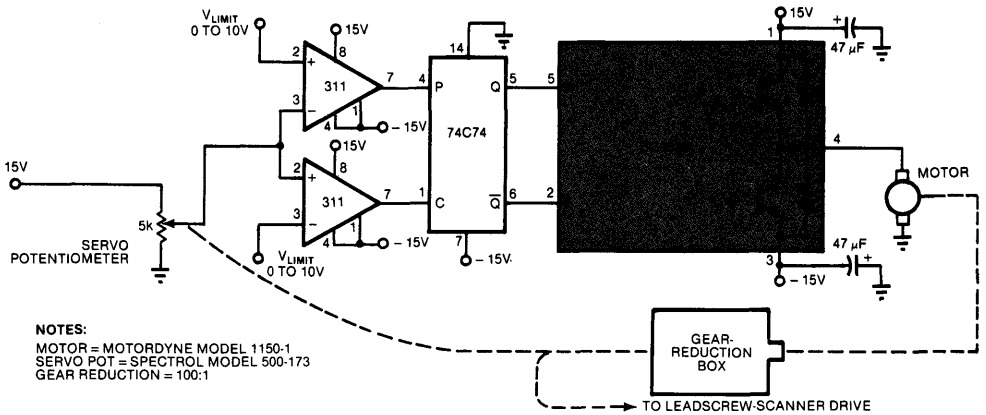


Fig 5—Control a shaft's angular position *with this servo-loop circuit. Select the position by applying limits to the comparator inputs. The circuit uses supplies shifted 15V negative to provide a ground-level bipolar output to the motor.*

a mechanical scanner in either direction between a set of programmed limits. The driver IC's ground pin is biased at −15V, allowing the device's output to swing symmetrically about 0V.

The 5-kΩ pickoff potentiometer detects the scanner's position, then trips a pair of limit comparators; these comparators in turn bias the RS flip flop that controls the SG3635. To provide logic-level compatibility with the driver, the flip flop uses 0 and −15 supplies instead of the usual +15 and 0V configuration. This circuit forces the scanner to run continuously between the limits defined by the V_{LIMIT} inputs. You could control speed by summing pulse-width-modulated signals at the comparator inputs or by gating the SG3635's inputs.

Tackle nonmotor drive problems, too

You can also use the driver IC in applications other than motor control. Consider, for example, the problem of driving long cables at high data rates—a difficult task because of the rapid buildup of parasitic capacitance

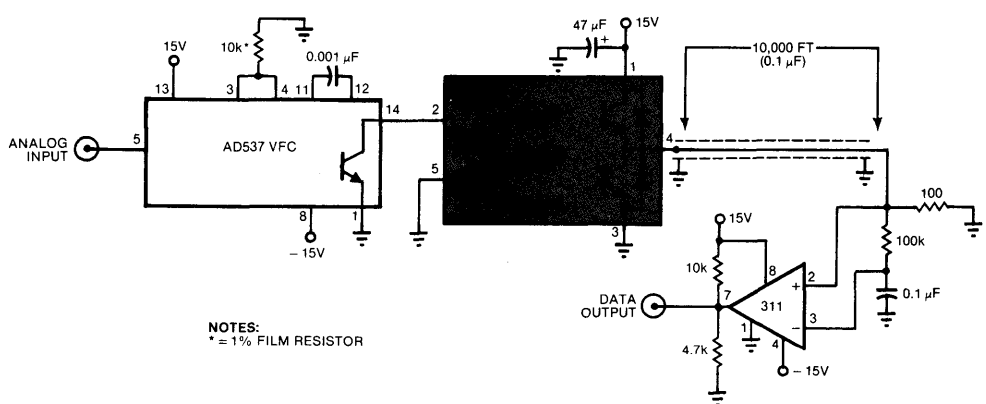


Fig 6—Driving a brutal capacitive load *presents little problem to the SG3635 driver. In this circuit, the IC drives a 10,000-ft data-communications cable having 0.1-μF capacitance. The driver transmits serial 100-kHz data to the receiving comparator.*

Drive long cables with total data recovery

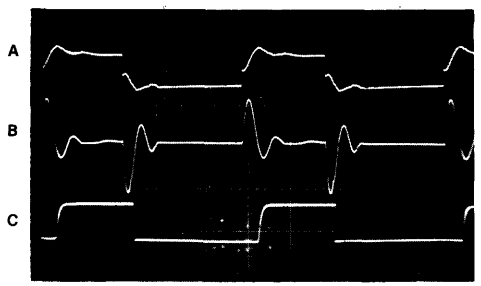
with increasing cable length. In a remote data-monitoring application, for instance, a 10,000-ft cable displays 0.1-μF capacitance—a brutal load at high speed, making receiver-end data recovery difficult.

Fig 6's circuit provides the drive for this difficult load: The V/F converter presents a serial, 100-kHz square-wave data format to the SG3635. The driver's output (**Fig 7**, trace A)—somewhat distorted because of the load—drives the line. Trace B shows the IC's output current: The 5A peaks at the waveform's edges clearly reflect the heavy capacitance.

The square wave's distortion is relatively minor, allowing easy data recovery. The 311 comparator uses a simple RC network to set an adaptive amplitude threshold against which to compare the line output. Because the threshold is derived from the signal, power-supply shifts produce no undesirable effects.

In another nonmotor-related application, you can use the SG3635 in conjunction with a pH probe as a 3-mode controller (**Fig 8**). The FET op amp unloads the probe and routes the signal—via an RC filter—to the two comparators. The comparators, configured as a double-ended limit detector, bias the SG3635; the IC then drives valves that feed either acidic or basic solutions to the chemical vessel.

If pH is correct, both comparator's outputs remain HIGH and neither valve energizes: The appropriate LOW-switching comparator redresses eventual pH imbalance by turning the necessary valve on.



TRACE	VERTICAL	HORIZONTAL
A	20V/DIV	2 μSEC/DIV
B	4A/DIV	2 μSEC/DIV
C	5V/DIV	2 μSEC/DIV

Fig 7—The effects of Fig 6's gluttonous capacitive load *are evident in traces A and B. The 10,000-ft line absorbs 5A current peaks during the IC's switching transitions. The receiving-end comparator uses an adaptive amplitude threshold to produce a clean output.*

In a final example of the driver IC's versatility, consider its use as a power-transistor driver. Driving these devices at high speed requires active turn-off techniques to sweep charges from the base-emitter junction. Moreover, many high-voltage power transistors need negative base bias to guarantee breakdown ratings.

Assume, for example, the use of unipolar base drive

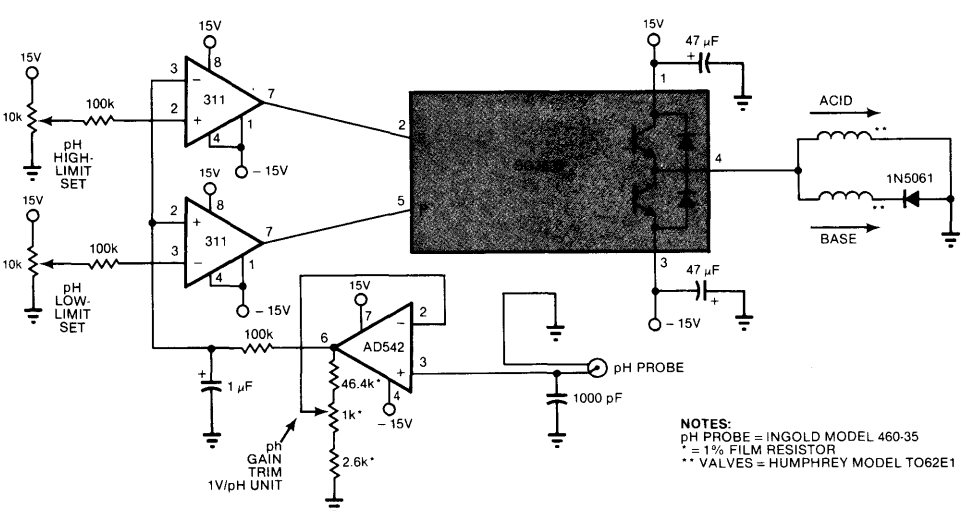
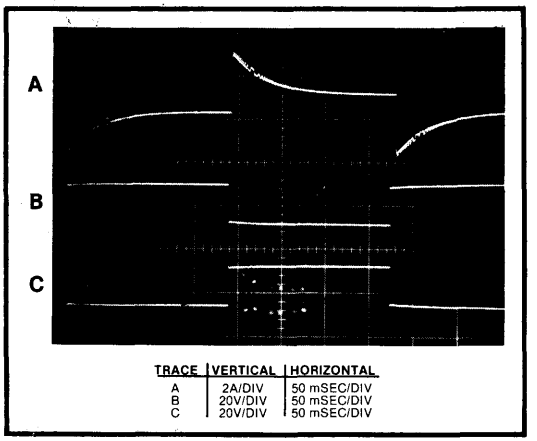


Fig 8—Regulate a chemical solution's acidity *with this 3-mode controller circuit. The SG3635 drives the valves that add either acidic or basic solution to the bath. Set the desired pH with potentiometer-determined comparator limits.*



TRACE	VERTICAL	HORIZONTAL
A	2A/DIV	50 mSEC/DIV
B	20V/DIV	50 mSEC/DIV
C	20V/DIV	50 mSEC/DIV

them to control motor speed.

Fig 3's circuit is a good test of the IC's peak current capabilities, because motors present a very difficult load during instantaneous reversal. **Fig 4,** trace A shows the motor current; traces B and C represent the SG3635's voltage outputs. The motor draws 200 mA in normal mode but requires more than 3A during a reversal because of the armature's stored energy.

Servoed motor makes position clear

In addition to controlling speed and direction, you can use the SG3635 in a simple circuit to control a shaft's position **(Fig 5).** In this configuration, the motor drives

Fig 4—Large peak-reversal current in Fig 3's motor *is evident in trace A. Traces B and C show the drivers' output reversal; the outputs handle the 3A motor peaks cleanly.*

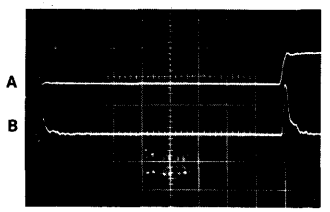
supply current flows through both devices, effectively shorting the supplies. A common approach to alleviating the problem is to make the stage switch quickly, minimizing concurrent ON time.

The widely used 555 timer furnishes this simple solution. However, it still generates considerable supply glitches **(c).** Trace B shows the large supply-current spike the IC's output pair produces when switching (trace A). Such a current spike, in conjunction with a supply bus's impedance, can result in unacceptable system noise or device destruction.

The SG3635's interlock circuitry ensures complete turn-off of one output device before the other begins to turn on. This provision eliminates supply shorts during switching, even when controlling high power. To verify this action, use the **figure**'s test circuit **(d).** Part **(e),** trace A shows one phase (Q) of the 74C74's output; trace B depicts the driver's output.

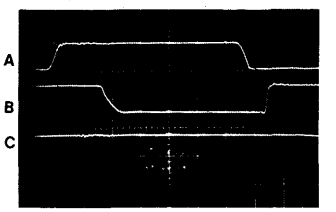
When Q switches LOW, the SG3635 unclamps its sink transistor, then allows the source device to turn on. The reverse holds true when Q switches HIGH. These intentional turn-on delays account for the 200-nsec output-timing skew. Note in trace C—the ground-pin-current—that no current ever flows directly through the source/sink pair.

(c)



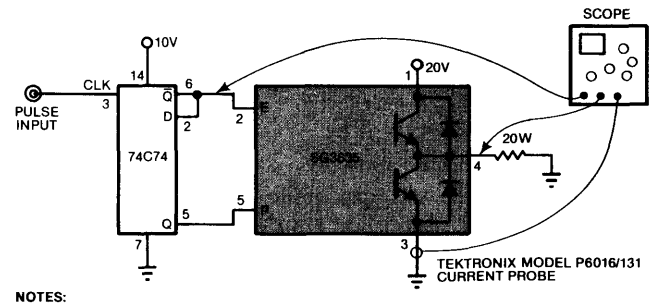
TRACE	VERTICAL	HORIZONTAL
A	20V/DIV	200 nSEC/DIV
B	500 mA/DIV	200 nSEC/DIV

(e)



TRACE	VERTICAL	HORIZONTAL
A	10V/DIV	200 nSEC/DIV
B	20V/DIV	200 nSEC/DIV
C	100 mA/DIV	200 nSEC/DIV

(d)



NOTES:
RETURN SG3635 LOAD AND GROUND-PIN LEADS SEPARATELY TO SUPPLY

Valve-control circuit maintains constant pH

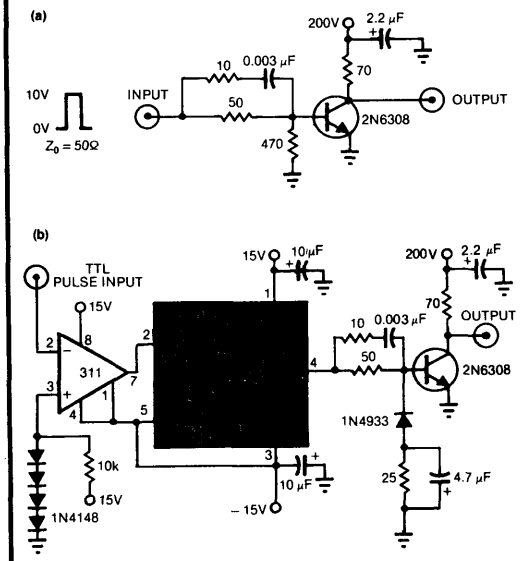
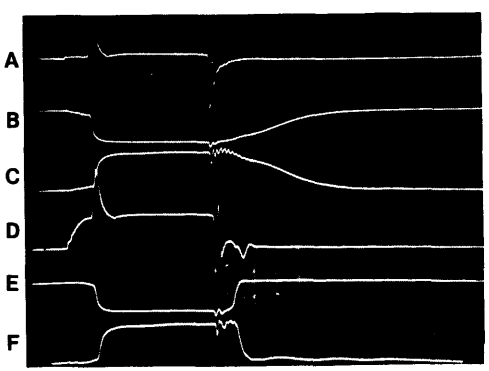


Fig 9—Using unipolar base drive (a) *for a high-power transistor can result in slow collector turn-off. A bipolar-drive circuit* **(b)** *shortens turn-off time considerably by sweeping out base-emitter charge. Moreover, the negative base bias improves the transistor's breakdown characteristics.*



TRACE	VERTICAL	HORIZONTAL
A	5V/DIV	500 nSEC/DIV
B	200V/DIV	500 nSEC/DIV
C	3A/DIV	500 nSEC/DIV
D	5V/DIV	500 nSEC/DIV
E	200V/DIV	500 nSEC/DIV
F	3A/DIV	500 nSEC/DIV

Fig 10—Dramatic turn-off-time differences *between unipolar- and bipolar-base-drive circuits* **(Figs 9a** *and* **9b)** *are evident in this photo. Long collector-voltage (trace B) and -current (trace C) ON-to-OFF transitions result from the unipolar drive (trace A); the bipolar drive (trace D) increases turn-off speed more than sevenfold.*

(Fig 9a) for a high-power 2N6308. **Fig 10,** trace A shows the transistor's base waveform; traces B and C display collector voltage and current, respectively. Because the base drive is unipolar, the collector turns off slowly: Voltage and current require about 1.5 μsec to settle. What's more, the transistor dissipates considerable power during turnoff, increasing its vulnerability to secondary breakdown. Inductive loads (eg, flyback transformers) can exacerbate the situation.

The solution? **Fig 9b**'s circuit uses an SG3635 to provide bipolar base drive, thereby shortening turn-off time. The 311 comparator shifts the TTL-command level to bias the driver's Enable input; shifting is necessary because the SG3635's ground pin is returned to −15V. The 25Ω resistor to ground limits the transistor's reverse bias. Traces D, E and F show the 2N6308's base voltage and collector voltage and current, respectively—you can see that collector turn-off time decreases to 200 nsec, greatly reducing the likelihood of secondary breakdown.

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SIMPLIFIED HIGH-EFFICIENCY MOTOR DRIVE SYSTEMS WITH NEW PWM INTEGRATED CIRCUITS

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ABSTRACT

This paper describes a new pulse width modulator circuit designed specifically for DC motor control. It provides a bi-directional pulse train output in response to the magnitude and polarity of an analog error signal input. The device is useful as the control element in motor-driven servo systems for precision positioning and speed control, as well as in audio modulators and amplifiers using carrier frequencies to 350 kHz.

1. INTRODUCTION

Power management engineers have been aware for a number of years of the efficiency advantages of switching power supplies over linear designs. In response to growing production of switchers, the semiconductor industry has spawned a number of pulse width modulator (PWM) integrated circuits of varying degrees of complexity for the control of these power supplies.

Perceptive designers soon realized that the same efficiency advantages apply to motor control. Unfortunately, when they attempted to utilize existing PWM circuits, they found that the architecture was not optimized for motor control. So many auxiliary components had to be added to work around the restrictions of the PWM circuit that totally discrete designs were frequently found to be more economical.

The main difficulty has been that PWM controllers for switching power supplies were designed to be one quadrant power conditioners; i.e., the polarity of DC output voltage is fixed and proportional to a unipolar reference voltage. A second difficulty has been that power supply controllers attempt to produce an AC waveform of variable energy content, since power must be transferred through a high frequency transformer. This requires that PWM pulses alternate from side to side with a dual-driver architecture.

The requirements for PWM motor control are different: The integrated pulse train must have a DC component proportional to the magnitude of the applied reference voltage, and a polarity determined by the sign of the reference to accomplish bi-directional rotation. All of the necessary control elements for two quadrant operation are found in the PWM circuit to be described, which is designated the SG1731.

2. BLOCK DIAGRAM

The SG1731 contains a triangle waveform oscillator, a wideband operational amplifier for error voltage generation, a summing/scaling

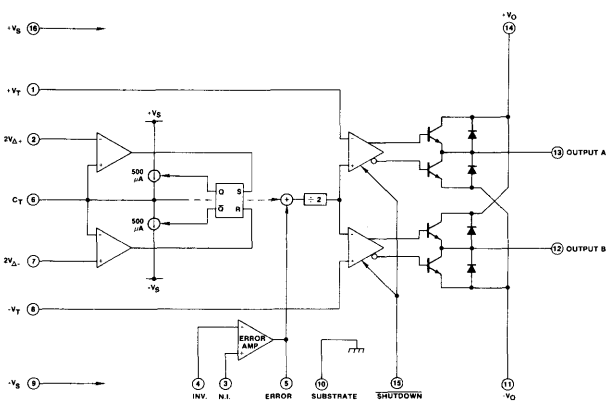


FIGURE 1. SG1731 BLOCK DIAGRAM

network for level-shifting the oscillator waveform, externally-programmable PWM comparators, and dual ±100mA, ±32 volt totem pole drivers with commutation diodes for full bridge output drive. A TTL-compatible SHUTDOWN terminal forces the output drivers into a floating high-impedance state when driven LOW. Supply voltage to the circuit may be either from dual positive and negative supplies, or single-ended.

3. PULSE WIDTH MODULATION

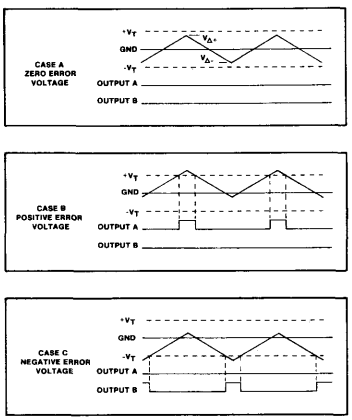


FIGURE 2. DEADBAND OPERATION

Pulse width modulation occurs by adding an error voltage to the triangle waveform, attenuating the resulting signal by a factor of 2, and comparing it to threshold voltages $+V_T$ and $-V_T$, which are applied to pins 1 and 8 respectively. Figure 2 illustrates the case for $V_{\Delta+} < +V_T$. When the error voltage is zero, no threshold crossings occur, and the output drivers remain in the LOW state. If the error voltage is sufficiently positive, the upper threshold will be periodically crossed by the shifted triangle waveform and output driver A will switch to the HIGH state. As the error voltage becomes larger, the duty cycle of driver A will linearly increase towards 100%. The same action occurs at output driver B for negative error voltages.

A motor connected across the full bridge formed by drivers A and B will receive a high frequency pulse train which, when integrated by the LR time constant of the armature, will result in a voltage drive proportional to the magnitude of the error signal. The polarity of the drive signal will be the same as the polarity of the error voltage.

With deadband operation, there is a small region around the null point of the servo loop where no power is applied to the motor. This conserves power, which may be desirable in some applications, but it also results in loss of both positioning accuracy and mechanical stiffness.

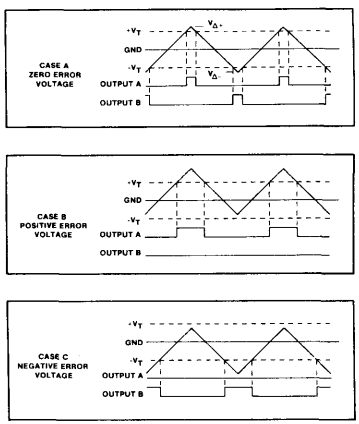


FIGURE 3. NON-DEADBAND OPERATION

The other possible mode of operation is shown in Figure 3, where $V_{\Delta+} > +V_T$. At the loop null point the motor still receives drive pulses, which provides resistance to armature movement by external forces. The integrated drive voltage is still zero when the error voltage is zero, since the drive pulses alternate in polarity with identical pulse widths at the null point.

This is the preferred mode of control in a missile fin actuator system where aerodynamic forces on the airfoil attempt to move the motor armature away from the null position. A second example where deadband operation is not desirable is a switching, or "Class D", audio amplifier. Cross-over distortion would be unacceptable, and poor speaker damping would also result.

4. OSCILLATOR CIRCUIT

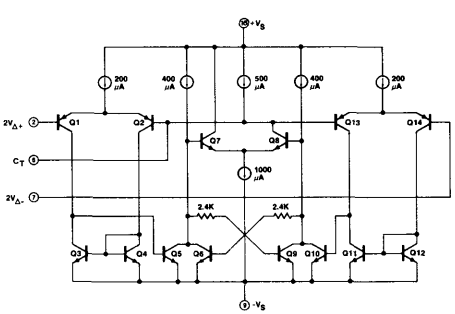


FIGURE 4. SG1731 OSCILLATOR SCHEMATIC

The triangle oscillator consists of two voltage comparators, a set/reset flip-flop, a bi-directional 500 μA current source, and an external timing capacitor C_T. A positive reference voltage applied to pin 2 ($2V_{\Delta+}$) sets the peak value of the triangle, and a negative reference voltage at pin 7 ($2V_{\Delta-}$) determines the valley of the triangle. Normally, the reference voltages are equal, so that a symmetrical waveform about ground results.

Circuit operation is as follows: Transistors Q6 and Q9 form the set/reset flip-flop. Assume that Q9 is conducting and Q6 is off. The collector voltage of Q9 will be low compared to that of Q6, resulting in Q7 conducting and Q8 being off. The current from the 500 μA source will flow into C_T and a positive voltage ramp will occur at pin 6. When the voltage exceeds $2V_{\Delta+}$, the comparator formed by Q1 through Q4 changes state, turning on Q5. This removes base drive from Q9 and the flip-flop will change state. The current-steering transistor pair Q7 and Q8 now switch the 1 mA discharge current source onto the C_T bus. Since the 500 μA charging source is still active, the net discharge current out of C_T is the difference of the two sources, or 500 μA. Since monolithic construction allows close ratioing of current sources, the discharge rate will closely match the charge rate. When the voltage on C_T falls below $2V_{\Delta-}$, the comparator formed by Q11 through Q14 will reset the flip-flop and another charge cycle will begin.

Since the values of the current sources are fixed at a nominal 500 μA, the oscillator frequency may be calculated as follows:

For a given capacitance and current,

$$\frac{dV}{dt} = \frac{I}{C} \qquad (1)$$

or

$$dt = \frac{C}{I}\, dV \qquad (2)$$

where

$dV = V_{OSC}$ peak-to-peak
$I = 500\ \mu A = 5 \times 10^{-4}$ A
$dt = \frac{1}{2} T_{OSC}$ (assuming symmetry)
C = Variable

Therefore

$$T_{OSC} = 2dt = \frac{2CdV}{5 \times 10^{-4}} \qquad (3)$$

The desired oscillator frequency can be obtained by first choosing a peak-to-peak voltage for the triangle waveform, and then selecting the proper value of C_T from Equation 3.

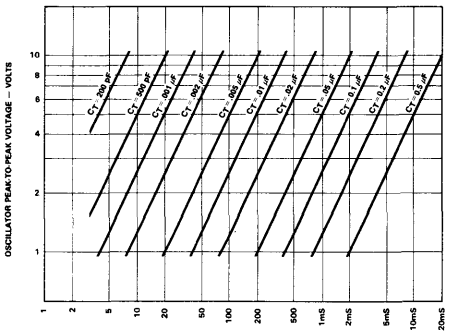


FIGURE 5. SG1731 OSCILLATOR PERIOD VS. V_{OSC} AND C_T

As a design aid, the solutions to Equation 3 over the recommended range of T_{OSC} and V_{OSC} are presented in graphical form in Figure 5. The lower limit on T_{OSC} is 2.85 μsec, corresponding to a maximum frequency of 350 kHz. The maximum value of V_{OSC}, $(2V_{\Delta+})-(2V_{\Delta-})$, is 10 volts peak-to-peak for linear waveforms.

5. ERROR AMPLIFIER

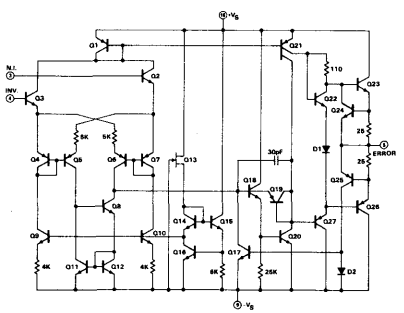


FIGURE 6. SG1731 ERROR AMP SCHEMATIC

The error amplifier is a high slew rate unit designed for low input offset voltage and bias current under equilibrium conditions. It consists of two gain sections, with frequency compensation for unity closed-loop gain stability in the second stage. The first stage is formed by transistors Q1 through Q12. When the differential input voltage is zero, the emitter voltages of Q2 and Q3 are equal, and the collector currents of Q5 and Q6 are equal to a small fraction of the collector current in Q4 and Q7. The value of current is set by current sources Q9 and Q10 and the two 5K emitter resistors. Transistors Q8, Q11 and Q12 form a compound current mirror which converts the full differential voltage gain of the input stage into a single-ended gain referred to $-V_S$. A Darlington gain stage formed by Q18 and Q20 provides the large voltage swing required for the amplifier output. When the differential input

voltage is not zero, that voltage appears across the 5K resistors of the input stage, increasing the operating current. Simultaneously this increased current is sensed by Q1, and current supply to the output stage is increased proportionally. Since more current is available to charge the 30 pF compensation capacitor, the amplifier output voltage slews at a much higher rate. When equilibrium is again reached, the bias currents return to their normal quiescent levels.

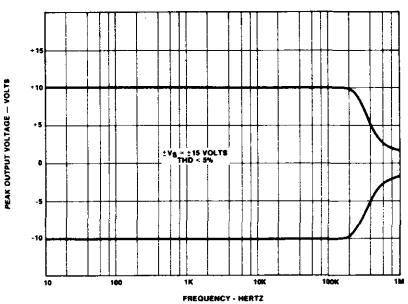


FIGURE 7. ERROR AMP POWER BANDWIDTH

As shown in Figure 7, the error amplifier is capable of excellent power bandwidth. Full output swing to 200 kHz is available, with slew rates exceeding 15 volts/microsecond. These dynamic characteristics allow application to audio modulation circuits with very low transient distortion.

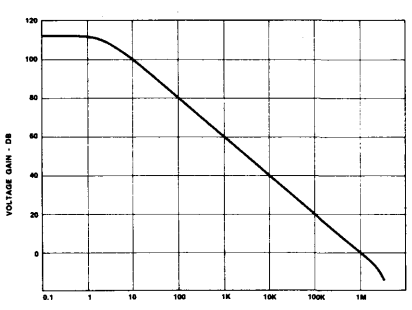


FIGURE 8. ERROR AMP OPEN-LOOP FREQUENCY RESPONSE

The amplifier frequency-gain plot is a constant 6 dB/octave roll-off to unity gain, resulting both in unity gain stability and good transient response. Typical DC voltage gain is 110 dB into a 2K load, and unity gain crossover frequency is 1 megahertz.

6. OUTPUT DRIVERS

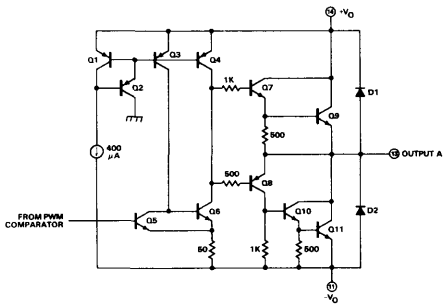


FIGURE 9. HALF-BRIDGE OUTPUT DRIVER SCHEMATIC

The output stage is a non-saturating quasi-complementary high current switch for efficient high frequency operation. Transistors Q3, Q4, Q5 and Q6 form a high voltage Schmitt trigger input stage. The positive feedback produces fast switching times and jitter-free pulse width modulation. Q7 and Q9 provide output current sourcing, and Q8, Q10 and Q11 provide current sinking. Commutation diodes D1 and D2 clamp inductive loads to the supply rails. Their current capability is the same as the output transistors: 200 mA peak.

7. TYPICAL APPLICATIONS

7.1 SIMPLE POSITION SERVO

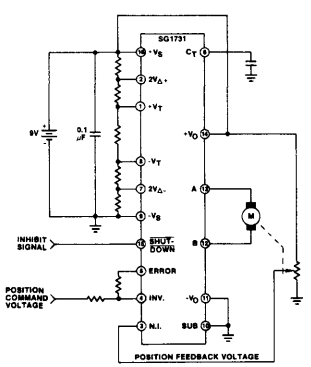


FIGURE 10. A SIMPLE BATTERY-POWERED POSITION SERVO

A simple, low-voltage, battery-powered position servo is illustrated in Figure 10. A resistive divider network sets up the reference voltages for triangle waveform amplitude and PWM thresholds. Since the circuit is powered by battery, $V_{\Delta+}$ is designed to be less than $+V_T$ (deadband) to conserve power. The 9 volt DC motor is driven directly from the output drivers, and it in turn drives a position feedback potentiometer through a geartrain. The position feedback voltage is subtracted from the

external position command voltage in the on-chip error amplifier. The difference between commanded position and actual position generates an error voltage which in turn generates a series of PWM pulses to the motor to correct the difference. Once null has been reached, no further power is applied to the motor until a new position command voltage is received, or the wiper is moved out of position by external forces.

7.2 HIGH TORQUE POSITION SERVO

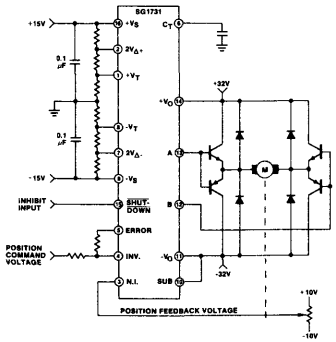


FIGURE 11. HIGH TORQUE POSITION SERVO

Figure 11 illustrates a high power version of the previous position servo loop. The control circuit is powered from balanced positive and negative supply voltages, and the output drivers switch the load between ±32 volt supply rails for maximum output power. Complementary emitter follower buffers on each output provide increased current gain and power handling capability.

7.3 MOTOR SPEED CONTROL

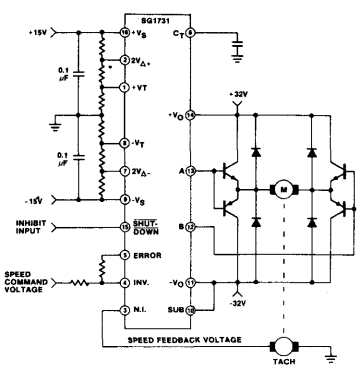


FIGURE 12. HIGH TORQUE BI-DIRECTIONAL MOTOR SPEED CONTROL CIRCUIT

In Figure 12, a bi-directional motor speed control circuit is derived from the previous circuit by substituting a tachometer for the position pot in the motor feedback circuit. The external command voltage now represents a speed rather than a position, with direction of motor rotation a function of command voltage polarity. Magnetic tape drives are an example of this configuration, with the velocity feedback voltage frequently derived from an encoded bit pattern on the tape.

7.4 PWM AUDIO POWER AMPLIFIER

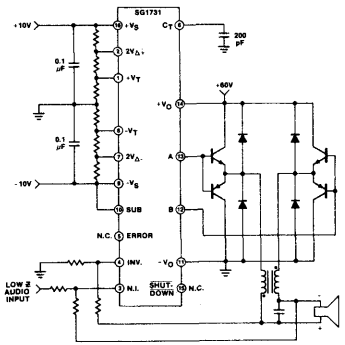


FIGURE 13. P.W.M. AUDIO POWER AMPLIFIER

A complete PWM power audio amplifier is illustrated in this last application. The circuit reconstructs an amplified version of the audio input voltage by deriving the feedback signal from the speaker voice coil. An oscillator frequency of 300 kHz was chosen to maintain a ratio of at least 15 to 1 between the carrier frequency and the highest modulation frequency (20 kHz).

Ratios of at least 10 to 1 are necessary for acceptable linearity, low distortion and good transient response. An LC output filter smoothes the pulse width modulated output to the speaker; its design is critical for low distortion. This circuit, consisting of one integrated circuit and four power transistors, can deliver 150 watts RMS of power into a 4 ohm load.

8. CONCLUSION

A new pulse width modulator integrated circuit designed for motor control has been described which includes all the circuitry necessary for implementing high efficiency bi-directional controllers. Inputs and outputs have been designed for maximum flexibility, allowing the device to be useful in a wide range of position and speed servo systems.

Simplify feedback controllers with a 2-quadrant PWM IC

A 2-quadrant pulse-width-modulator IC eliminates many of the problems arising with unipolar devices in feedback-control applications.

Jim Williams, Consultant,
and **Stan Dendinger,** Silicon General Corp

The SG1731 pulse-width-modulator (PWM) IC brings to motor controllers and similar applications the efficiency previously limited to switching-power-supply circuitry. As a result, you can use it to design motor-controller circuits having parts counts smaller than previously achievable.

Switching-power-supply PWM controllers are designed to be 1-quadrant power conditioners, furnishing a dc output voltage with fixed polarity and amplitude proportional to a unipolar reference voltage. Motor controllers, on the other hand, require an integrated pulse train with a dc component proportional to the magnitude of an applied reference voltage and polarity determined by the reference's sign. Otherwise, they can't produce bidirectional rotation.

In addition, the architecture of power-supply PWM ICs often proves inappropriate for motor-control tasks, requiring so many auxiliary circuits that totally discrete designs often prove more economical. PWM

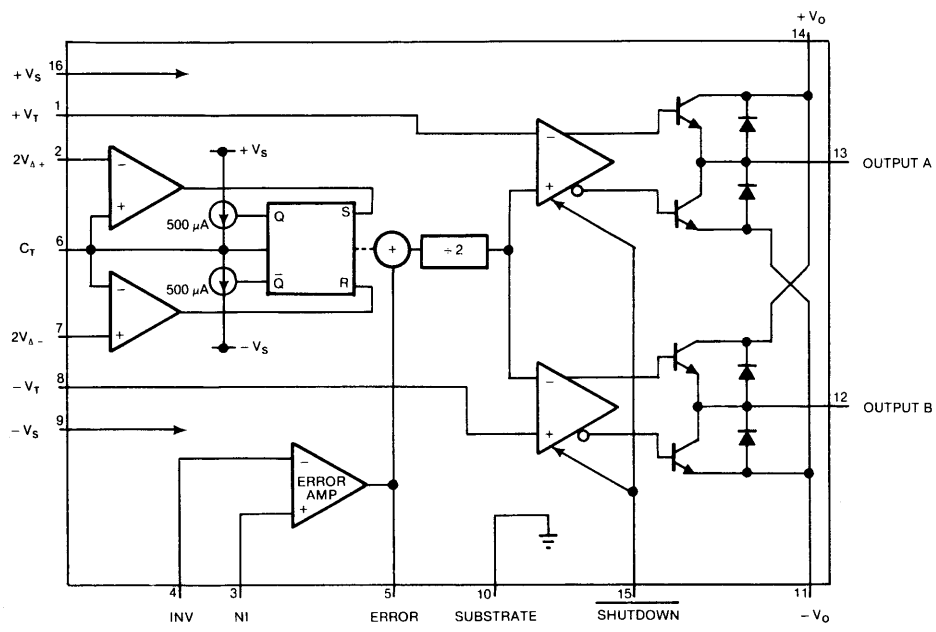


Fig 1—A dc-motor pulse-width-modulator IC, *the SG1731 features 50-Hz to 350-kHz oscillator range, adjustable deadband operation, a high-slew-rate error amplifier, a Shutdown input providing floating outputs, and dual 100-mA source/sink output drivers capable of operating from supplies to ±32V.*

Error voltage controls pulse-width modulation

power-supply controllers attempt to produce a variable-energy-content ac waveform, because power must be transferred via a high-frequency transformer. Unlike those from a PWM motor-control IC, the PWM pulses produced by these devices must alternate and are therefore produced by a dual-driver architecture.

Fig 1 shows the SG1731's structure. The device contains a triangle-waveform oscillator whose frequency is determined by an external capacitance at pin 6 and whose amplitude can be set through resistor or voltage programming at pins 2 and 7. The IC also contains a wide-band op amp for error-voltage generation, a summing/scaling network for level-shifting the oscillator waveform, externally programmable PWM comparators and dual ±100-mA continuous (±200-mA pk), ±32V totem-pole drivers with commutation diodes for full-bridge output drive. Typical supply voltages are ±15V, although the device can function at values as low as ±3.5V. You can use dual- or single-polarity supply voltages. Pin 15, the $\overline{\text{Shutdown}}$ terminal, forces the output drivers into high-impedance states when LOW.

Pulse-width modulation occurs when an error voltage gets added to the triangle waveform, attenuating the resulting signal by a factor of two and comparing it with threshold voltages $+V_T$ and $-V_T$ (pins 1 and 8). **Fig 2** illustrates the case for $V_\Delta < V_T$. When the error is 0V, no threshold crossings occur, and the output drivers remain at $-V_0$ **(Fig 2a).** As the error voltage goes positive, the upper threshold gets periodically crossed by the shifted waveform, and output driver A switches to $+V_0$ **(Fig 2b).** As the error voltage becomes larger, the duty cycle of driver A increases linearly toward 100%. The same action occurs at output B **(Fig 2c)** for negative error voltages.

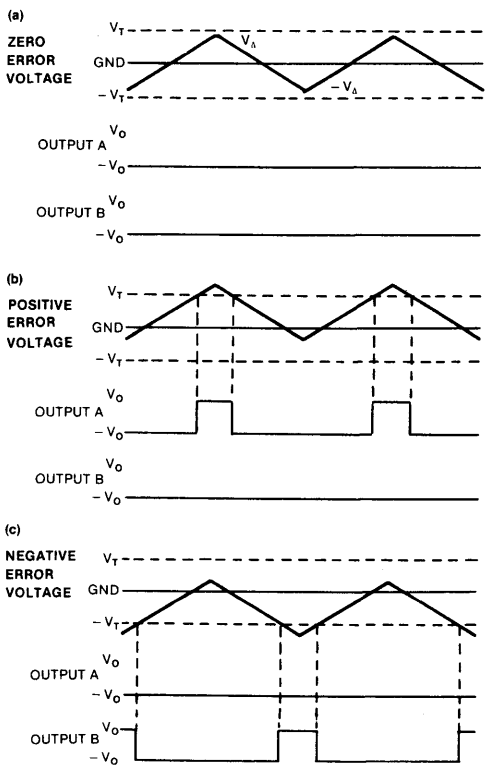


Fig 2—With oscillator voltage less than threshold voltage, *the SG1731's outputs switch LOW to HIGH when the error voltage shifts oscillator output outside the threshold.*

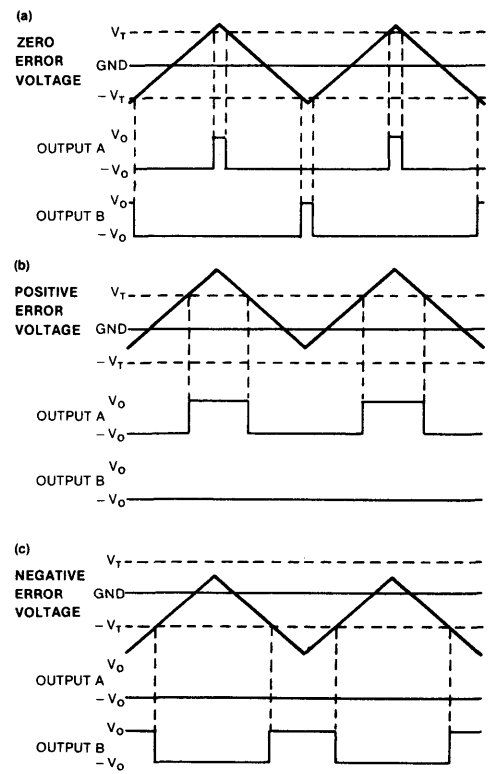


Fig 3—With oscillator voltage greater than threshold voltage *in the 1731, lack of a deadband provides resistance to motor movement caused by external forces.*

Class D amplifiers for audio applications

Almost all amplifiers use some form of output pass element to deliver power to a load. Because the amplifier controls this pass element, and because the amount of power delivered to the load varies, dissipation is inevitable. And at high power, substantial dissipation losses place limits on packaging, power consumption and efficiency.

One form of amplifier, the Class D stage, largely circumvents these problems by using a switched-mode output stage to deliver power to the load. Because the amplifier's output is either ON or OFF, efficiency is higher than that of a linear stage, and heat dissipation is low. In **Fig A,** the output of such a stage is represented by a series of width-modulated pulses whose power-time spectrum is related to the input signal.

In theory, this type of stage can serve in an efficient audio amplifier. And recently, designers have expressed a great deal of interest in developing such an amplifier. However, practical problems have made a workable switching design for audio difficult to achieve.

Historically, switched-mode-amplifier designs called for complex circuitry and expensive output devices. Producing a pulse-width modulator that provides 2-quadrant response with high linearity and wide bandwidth was difficult. In addition, even if available, low-loss output switches that operated at high carrier frequencies were expensive, and the drive circuitry quite complex.

The introduction of power-FET devices has reduced design-cost and complexity problems in the output stage. But although such components make the job easier, designers still must deal with several issues to achieve optimum performance.

One unpleasant surprise is the combination of the high-frequency

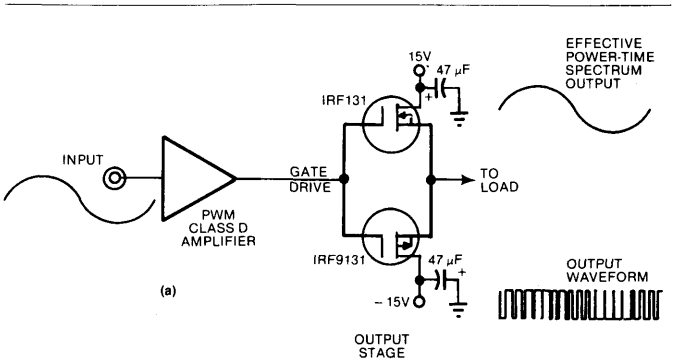
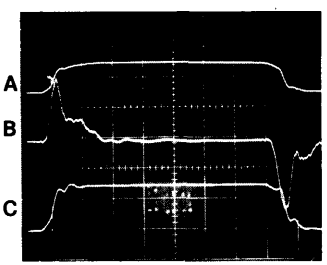


Fig A—A switched-mode PWM Class D amplifier *coupled to an FET output stage provides efficient operation.*

carrier and the FETs' input capacitance. The FET gate drive (**Fig B,** trace A) causes the current drawn through the input capacitances (trace B) to peak at 400 mA on both edges as the FETs switch. Although the FETs have a high impedance at dc, the high carrier frequency required for audio calls for substantial average gate current. This requirement in turn calls for some form of preceding driver.

A more serious problem centers on filtering the carrier at the load (a speaker in audio applications). Filter design is complicated by the uncertain characteristics of the lead wire and speaker that connect to the amplifier. Even if these parameters are fixed by specification, the speaker's reactive nature complicates the design.

Even assuming the filter can be built, the waveform across the speaker is well out of the phase with the input because of carrier-induced phase shift as well as filter phase shift. As a result, closing a feedback loop from the load proves difficult. It might be possible to use a complementary phase-shift network to correct for this shortcoming, but the design of this type of an audio-grade compensation scheme is difficult. Without feedback, the problem goes away, but nonlinearities in



TRACE	VERTICAL	HORIZONTAL
A	50V/DIV	200 nSEC/DIV
B	200 mA/DIV	200 nSEC/DIV
C	20V/DIV	200 nSEC/DIV

Fig B—Fig A's FET output stage *draws 400-mA pk gate current when the FETs switch (trace B). Trace A is the gate drive signal; trace C, the FETs' source lines.*

the pulse-width modulator then contribute to output distortion.

Finally, the high-frequency harmonics in the switching stage pose a difficult RFI-suppression problem. The same fast switching that yields efficiency and wide-range audio bandwidth also qualifies as a potential broadband radio transmitter and must be suppressed. This need mandates careful layout, expensive and complex packaging and RFI suppression on both power and speaker connections.

No motor power required with deadband operation

A motor connected across the full bridge formed by drivers A and B receives a high-frequency pulse train. When integrated by the armature's L/R time constant, this pulse train results in a voltage drive proportional to the error signal's magnitude. Drive-signal and error-voltage polarities are identical.

With this deadband operation, no motor power gets applied in a small region around the servo loop's null point. Although this action conserves power (desirable in some applications), it results in a loss of both positioning accuracy and mechanical stiffness. Deadband operation is also not desirable in switching (Class D) audio amplifiers. There, crossover distortion is unacceptable, and poor speaker damping results (see **box,** "Class D amplifiers for audio applications").

The other SG1731 mode of operation is shown in **Fig 3,** where $V_\Delta > V_T$. At the loop null point, the motor receives drive pulses that resist externally produced armature movement. The integrated drive voltage is 0V with no error voltage **(Fig 3a)** because the drive pulses alternate in polarity and have identical widths at the null point. **Figs 3b** and **3c** show the effects of error voltages on the oscillator signal.

This is the preferred control mode in a missile-fin-actuator system, for example, where aerodynamic forces on the airfoil attempt to move the motor armature away from the null position.

You can configure the SG1731 as a bidirectional motor-speed controller as shown in **Fig 4.** The motor specified runs directly from the device's outputs, and the tachometer produces an output directly proportional to the motor's speed and direction. This high-level signal gets divided down and filtered by the discrete components associated with the tachometer, then applied to the 1731's error-amplifier input. The 1731 internally compares this signal with the speed-control input's value and provides output drive of the appropriate phase and magnitude, completing a speed-control loop. Set the comparator voltages for nondeadband operation. The lowest rotation speed depends on the motor's friction characteristics.

Instantaneous-direction-reversing applications might require an optional current-limiting circuit rather than ±15V applied directly to pins 11 and 14. At the time of direction reversing, the motor draws peak currents that could damage the 1731's output drivers. Q_1's ability

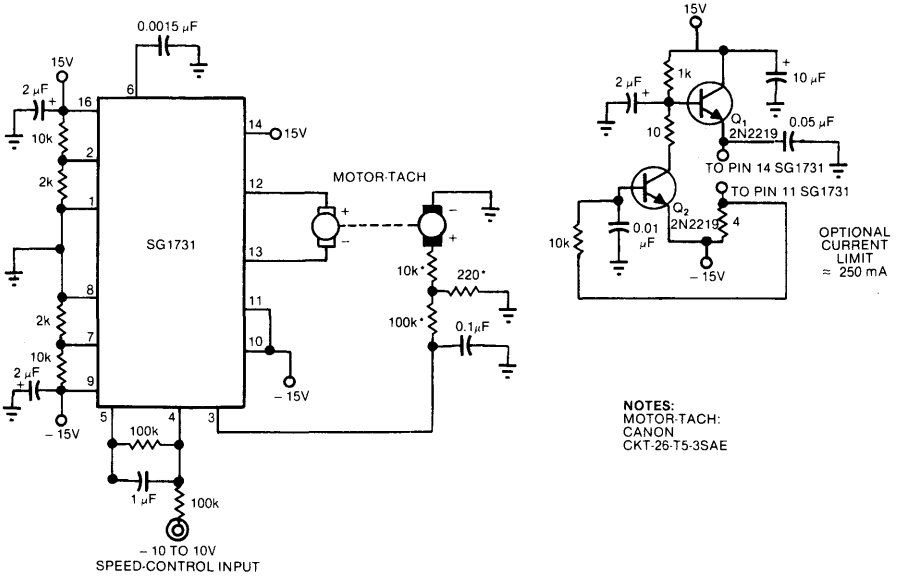


Fig 4—In this bidirectional motor-speed controller, *the tachometer provides feedback while the current-limiting circuit protects the outputs from surge currents.*

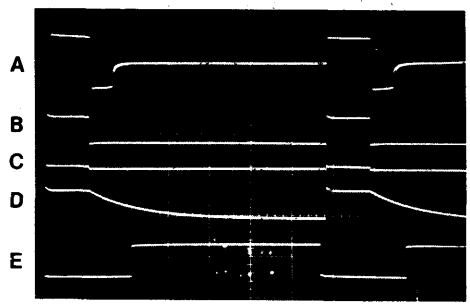
Extend control capability with high-current drivers

to supply current is controlled by Q_2's state, which in turn depends on the voltage across the 4Ω current-sensing resistor. If the motor current exceeds 200 to 250 mA, Q_2 turns on and Q_1 shuts off.

Another bidirectional speed-control loop appears in **Fig 5.** Here, SG1635 drivers control higher motor power and eliminate the need for a speed-monitoring tachometer; instead, back EMF produced by the motor serves as a feedback signal. This arrangement entails some increase in circuit complexity but eliminates the tachometer's cost.

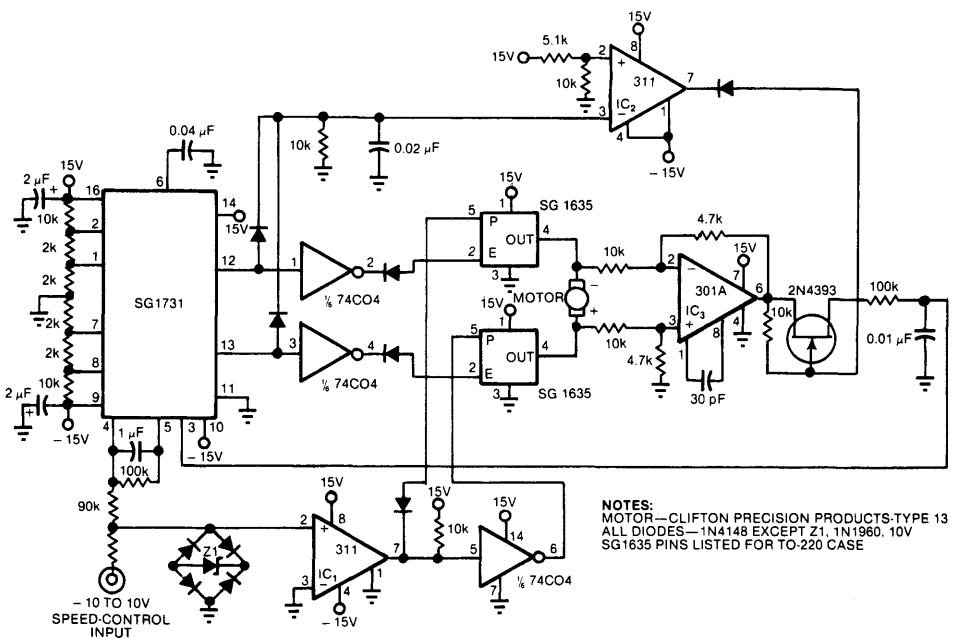
The circuit's basic servo mode is similar to that of **Fig 4.** The 311 comparator (IC_1) senses the polarity of the input command signal. Its output goes to the 1635s via a diode and inverter, allowing both 1635s to be OFF, neither sinking nor sourcing current, when the 1731 is not producing output pulses. **Fig 6** shows the circuit waveforms. When either 1731 output is HIGH, the other output is LOW, and the motor is driven. When both outputs are LOW, the 1635s are OFF and the motor is electrically floating.

The motor's inductive turn-off spike gets damped by the 1635s' internal diodes. After turn-off, the waveform



TRACE	VERTICAL	HORIZONTAL
A	5V/DIV	200 μSEC/DIV
B	20V/DIV	200 μSEC/DIV
C	10V/DIV	200 μSEC/DIV
D	20V/DIV	200 μSEC/DIV
E	20V/DIV	200 μSEC/DIV

Fig 6—Waveforms for Fig 5's tachless controller *include the controller's outputs (traces B and C) and the voltage across the motor (trace A). The 10-kΩ/0.02-μF network's decay time (trace D) ensures that the FET drive (trace E) remains off until after the inductive spike has settled out.*



NOTES:
MOTOR—CLIFTON PRECISION PRODUCTS-TYPE 13
ALL DIODES—1N4148 EXCEPT Z1, 1N1960, 10V
SG1635 PINS LISTED FOR TO-220 CASE

Fig 5—A tachless controller *based on the 1731 uses motor back EMF and some additional parts to reduce overall cost.*

Eliminate servo hunting with long time constants

returns to a dc level determined by the back EMF of the undriven motor, now functioning as a tachometer. This level gets differentially picked off by the 301A op amp (IC_3), whose output feeds a switched synchronous filter. This filter, composed of the FET and the 100-kΩ/0.01-μF combination, samples the back-EMF value during the motor's powered interval.

A 311 (IC_2) gates the FET switch synchronously with the 1731's output. The diode-RC network feeding IC_2 allows either output to actuate the filter. The 10-kΩ/0.02-μF network's decay time length (**Fig 6,** trace D) ensures that the FET drive (trace E) remains OFF until well after the inductive spike has settled out.

The pure dc filter output feeds back to the 1731's error amplifier to complete the speed-control loop. The zener-diode bridge clamps all inputs above approximately ±10V; otherwise the 1731's outputs would saturate at dc and the switched feedback loop would never operate.

Another SG1731 application appears in **Fig 7.** Here, two 1731s bidirectionally control the speed and shaft position of a printed-circuit-type motor.

The shaft position gets sensed at the output of a geardown transmission. Slave the 1731s together to avoid producing frequency beating from separate oscillators; take the triangle waveform of $SG1731_A$ through a 301A follower and use the output to drive the capacitor pin of $SG1731_B$. This is an effective way to slave 1731s together because the follower's low-impedance output overrides whatever state the unbiased internal oscillator of $SG1731_B$ might take. Control the shaft position by sensing it with a potentiometer that feeds a signal back to $SG1731_A$. This signal then gets compared with the Position input, and the outputs of $SG1731_A$ drive the shaft to the position required to balance the error amplifier's inputs.

$SG1731_B$ functions in a speed-control loop similar to that described in **Fig 4.** It controls speed by using its output pins, via a diode OR gate, to pulse-width-modulate $SG1731_A$'s $\overline{\text{Shutdown}}$ pin. The 311 comparator prevents either $SG1731_B$ output from going LOW on a dc basis by synchronously gating signals into the device's output comparators, forcing the appropriate output HIGH.

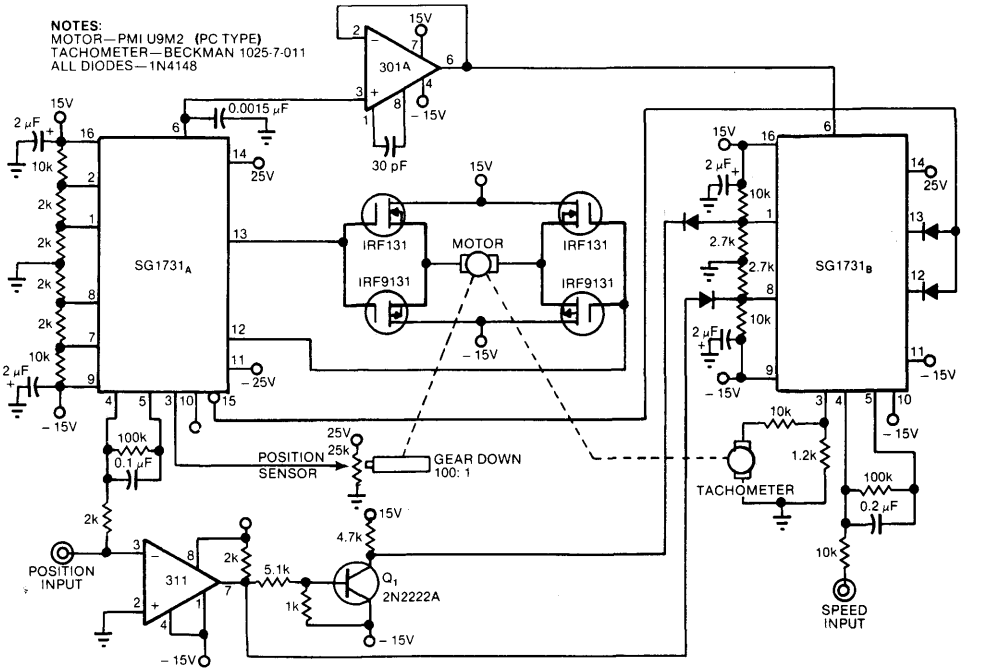


Fig 7—In this bidirectional motor-speed-controller/positioner application, *$SG1731_A$ acts as a position servo, while $SG1731_B$ controls speed.*

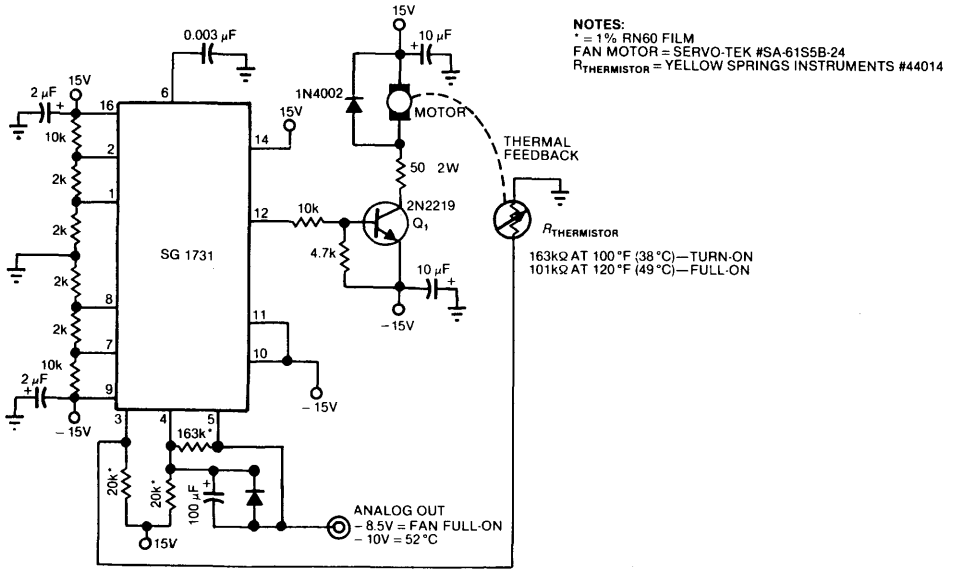


Fig 8—A fan-temperature controller's error-amplifier output *(pin 5) warns of an overtemperature condition.*

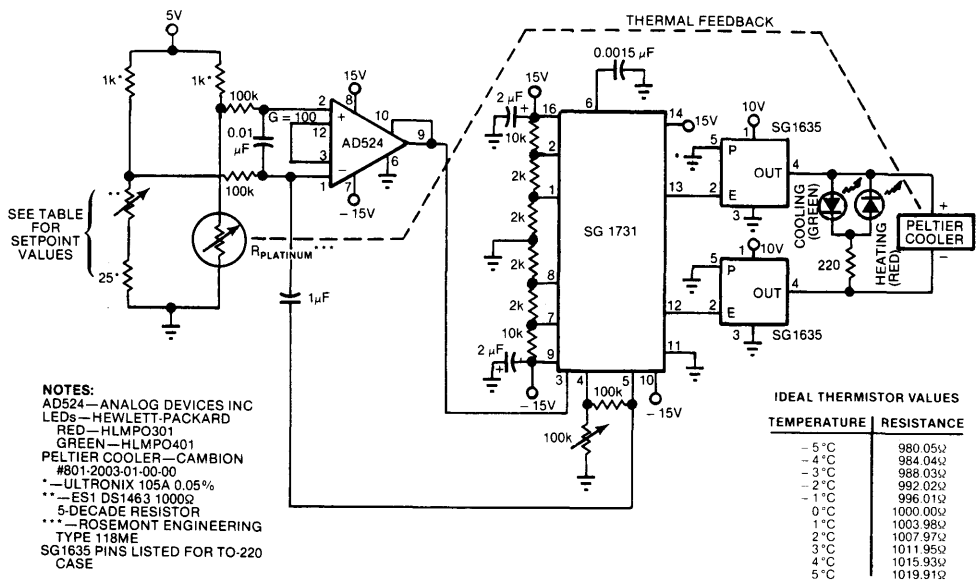


Fig 9—A well-insulated Peltier cooler *with good heat removal on its normally hot side specs stability better than 0.02°C typ.*

Motors adapt easily to Class D operation, speakers don't

Consider $SG1731_A$ to be a position servo; $SG1731_B$ controls how quickly the position is acquired. Deadzone control results from voltage-modulating $SG1731_B$'s comparator thresholds.

Fan-temperature control safeguards instruments

You can also use a 1731 to control a fan motor's speed, regulating instrument temperature and extending fan life (**Fig 8**). At least one oscilloscope manufacturer uses this approach, and it has also found use in several military applications.

When power is applied, the thermistor, located near the fan, has a high resistive value. This condition unbalances the amplifier-driven bridge, sending pin 12 LOW. Q_1 and the fan motor are off. But as the instrument warms, thermistor resistance decreases, producing PWM signals at pin 12 and turning Q_1 and the fan motor on.

The 100-μF capacitor determines the time constant across the error amplifier; a short time constant produces audibly annoying hunting in the servo. The 50Ω resistor limits motor current, and the 1N4002 diode dampens motor spikes.

The SG1731 can function in nonmotor applications, too. The freezing point of water serves as a reference point for the calibration of various types of temperature sensors, such as platinum RTDs and thermocouples. In such applications, an ice slurry in a Styrofoam container or a Dewar bottle is usually used to achieve the 0°C condition. Although inexpensive, this approach requires constant ice replenishment and water removal and tends to be messy. As an alternative, you can use the SG1731 to provide 2-quadrant control for a Peltier-junction-type thermoelectric cooler.

Current flow in a Peltier device cools one side of the junction and heats the other; reversing the applied current causes the cold side of the junction to heat and the hot side to cool. Commercial devices use a large number of junctions to achieve high thermal capacity and are about the size of a postage stamp. They are optimized for one direction of current flow but can work both ways.

Fig 9's circuit capitalizes on this characteristic to achieve a very precise temperature reference that cools to 0°C and then settles out very quickly. Most thermal control loops settle slowly because energy can only be

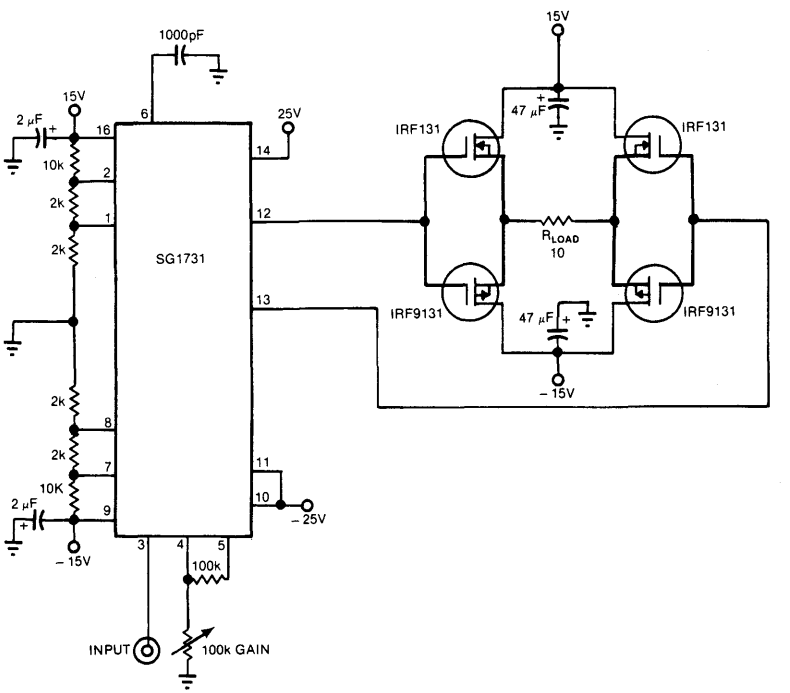
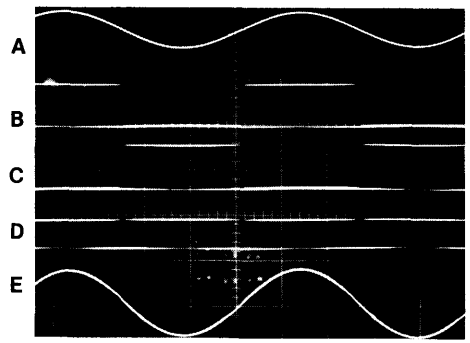


Fig 10—A switched-mode power amplifier *using a 25-kHz carrier transmits a 400-Hz waveform to a load.*

Temperature reference is bidirectional



TRACE	VERTICAL	HORIZONTAL
A	10V/DIV	500 μSEC/DIV
B	50V/DIV	500 μSEC/DIV
C	50V/DIV	500 μSEC/DIV
D	50V/DIV	500 μSEC/DIV
E	20V/DIV	500 μSEC/DIV

Fig 11—In these waveforms for Fig 10's amplifier, *trace A is the amplifier's input, traces B and C the 1731's outputs and trace D the waveform across the load. Trace E, a 3-kHz filtered version of trace D, shows that power density approximates input signal.*

removed (as in a refrigerator) or added (as in a crystal oven). But because the Peltier device is thermodynamically bidirectional, it's an ideal choice for use in a low-temperature servo.

When power is applied, the platinum sensor (at a high resistive value) unbalances the bridge and causes the AD524 instrumentation amplifier to saturate negatively. This action turns the 1731 and its 1635 drivers on, resulting in current flow through the Peltier device in the cooling direction. When the temperature reaches 0°C, the 1731 tends to cut off, causing loop overshoot. However, the heat-pump reversal in the Peltier device forces short thermal settling times.

The 100-kΩ potentiometer adjusts loop gain; the 1-μF capacitor sets bandwidth. The 100-kΩ resistors and the 0.01-μF capacitor across the instrumentation amplifier filter out the fast chopping noise the platinum sensor, a wirewound device, picks up.

If you use the resistance decade shown, you can control the junction at any desired temperature around 0°C. For an ideal 1000Ω sensor at 0°C, the **table** values shown in **Fig 9** apply. You can substitute the actual 0°C value for the platinum sensor used, biasing all values by the difference between the sensor resistance at 0°C and 1000Ω. The bidirectional thermal control and high loop gain produce very rapid response to any shift in temperature setpoint, plus high stability.

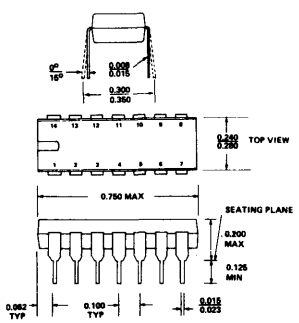
Finally, the SG1731's 2-quadrant capability allows its use as a switched-mode (Class D) power amplifier. Motors and other devices that can integrate the time-power spectrum of a Class D amplifier output are obvious loads. The design can also serve audio applications but requires careful attention to output filtering to achieve acceptable distortion levels.

Fig 10 shows the 1731 set up to deliver high power to a 10Ω load via complementary power FETs. The device's output stage swings ±25V, providing a 10V enhancement for turning on the FETs. The active 1731 outputs are ideal for driving power FETs because they can both source and sink the relatively high gate currents caused by the FETs' input capacitances. **Fig 11** shows the waveforms associated with this circuit. **EDN**

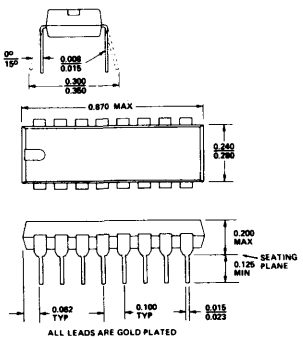
SILICON GENERAL PACKAGE RATINGS

Package Type	Thermal Resistance (°C/W)				Power Dissipation (mW)	Derate above 25°C (mW/°C)
	θ_{JC}		θ_{JA}			
	Typ.	Max.	Typ.	Max.		
K (TO-3)	3.0	5.5	35	45	4300	30
P (TO-220)	3.0	5.0	60	65	2000	16
R (TO-66)	5.0	6.0	40	50	3000	24
T (TO-39)	15	25	120	185	1000	6.7
T (TO-99)	25	40	150	190	680	5.4
T (TO-96)	25	40	130	165	800	6.8
T (TO-100)	25	40	150	190	680	5.4
T (TO-101)	25	40	150	190	680	5.4
J (16-pin)	45	60	80	110	1000	6.7
J (14-pin)	45	60	80	110	1000	6.7
Y (8-pin)	50	60	125	150	800	8
N (16-pin)	50	60	130	150	600	6.0
N (14-pin)	50	60	130	150	600	6.0
M (8-pin)	50	60	160	190	400	4.0
F (10-pin)	40	60	170	190	500	3.3

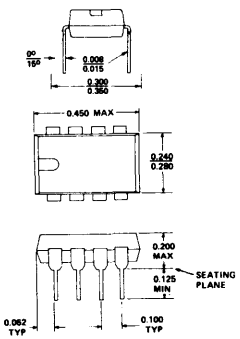
PLASTIC PACKAGES



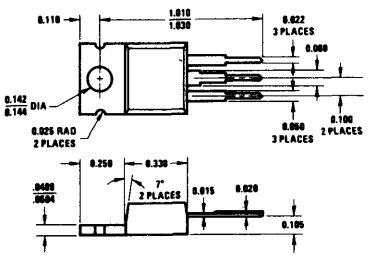
N-PACKAGE
14-PIN PLASTIC



N-PACKAGE
16-PIN PLASTIC

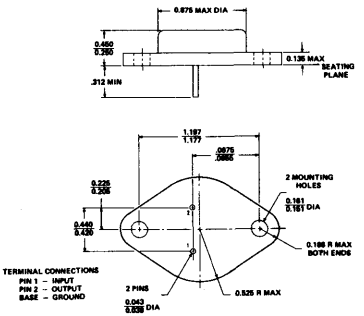


M-PACKAGE
8-PIN MINIDIP

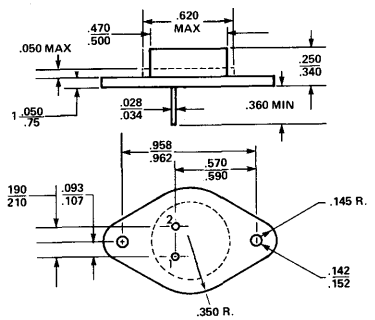


P-PACKAGE
TO-220

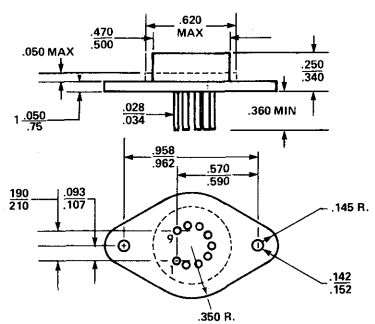
POWER PACKAGES



K-PACKAGE
TO-3

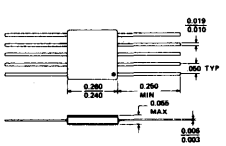


R-PACKAGE
TO-66, 2-PIN



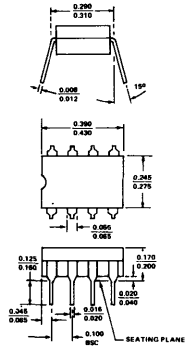
R-PACKAGE
TO-66, 9-PIN

FLATPACK

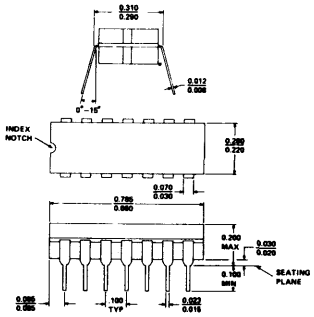


F-PACKAGE
10-PIN FLATPACK

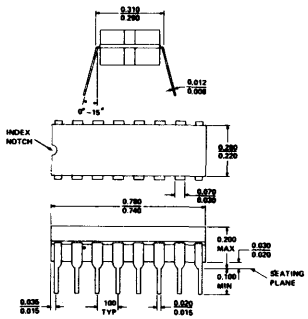
CERAMIC PACKAGES



Y-PACKAGE
8-PIN CERDIP

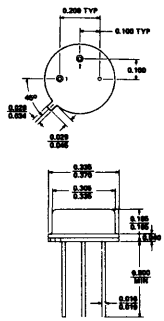


J-PACKAGE
14-PIN CERDIP

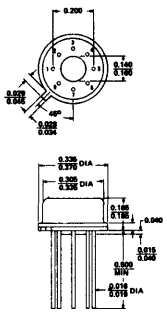


J-PACKAGE
16-PIN CERDIP

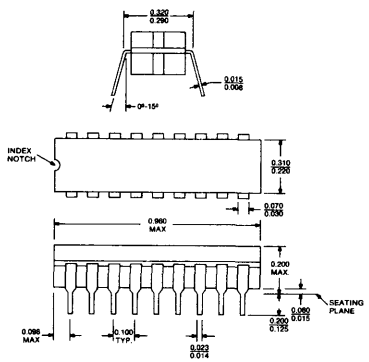
METAL CANS



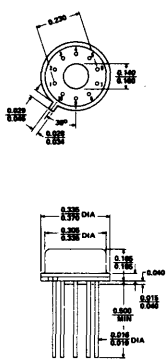
T-PACKAGE
TO-39



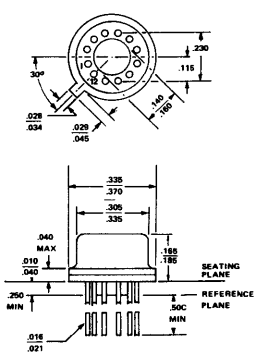
T-PACKAGE
TO-99



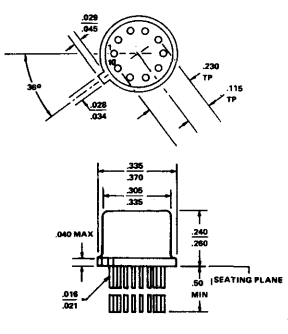
J-PACKAGE
18-PIN CERDIP



T-PACKAGE
TO-100



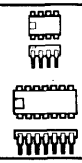
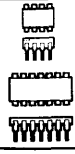
T-PACKAGE
TO-101



T-PACKAGE
TO—96

10

INDUSTRY PACKAGE CROSS-REFERENCE

	Silicon General	NSC	Signetics	Fairchild	Motorola	TI	RCA	AMD	Raytheon	Sprague
 Plastic DIP 8-Lead	M	N	V A	T	P	P	E	PC	N DN DP	M
14,16 and 18 Lead	N		B	P	P	N	E	PC	MP	A
 TO-220	P	T	U	U	T	KC				T
 Low Temperature Glass Hermetic Flat-Pack	F	W		F	F	W		FM		J
 TO-66 3 Lead 5 Lead 9 Lead	R			P	R				R TK	
 Glass/Metal Flat-Pack	F	F	Q	F	F	F S	K	F	J F Q	
 TO-5, TO-39, TO-96, TO-99, TO-100 and TO-101	T	H	T K L DB	H	G	L	S* V1**	H	T H	D K
 Ceramic DIP 8-Lead Ceramic DIP 14,16 and 18 Lead	Y J	J	F	D	U L	J			DC DD	R
 TO-3 (Steel) (Aluminum)	K	K KC	DA	K	K	K	K		K LK	
 SIP	S									W
 Leadless Package	L			L		FC	LH	L		
 Batwing	W					NE				B

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Sunnyvale, CA 94086
(408) 734-5470

R. V. Weatherford
1310 Kifer Road
Sunnvale, CA 94086
(408) 738-8694

Zeus
3350 Scott Blvd.
Building U4
Santa Clara, CA 95051
(408) 727-0714

CALIFORNIA (Southern)
Pacesetters Elect.
3137 W. Warner Ave.
Santa Ana, CA 92704
(714) 557-7131
TWX: 910-595-1704

Anthem Electronics
21730 Norhoff St.
Chatsworth, CA 91311
(818) 700-1000

Anthem Electronics
4125 Sorrento Valley Blvd.
San Diego, CA 92121
(619) 279-5200

Anthem Electronics
2661 Dow Ave.
Tustin, CA 92680
(714) 730-8000
(213) 582-2122

Diplomat/Westates Elec.
20151 Bahama St.
Chatsworth, CA 91311
(818) 700-8700

I.E.C.
20600 Plummer St.
Chatsworth, CA 91311
(818) 998-2200
TWX: 910-494-4917

I.E.C.
17062 Murphy Ave.
Irvine, CA 92714
(714) 660-1055

R. V. Weatherford
18 E. Ortega St.
Santa Barbara, CA 93101
(805) 965-8551

R. V. Weatherford
1550 Babbitt Ave.
Anaheim, CA 92805
(714) 634-9600
TWX: 910-593-1334

R. V. Weatherford
6921 San Fernando Rd.
Glendale, CA 91201
(213) 849-3451
TWX: 910-498-2223

R. V. Weatherford
1095 E. 3rd St.
Pomona, CA 91766
(714) 623-1261
(213) 966-8461
TWX: 910-581-3811

R. V. Weatherford
7665 Formula Pl.
San Diego, CA 92121
(619) 278-7400
TWX: 910-335-1570

R. V. Weatherford
18 E. Ortega St.
Santa Barbara, CA 93101
(805) 965-8551

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20151 Bahama St.
Chatsworth, CA 91311
(818) 700-8700

Diplomat/Westates Elec.
140 McCormick Ave.
Costa Mesa, CA 92626
(714) 549-8401

Diplomat/Westates Elec.
9787 Aero Dr.
San Diego, CA 92123
(619) 292-5693

Zeus West
1130 Hawk Circle
Anaheim, CA 92807
(714) 632-6880
TWX: 910-591-1696

COLORADO
Diplomat Electronics
96 Inverness Dr., E
Unit R
Englewood, CO 80112
(303) 799-8300

IEC
5750 N. Logan St.
Denver, CO 80216
(303) 292-6121

Anthem
8200 S. Akron St.
Englewood, CO 80112
(303) 790-4500

R. V. Weatherford
7000 N. Broadway
Bldg. 2, Suite 208
Denver, CO 80221
(303) 428-6900
TWX: 910-931-2222

CONNECTICUT
Diplomat Electronics
52 Federal Rd.
Danbury, CT 06810
(203) 797-9674

Milgray Electronics, Inc.
378 Boston Post Road
Orange, CT 06477
(203) 795-0711

FLORIDA

Diplomat Electronics
1300 N.W. 65th Place
Fort Lauderdale, FL 33309
(305) 974-8700

Milgray Electronics, Inc.
1850 Lee Road
Winter Park, FL 32789
(305) 647-5747

Zeus
422 26th St.
Bradenton, FL 33505
(813) 748-3125

GEORGIA
Diplomat Electronics
6679 Peachtree
Industrial Blvd., Suite B
Norcross, GA 30092
(404) 449-4133

Milgray Electronics, Inc.
17 Dunwoody Park
Atlanta, GA 30338
(404) 393-9666

ILLINOIS
Diplomat Lakeland
1071 Judson
Bensenville, IL 60106
(312) 595-1000

IEC
2200 Stonington Ave.
Suite 210
Hoffman Estates, IL 60195
(312) 843-2040

R. M. Electronics
265 Eisenhower Lane South
Lombard, IL 60148
(312) 932-5150
TWX: 910-651-3245

INDIANA
R. M. Electronics
5545 W. Raymond St.
Suite K
Indianapolis, IN 46241
(317) 247-9701

IOWA
Deeco
2500 16th Ave. S.W.
Cedar Rapids, IA 52406
(319) 365-7551
TWX: 910-525-1332

KANSAS
Milgray Electronics, Inc.
6901 West 63rd St.
Overland Park, KS 66202
(913) 236-8800

MARYLAND
Diplomat Electronics
9150 Rumsey Rd.
Columbia, MD 21045
(301) 995-1226

Kierulff Electronics
202 Azar Court
Baltimore, MD 21227
(301) 247-5020

Milgray Electronics, Inc.
11820 Parklawn Dr.
Rockville, MD 20852
(301) 468-6400

MASSACHUSETTS
Diplomat/New England, Inc.
28 Commings Park
Woburn, MA 01801
(617) 935-6611

Green-Shaw Company
70 Bridge St.
Newton, MA 02195
(617) 969-8900
Telex: 92-2498

Milgray Electronics, Inc.
79 Terrace Hall Ave.
Burlington, MA 01803
(617) 272-6800

Zeus
429 Marrett Rd.
Lexington, MA 02173
(617) 863-8800

MICHIGAN
R. M. Electronics
4310 Rob Chaffee, S.E.
Grand Rapids, MI 49508
(616) 531-9300

MINNESOTA
Industrial Components
5229 Edina Industrial Blvd.
Minneapolis, MN 55435
(612) 831-2666
TWX: 910-576-3153

MISSOURI
Olive Industrial Electronics
9910 Page Blvd.
St. Louis, MO 63132
(314) 426-4500
TWX: 910-763-0720

Kierulff Electronics
Metro Park
2608 Metro Park Blvd.
Maryland Heights, MO 63043
(314) 739-0855
TWX: 910-762-0721

NEW JERSEY (Northern)
Diplomat/IPC
490 S. Riverview Dr.
Totawa, NJ 07512
(201) 785-1830

Vantage Components, Inc.
257 Park Ave.
Nutley, NJ 07110
(201) 667-1840
TWX: 710-989-1401

Milgray Electronics, Inc.
3002 Greentree Executive
Campus
Marlton, NJ 08053
(609) 983-5010

NEW MEXICO
(Contact Factory)

NEW YORK
Diplomat Electronics
110 Marcus Dr.
Melville, NY 11747
(516) 454-6400
Telex: 14-3242

Diplomat Electronics
4610 Wetzel Rd.
Liverpool, NY 13088
(315) 652-5000

Jaco Electronics
145 Oser Ave.
Hauppauge, L.I., NY 11787
(516) 273-5500
TWX: 510-227-6232

Nu-Horizons
238 Route 109
Farmingdale, NY 11735
(516) 694-2500

Summit Electronics
916 Main St.
Buffalo, NY 14202
(716) 884-3450
TWX: 710-522-1692

Summit Electronics
292 Commercial Dr.
Rochester, NY 14623
(716) 334-8110

Zeus Components, Inc.
100 Midland Ave.
Port Chester, NY 10573
(914) 937-7400
TWX: 710-567-1248

Milgray Electronics, Inc.
77 Schmitt Blvd.
Farmingdale, NY 11735
(516) 420-9800

Milgray
57 Monroe Ave.
Pittsford, NY 14534
(716) 385-9330

OHIO
Milgray Electronics, Inc.
6155 Rockside Road
Cleveland, OH 44131
(216) 447-1520

Kierulff Electronics
23060 Miles Road
Cleveland, OH 44128
(216) 587-6558

OKLAHOMA
Quality Components
9934 E. 21st St. S.
Tulsa, OK 74129
(918) 664-8812

Kierulff Electronics
Metro Park
12318 E. 60th St.
Tulsa, OK 74145
(918) 252-7537
TWX: 910-845-2150

Quality Components
9934 E. 21 St., S.
Tulsa, OK 74129
(918) 664-8812

PENNSYLVANIA
(Contact Factory)

TEXAS
Quality Components
2427 Rutland
Austin, TX 78758
(512) 835-0220

Quality Components
4257 Kellway Cir.
Addison, TX 75001
(214) 387-4949
TWX: 910-860-5459

Zeus
14001 Goldmark
Suite 250
Dallas, TX 75240
(214) 783-7010

Jaco
1209 Glenville Dr.
Richardson, TX 75080
(214) 235-9575

Quality Components
6126 Westline
Houston, TX 77036
(713) 772-7100
TWX: 910-881-7251

R. V. Weatherford
4658 Sunbelt Rd.
Dallas, TX 75248
(214) 243-1571
TWX: 910-880-5544

R. V. Weatherford
3500 West T. C. Jester Blvd.
Houston, TX 77018
(713) 688-7406
TWX: 910-881-6222

Kierulff Electronics
9610 Skillman Ave.
Dallas, TX 75243
(214) 343-2400
TWX: 910-861-9149

Kierulff Electronics
10415 Landsbury Dr.
Suite 210
Houston, TX 77099
(713) 530-7030
TWX: 910-860-4057

Kierulff Electronics
3007 Longhorn Blvd.
Suite 105
Austin, TX 78758
(512) 835-2090
TWX: 910-874-1359

UTAH
Diplomat/Alta
3007 S.W. Temple
Salt Lake City, UT 84115
(801) 486-4134

IEC
101 N. 700 West
N. Salt Lake City, UT
(801) 298-1869

WASHINGTON
R. V. Weatherford
541 Industry Dr.
Seattle, WA 98188
(206) 575-1340
TWX: 910-444-2270

I.E.C.
1750 124th Ave. N.E.
Bellevue, WA 98005
(206) 455-2727

WISCONSIN
Marsh Electronics
1563 S. 101 St.
Milwaukee, WI 53214
(414) 475-6000
TWX: 910-262-3321

CANADA
Future Electronics Corp.
4800 Dufferin St.
Downsview, Ontario M3H 5S8
(416) 663-5563

FUTURE Electronics Corp.
237 Hymus Blvd.
Pointe Claire (Montreal)
Quebec, Canada H9R 5C7
(514) 694-7710
TWX: 610-491-1470

Future Electronics Inc.
Baxter Center
1050 Baxter Rd.
Ottawa, Ontario K2C 3P2
(613) 820-8313
TWX: 610-563-1697

Canadian General Electric
189 Dufferin St.
Toronto, Ontario M6K 1Y9
(416) 530 2986
TWX: 06-23238

Silicon General

LINEAR INTEGRATED CIRCUITS

INTERNATIONAL

ARGENTINA
YEL srl
Cangallo 1454, Piso 8 of, 41
(1037) Buenos Aires
Argentina
Tel: 46-2211
Telex: 18605

AUSTRIA
Othmar Lackner Electronics
Singerstr 2
A-1010 Wien, Austria
Tel: 222/531185
Telex: 111198

AUSTRALIA
AJ Distributors Pty. Ltd.
44 Prospect Rd.
Prospect, S. Australia 5082
Tel: (08) 2691244
Telex: 82635

BELGIUM
Heynen b.v.
Bedrijfsstraat 2
3500 Hasselt 2
Belgium
Tel: 011-210006
Telex:39047

CANADA (Except B.C.)
Vitel Electronics
3300 Cote Vertu,
Suite 203
St. Laurent, Quebec
Canada H4R 2B7
Tel: (514) 331-7393
Telex: 05 821762
TWX: 610-421-3124

Vitel Electronics
5945 Airport Rd.
Suite 180
Mississauaga, Ontario
Canada L4V 1R9
Tel. (416) 676-9720
TWX: 610-492-2528

Vitel Electronics
4019 Carling Ave.
Kanata, Ontario
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TWX: (610) 421-3124

CANADA (B.C. only)
N.R. Schultz Company
300 120th St., N.E.
Bellevue, WA 98009
Tel: (206) 454-0300
TWX: 910-443-2329

DENMARK
E.V. Johanssen Elektronik
15 Titangade
DK-2200
Copengahen N. Denmark
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Telex: 885-16522

FINLAND
Panta-Tuote OY
Karakalliontie 3F61
02620 Espoo 62
Finland
Tel: 90-598525
Telex: 12-1394

FRANCE
Radio Equipements-Antares
Boite Postale No. 5
92301 Levallois-Perret
Paris, France
Tel: 758-11-11
Telex: 842-620630

GERMANY
Neumuller GMBH
8028 Munchen Taufkirchen
Eschenstr, 2 Germany
Tel: 089-61181
Telex: 5-22106

Astronic GMBH
Winzerestr 47D
8000 Munchen 40
West Germany
Tel: 089-309031
Telex: 5216187

HONG KONG
Tektron Electronics Ltd.
1702 Bank Center
636 Nathan Rd.
Kowloon, Hong Kong
Tel: 3-856199
Telex: 780-38513

INDIA
Zenith Electronics
541, Panchratna
Mama Parmanand Marg.
Bombay 400 004, India
Tel: 384214
Telex: 011-3152

ISRAEL
Talviton Electronics Ltd.
P.O. Box 21104
9, Biltmor St.
Tel Aviv, Israel
Tel: 44-45-72
Telex: 033400

ITALY
Exhibo Italiana, S.P.A.
Via F. Frisi, 22
20052 Monza, Italy
Tel: 039-360021
Telex: 333315

JAPAN
Hakuto Company Ltd.
C.P.O. Box 25
Tokyo 100-91, Japan
Tel: 03-502-2211
Telex: J22912A

NETHERLANDS (Holland)
Heynen b.v.
Postbus 10
NL 6590AA Gennep
Steendalerstraat 56
Netherlands
Tel: 08851-1956
Telex: 37282

NORWAY
Henaco
Trondheimsveien 436
Ammerud
Oslo, Norway
Tel: 02-645040
Telex: 16716 HENACN

PUERTO RICO
M. Anderson Co., Inc.
Suite 18 3rd Floor
Edifisio El Monte Hall
Hato Ray, P.R. 00918
Tel: (809) 751-2026
Telex: 345 0531

REPUBLIC OF CHINA
Helm Engineering & Trading
9FL, 143, HSIN YI RD, SEC 4
Taipei, Taiwan, R.O.C.
Tel: (02) 781-0003
Telex: 28204

SOUTH AFRICA
Electronic Bldg. Elements
South Africa (Pty) Ltd.
P.O. Box 4609
Pretoria, 0001
Rep. of South Africa
Tel: 469221
Telex: 960-440181

SPAIN
Amitron S.A.
Loecheo LE 6
Madrid 8, Spain
Tel: 2485863
Telex: 45550

SWEDEN
Svensk Teleindustri AB
Box 502
S-16205 Vallingby 5
Sweden
Tel: 08-380320
Telex: 13033

SWITZERLAND
Kontron Electronics
Bernerstr Sud 169
8048 Zurich Switzerland
Tel: 01 4354111
Telex: 58836

UNITED KINGDOM
Power Technology Ltd.
Bulton Rd.
Reading, Berkshire, RG20LT
England
Tel: (734) 866 766
Telex: 847203

OTHER COUNTRIES
Total Electronics
3630 Enterprize St.
San Diego, CA 92138
Tel: (619) 224-3291
Telex: 69-7966

Silicon General
LINEAR INTEGRATED CIRCUITS

CUSTOM CIRCUITS CAPABILITY

Silicon General designs and produces standard and custom integrated circuits in high volume. The full complement of logic elements can be integrated with operational amplifiers, comparators and power drivers to produce low cost, high performance system design. Over 500 logic gates may be integrated with power drivers and linear circuits.

Short Design Cycles are possible. Silicon General has the basic building block devices and logic elements in its CAD data base. Often prototypes, based on metal mask changes to existing standard products, can be delivered within twelve weeks. Other designs may require 20 to 40 weeks.

Unit Cost is directly related to chip size, package and volume. A minimum volume order is required. Silicon General's engineering staff will work with the customer's engineers to develop the most cost effective design for the total system.

The Specification for a custom device should be well defined. Silicon General's engineers will work with the customer to develop a solid specification.

PACKAGING

DIP to 40 pins (ceramic or plastic)
Power SIP (12 and 15 pins)
TO-3
TO-39
TO-66
TO-96
TO-99
TO-100
TO-101
TO-220
Flatpack
Leadless chip carrier
Custom
Silicon General sells dice.

TYPICAL CUSTOM DESIGN SCHEDULE

Task	Time in Weeks	Responsibility
Define Specification	—	Shared
Circuit Design	2 to 10	Silicon General
Breadboard Construction	2 to 8	Silicon General
Breadboard Approval	2 to 4	Customer
Circuit Layout	2 to 8	Silicon General
Prototype Build	3 to 8	Silicon General
Prototype Approval	3 to 4	Customer
Production Volume	12 to 16	Silicon General

Power Transistors	Sourcing — to 4A at 60V Sinking — to 4A at 60V (Several Power Transistors may be combined on a single chip).
Transistors	NPN — Beta to 300 BV_{CES} to 120V f_t to 500 MHz PNP — Beta to 40 BV_{CES} to 100V f_t to 4 mHz
Diodes	Small Signal — BV = 7.0V Zener — 5.7 to 7.0 ±0.3V Large Signal — BV = 100V at 4A
Resistors	0.1 to 2M Ohms (±20%) (Ratios within less than 1% are possible)
Capacitors	0.05 pF to 300 pF
Linear Circuit Elements	Operational Amplifiers Regulators Comparators Oscillators Power Amplifiers Custom
Logic Circuit Elements	Standard Gates: AND, NAND, OR, NOR, XOR, etc Flip/flops and Latches One Shots Shift Registers Custom (Standard bipolar gates with propagation delays of 10 nS per gate and I^2L gates of 100 nS per gate)

SILICON GENERAL

Linear 1984-85

SILICON GENERAL

IC Solutions for Power Management

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Garden Grove, California 92641
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